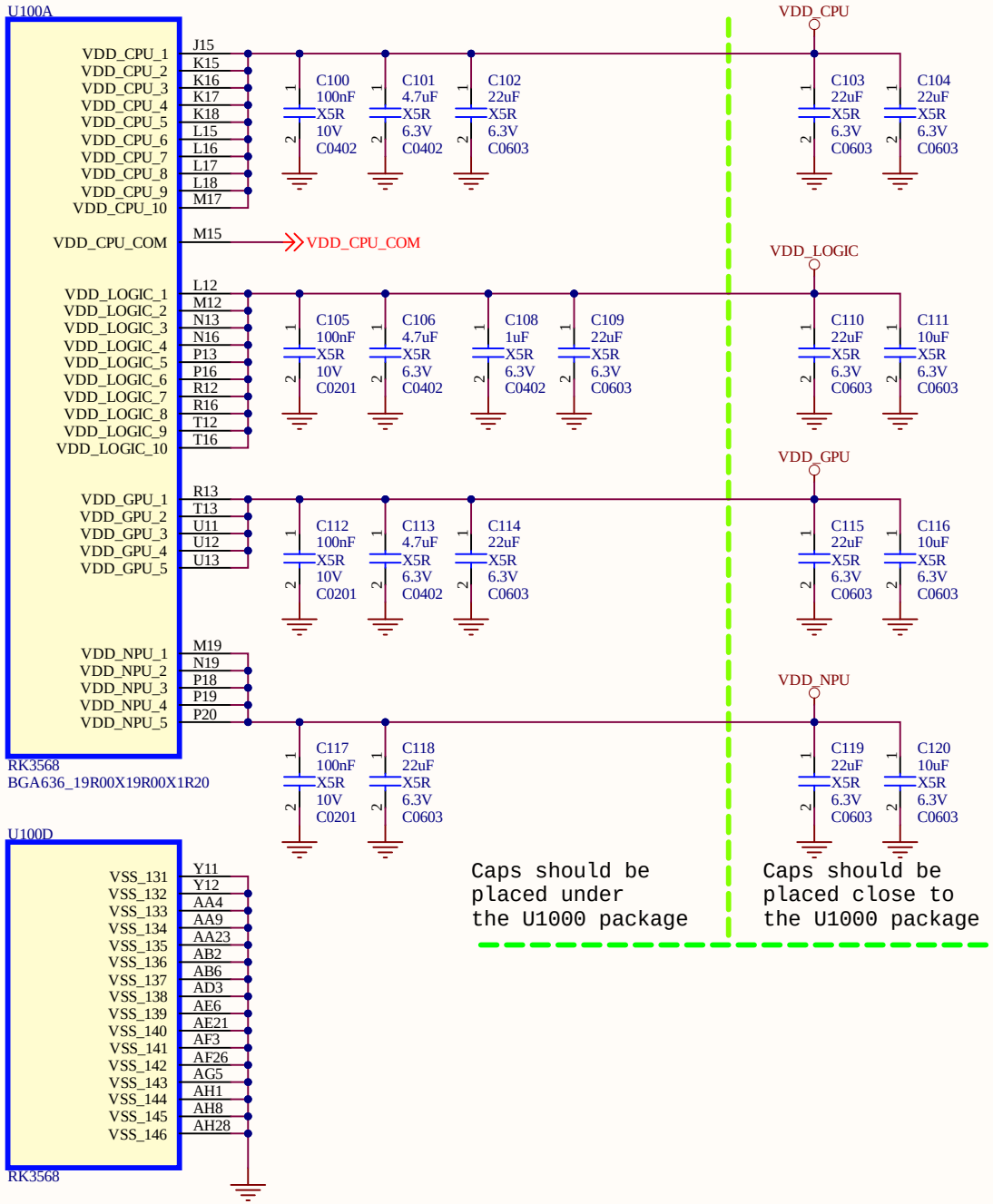
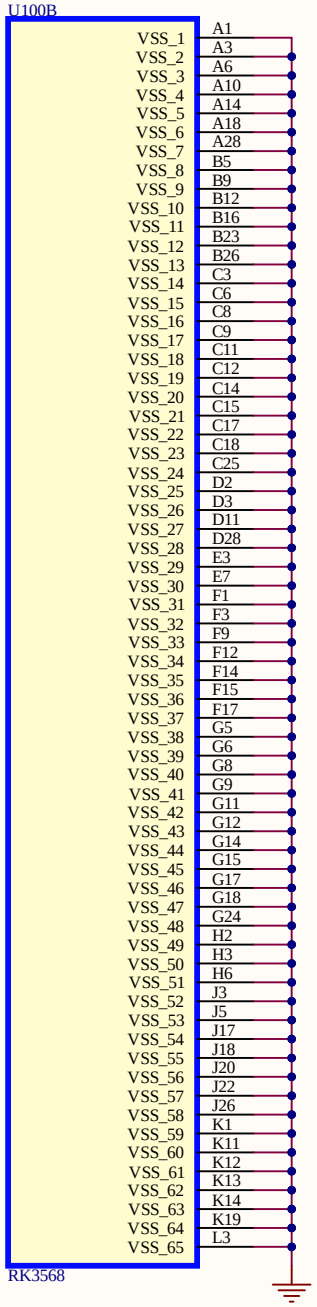
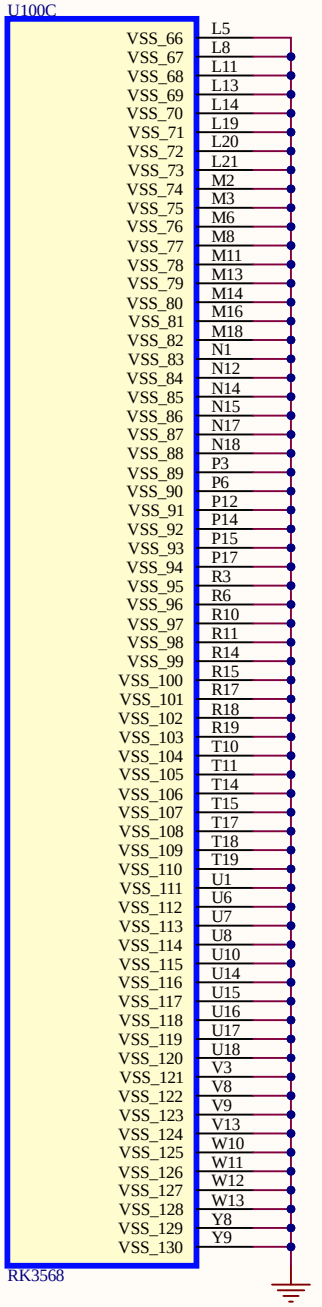
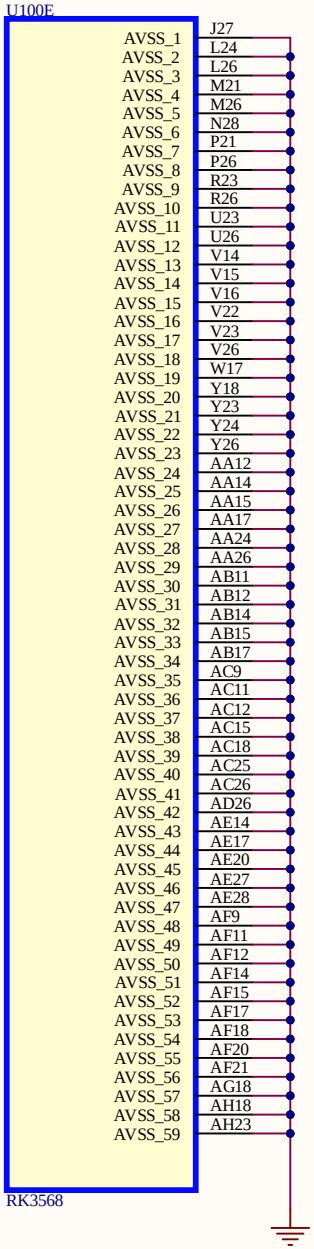
RK3568_ABCDE (Power&Gnd)









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RK3568_F (DDR PHY)

U100F

DDR4	LPDDR4	DDR3	LPDDR3		DDR4	LPDDR4	DDR3	LPDDR3	
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15	DDR4_A0	**LPDDR4_CLKP_B**	DDR3_A9	---	AC0
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14	DDR4_A1	---	DDR3_A2	---	AC1
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10	DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9	DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13	DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12	DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8	DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11	DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1	DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P	DDR4_A9	**LPDDR4_CLKN_B**	DDR3_A5	---	AC9
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
					DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8	AC11
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25	DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24	DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28	DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29	DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26	DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31	DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30	DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27	DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3	DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P	DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N	DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC22
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1	**DDR4_CLKP**	**LPDDR4_CLKP_A**	**DDR3_CLKP**	**LPDDR3_CLKP**	AC23
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5	**DDR4_CLKN**	**LPDDR4_CLKN_A**	**DDR3_CLKN**	**LPDDR3_CLKN**	AC24
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6	DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4	DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26
DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2	DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3	DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7					
DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0	DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29
DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0					
DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P					
DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N					
DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18					
DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19					
DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22					
DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23					
DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16					
DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17					
DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20					
DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21					
DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2					
DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P					
DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N					
DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0						
DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1						
DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2						
DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3						
DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4						
DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5						
DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6						
DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7						
DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM						
DDR_ECC_DQS/P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P						
DDR_ECC_DQS/N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N						

RK3568

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

DDR_RZQ

DDR_VREFOUT

DDR3L =1.35V DDR3 =1.5V DDR4 =1.2V LPDDR3 =1.2V LPDDR4 =1.1V LPDDR4x =1.1V	DDRPHY_VDDQ_1 DDRPHY_VDDQ_2 DDRPHY_VDDQ_3 DDRPHY_VDDQ_4 DDRPHY_VDDQ_5 DDRPHY_VDDQ_6 DDRPHY_VDDQ_7 DDRPHY_VDDQ_8
DDR3L =1.35V DDR3 =1.5V DDR4 =1.2V LPDDR3 =1.2V LPDDR4 =1.1V LPDDR4x **#NAME?**	DDRPHY_VDDQL_1 DDRPHY_VDDQL_2 DDRPHY_VDDQL_3 DDRPHY_VDDQL_4 DDRPHY_VDDQL_5 DDRPHY_VDDQL_6

DDR_AVSS

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

LPDDR4

VCC_DDR

C201 100nF X5R 10V C0201
C202 4.7uF X5R 6.3V C0402
C203 4.7uF X5R 6.3V C0402
C204 10uF X5R 6.3V C0603
C206 100nF X5R 10V C0201
C207 4.7uF X5R 6.3V C0402
C208 4.7uF X5R 6.3V C0402
C209 4.7uF X5R 6.3V C0402

Caps should be placed under the U1000 package

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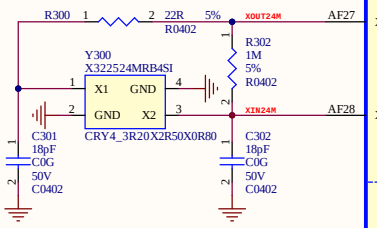
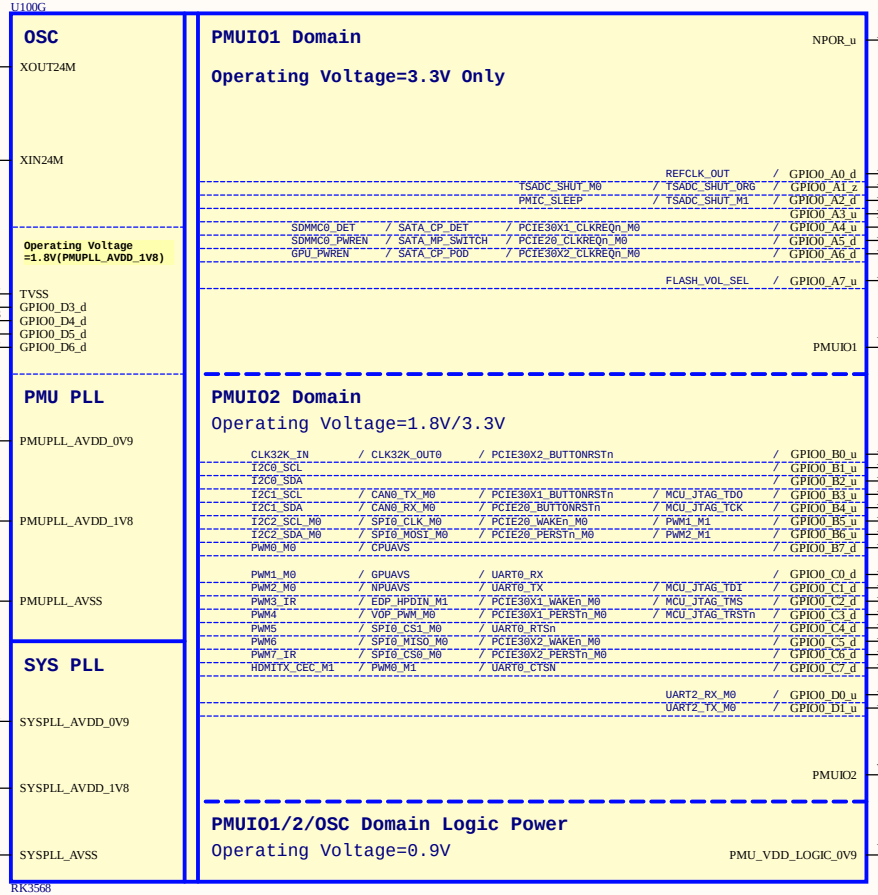
RK3568_G(OSC/PLL/PMUIO1/2)

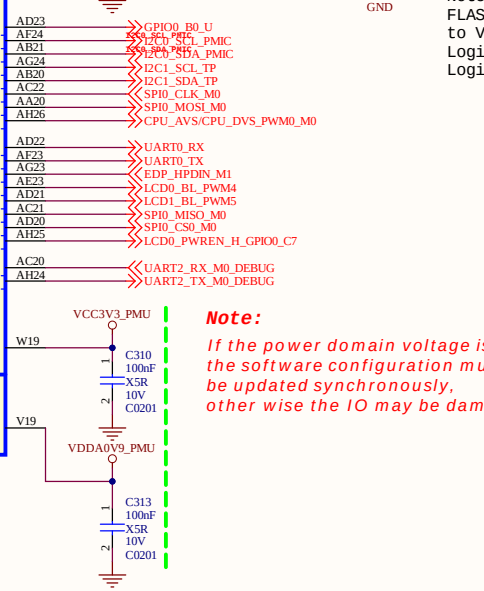
Note:

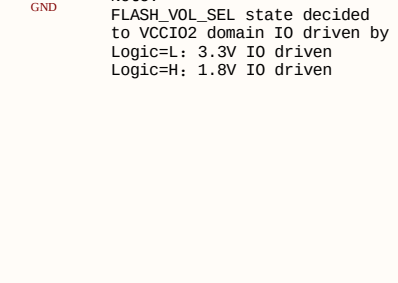
Adjusted the load capacitance
according to the crystal specification.



U100G

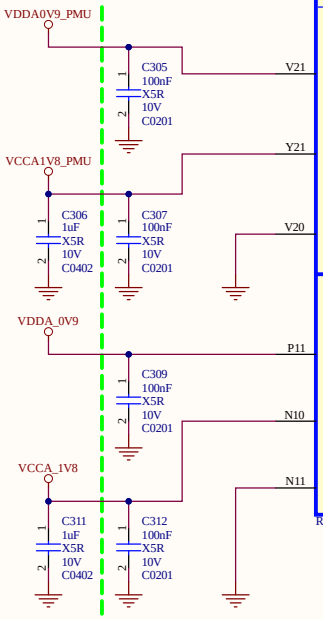


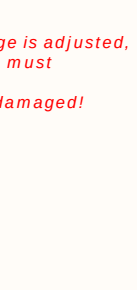




Default:24MHz

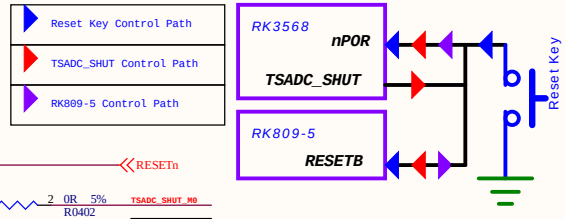
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven





Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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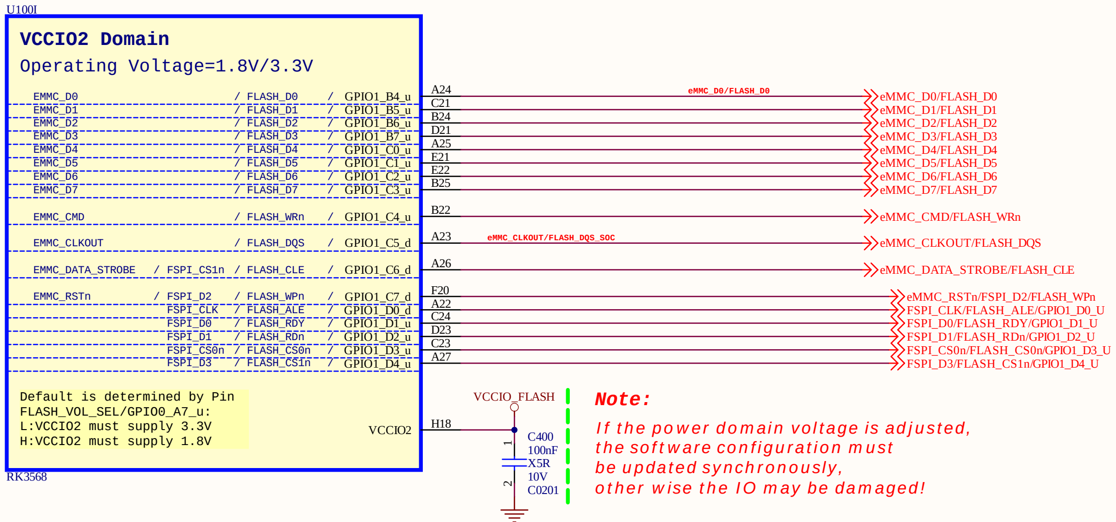
RK3568_I(VCCIO2 Domain)


U100I
VCCIO2 Domain
Operating Voltage=1.8V/3.3V
EMMC_D0 / FLASH_D0 / GPIO1_B4_u A24
EMMC_D1 / FLASH_D1 / GPIO1_B5_u C21
EMMC_D2 / FLASH_D2 / GPIO1_B6_u B24
EMMC_D3 / FLASH_D3 / GPIO1_B7_u D21
EMMC_D4 / FLASH_D4 / GPIO1_C0_u A25
EMMC_D5 / FLASH_D5 / GPIO1_C1_u E21
EMMC_D6 / FLASH_D6 / GPIO1_C2_u E22
EMMC_D7 / FLASH_D7 / GPIO1_C3_u B25
EMMC_CMD / FLASH_WRn / GPIO1_C4_u B22
EMMC_CLKOUT / FLASH_DQS / GPIO1_C5_d A23
EMMC_DATA_STROBE / FSPI_CS1n / FLASH_CLE / GPIO1_C6_d A26
EMMC_RSTn / FSPI_D2 / FLASH_WPn / GPIO1_C7_d F20
FSPI_CLK / FLASH_ALE / GPIO1_D0_d A22
FSPI_D0 / FLASH_RDY / GPIO1_D1_u C24
FSPI_D1 / FLASH_RDn / GPIO1_D2_u D23
FSPI_CS0n / FLASH_CS0n / GPIO1_D3_u C23
FSPI_D3 / FLASH_CS1n / GPIO1_D4_u A27
Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V
VCCIO2 H18
RK3568
eMMC_D0/FLASH_D0
eMMC_D0/FLASH_D0
eMMC_D1/FLASH_D1
eMMC_D2/FLASH_D2
eMMC_D3/FLASH_D3
eMMC_D4/FLASH_D4
eMMC_D5/FLASH_D5
eMMC_D6/FLASH_D6
eMMC_D7/FLASH_D7
eMMC_CMD/FLASH_WRn
eMMC_CLKOUT/FLASH_DQS_SOC
eMMC_CLKOUT/FLASH_DQS
eMMC_DATA_STROBE/FLASH_CLE
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_CLK/FLASH_ALE/GPIO1_D0_U
FSPI_D0/FLASH_RDY/GPIO1_D1_U
FSPI_D1/FLASH_RDn/GPIO1_D2_U
FSPI_CS0n/FLASH_CS0n/GPIO1_D3_U
FSPI_D3/FLASH_CS1n/GPIO1_D4_U
VCCIO_FLASH
C400
100nF
X5R
10V
C0201
Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode.

Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset,
then system will enter into Maskrom mode.

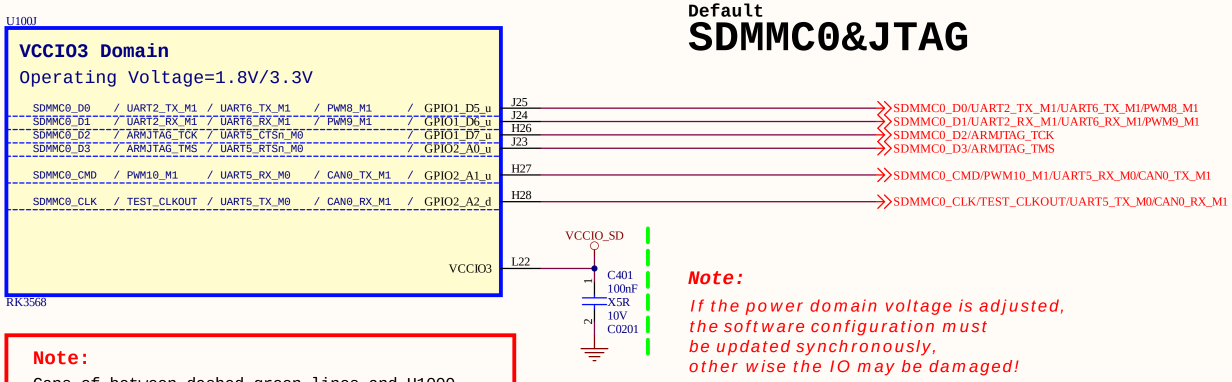
Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure,
use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

Layout note:
Test point must be placed on the line, and no branch can be added

RK3568_J(VCCIO3 Domain)

Default
SDMMC0&JTAG


U100J
VCCIO3 Domain
Operating Voltage=1.8V/3.3V
SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1 / PWM8_M1 / GPIO1_D5_u J25
SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1 / PWM9_M1 / GPIO1_D6_u J24
SDMMC0_D2 / ARMJTAG_TCK / UART5_CTSn_M0 / GPIO1_D7_u H26
SDMMC0_D3 / ARMJTAG_TMS / UART5_RTSn_M0 / GPIO2_A0_u J23
SDMMC0_CMD / PWM10_M1 / UART5_RX_M0 / CAN0_TX_M1 / GPIO2_A1_u H27
SDMMC0_CLK / TEST_CLKOUT / UART5_TX_M0 / CAN0_RX_M1 / GPIO2_A2_d H28
VCCIO3 L22
RK3568
SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1
SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1
SDMMC0_D2/ARMJTAG_TCK
SDMMC0_D3/ARMJTAG_TMS
SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1
SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1
VCCIO_SD
C401
100nF
X5R
10V
C0201
Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package

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Title		
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Date: 8/12/2024	Sheet of	
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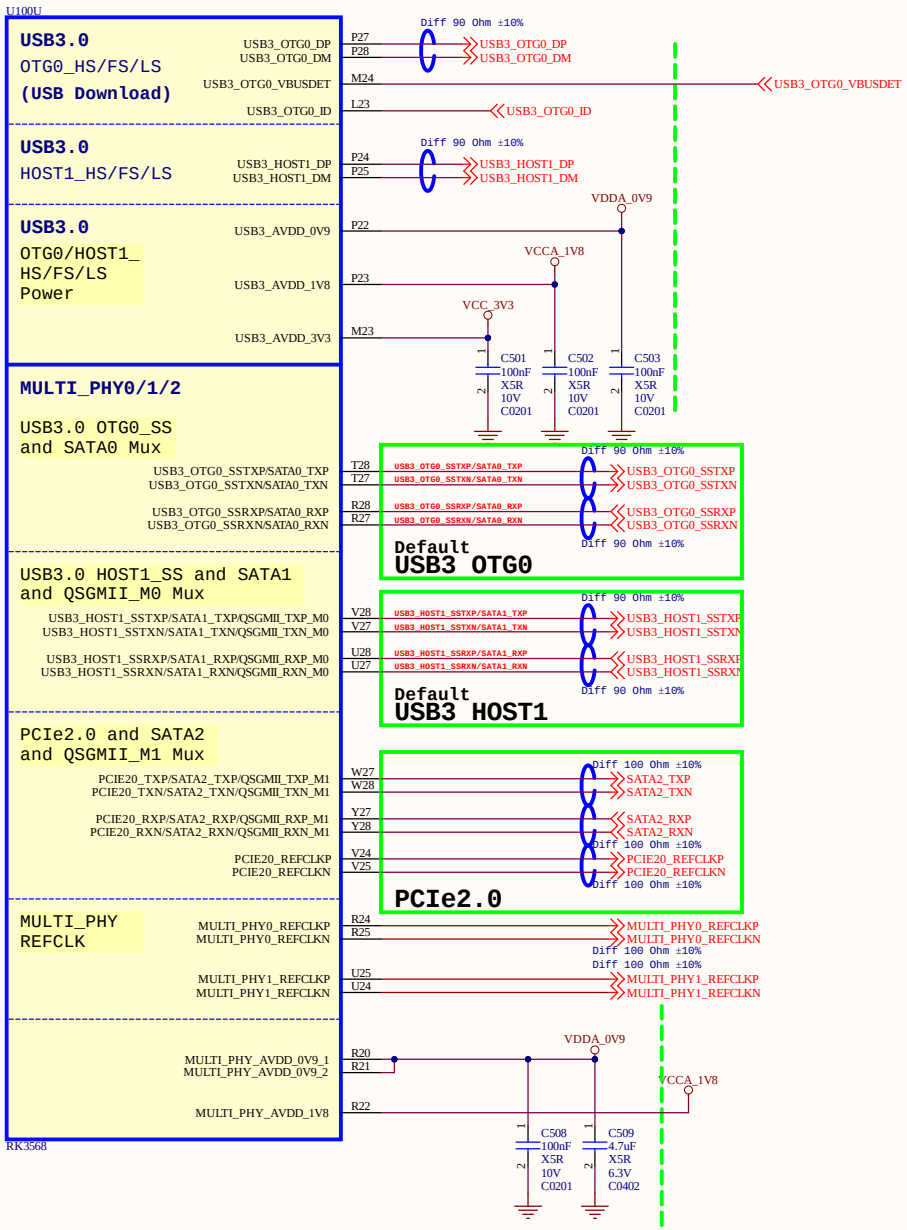
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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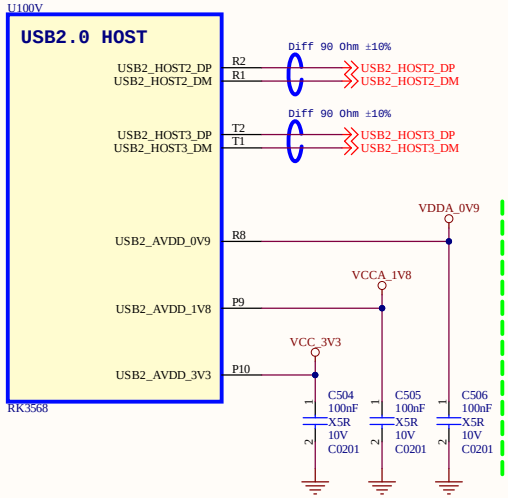
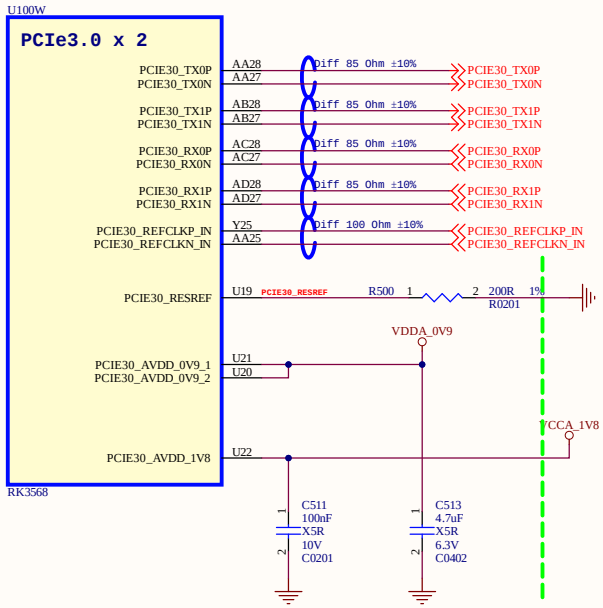
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



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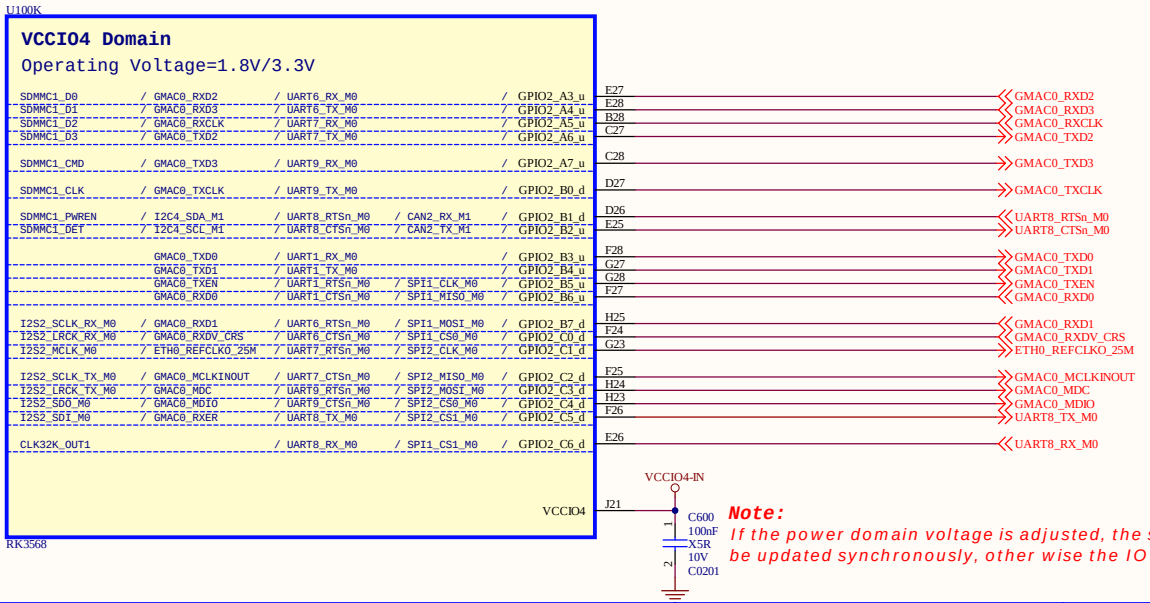
Date: 8/12/2024	Sheet of	
File: I:\2024-8-9_RK3568开发板\..\05 RK3568_USB&PCIe&SATA PHY.SchDoc	Drawn By:	

RK3568_K(VCCIO4 Domain)



RGMII0+UART8

Note:

If Ethernet PHY uses other models,
please note whether the default
pull-up and pull-down of GPIO
affect Ethernet PHY function

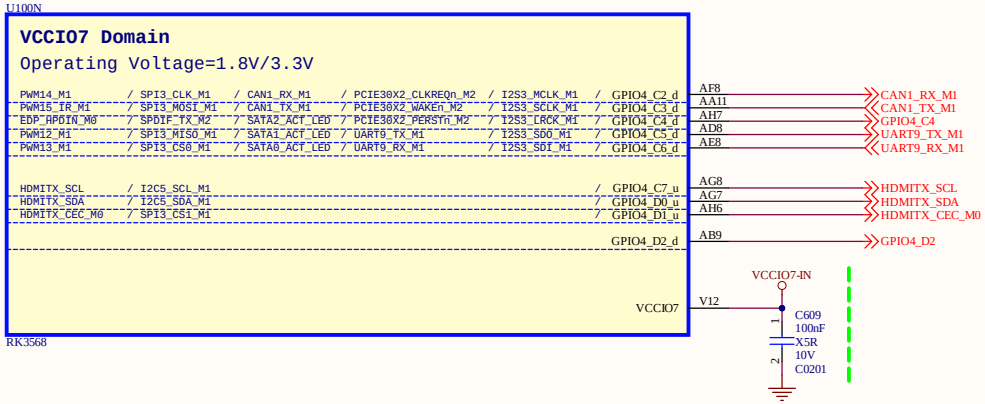
At present,
TXEN will be affected
if it defaults to high level
need to add a 4.7K
resistance to ground

Note: VCCIO4-IN

According to the actual
choice of mounted
Cannot be mounted
at the same time
Default:1.8V
Select the voltage according
to the application

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

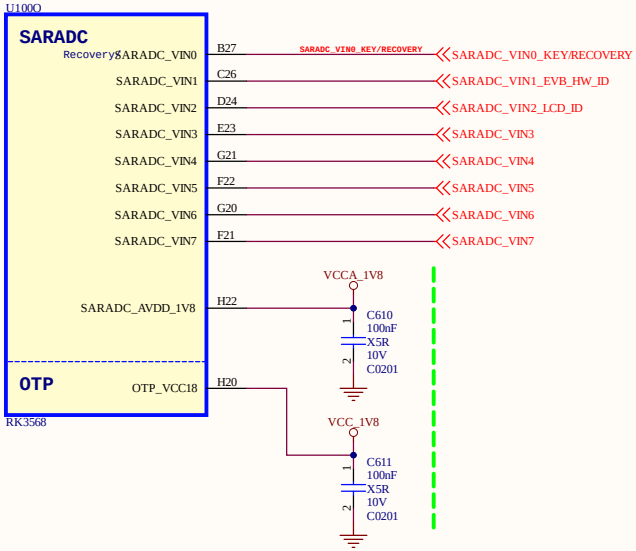


Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note: VCCIO7-IN

According to the actual
choice of mounted
Cannot be mounted
at the same time
Default:3.3V
Select the voltage according
to the application

RK3568_O(SARADC/OTP)



Note:
Must be mounted

Note:SARADC_VIN0_KEY/RECOVERY

If there is no Key requirement,
two test points must be reserved
to facilitate firmware update

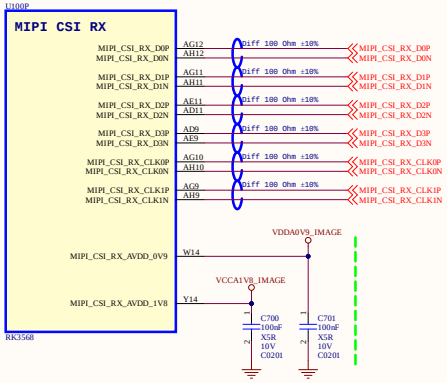
It is suggested to reserve a
Key to facilitate the
development debug

If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

Note:
Caps of between dashed green lines
and U1000 should be placed under
the U1000 package

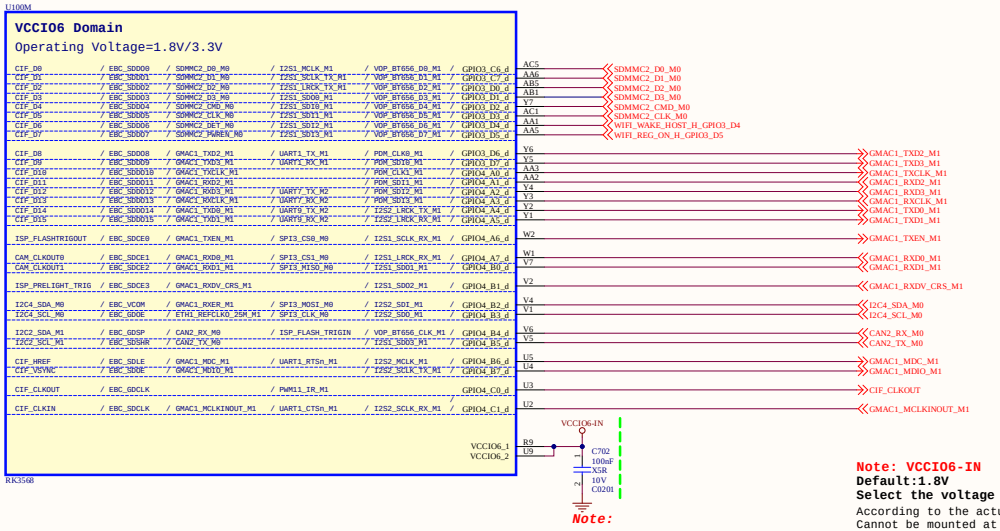
Title		
Size A4	Number	Revision
Date: 8/12/2024	Sheet of	
File: I:\2024-8-9_RK3568开发板\..\06 RK3568_SARADC&GPIO.SchDoc	Drawn By:	

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note: VCCIO6-IN
Default:1.8V
Select the voltage according to the application
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

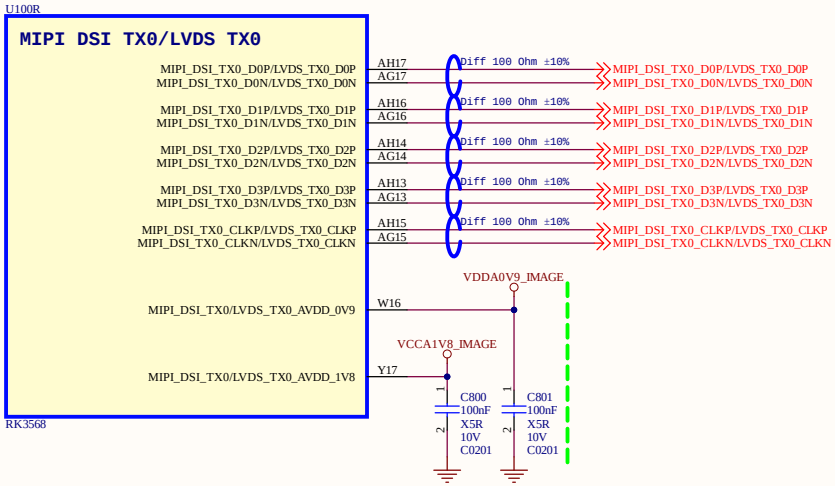
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

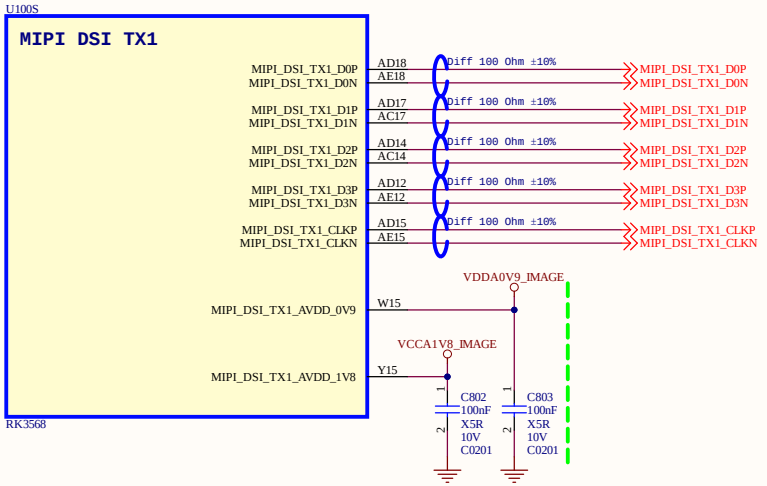
GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------>	PHYx_TXD0	GMACx_TXD0	------>	PHYx_TXD0
GMACx_TXD1	------>	PHYx_TXD1	GMACx_TXD1	------>	PHYx_TXD1
GMACx_TXD2	------>	PHYx_TXD2			
GMACx_TXD3	------>	PHYx_TXD3			
GMACx_TXEN	------>	PHYx_TXEN	GMACx_TXEN	------>	PHYx_TXEN
GMACx_TXCLK	------>	PHYx_TXCLK			
GMACx_RXD0	<------	PHYx_RXD0	GMACx_RXD0	<------	PHYx_RXD0
GMACx_RXD1	<------	PHYx_RXD1	GMACx_RXD1	<------	PHYx_RXD1
GMACx_RXD2	<------	PHYx_RXD2			
GMACx_RXD3	<------	PHYx_RXD3			
GMACx_RXDV	<------	PHYx_RXDV	GMACx_RXDV	<------	PHYx_RXDV
GMACx_RXCLK	<------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<------	PHYx_RXER
GMACx_MDC	------>	PHYx_MDC	GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<------>	PHYx_MDIO	GMACx_MDIO	<------>	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx_XTALIN			
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	------>	PHYx_XTALIN/REFCLK
GPIO	------>	PHYx_RSTn	GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB	GPIO	<------	PHYx_INT/PMEB

Title		
Size A4	Number	Revision
Date: 8/12/2024	Sheet of	
File: I:\2024-8-9_RK3568开发板\...\07 RK3568_MIPI_Interface.SchDoc	Drawn By:	

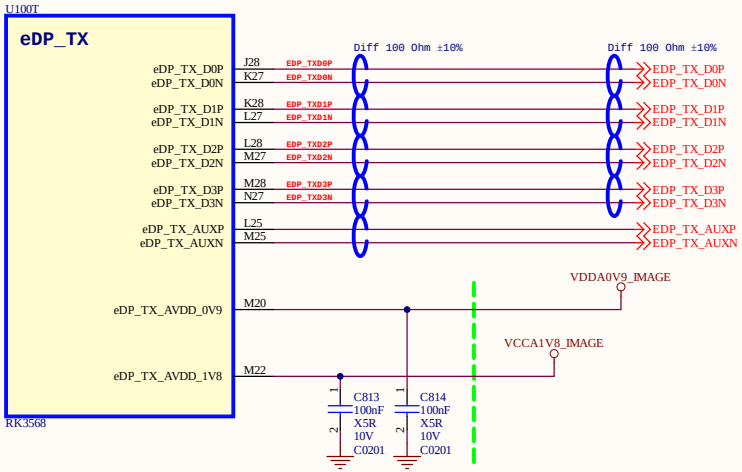
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

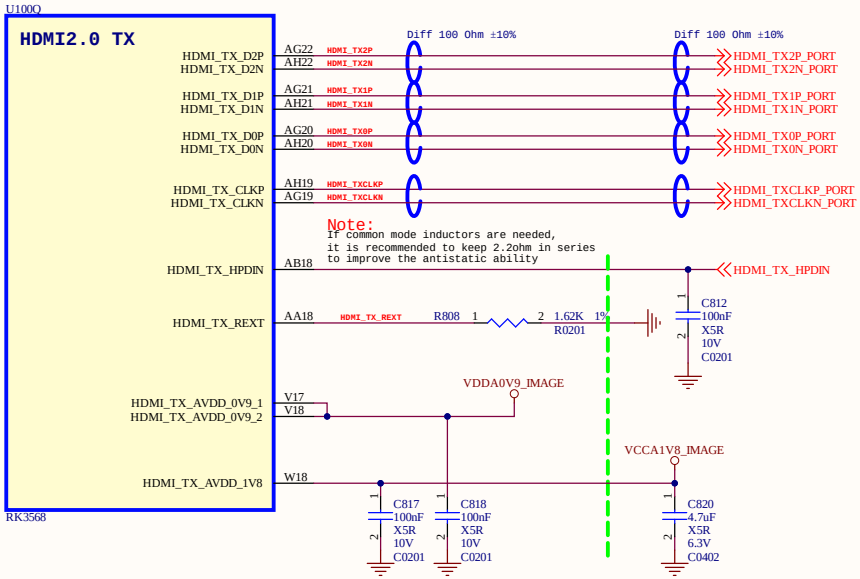


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



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Date: 8/12/2024	Sheet of	
File: I:\2024-8-9_RK3568开发板\..\08 RK3568_DVP_Interface_1.SchDoc	Drawn By:	

RK3568_L(VCCIO5 Domain)

U100L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d	AG6
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d	AD7
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d	AC8
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d	AC7
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d	AF5
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d	AF6
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d	AD6
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d	AH5
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d	AH4
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d	AB8
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d	AE5
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d	AG4
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d	AF4
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d	AH3
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d	AG3
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d	AH2
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d	AG2
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d	AG1
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d	AF2
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d	AF1
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d	AE1
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d	AE2
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d	AE3
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d	AD4
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d	AD2
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d	AD1
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d	AA7
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d	AC4
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d	AC3
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d	AC2

VCCIO5_1 V10
VCCIO5_2 V11

RK3568

GMAC1_INT/PMEB_GPIO2_D0
GMAC1_RSTn_GPIO2_D1
GMAC1_INT/PMEB_GPIO2_D2
GMAC0_RSTn_GPIO2_D3
PCIE30X2_CLKREQn_M1
PCIE30X2_WAKEn_M1
PCIE30X2_PERSTn_M1
PCIE30X2_PRSNT_L_GPIO2_D7
GPIO3_A0
SPI1_CS0_M1
GPIO3_A2
I2S3_SCLK_M0
I2S3_LRCK_M0
I2S3_SDO_M0
I2S3_SDI_M0
PCIECLKIC_OE_H_GPIO3_A7
ETH1_REFCLKO_25M_M0
UART4_RX_M1
UART4_TX_M1
I2C5_SCL_M0
I2C5_SDA_M0
GPIO3_B5
GPIO3_B6
UART3_TX_M1
UART3_RX_M1
SPI1_MOSI_M1
SPI1_MISO_M1
SPI1_CLK_M1
UART7_TX_M1
UART7_RX_M1

VCCIO5-IN
C900
100nF
X5R
10V
C0201

Note: VCCIO7-IN

According to the actual choice of mounted Cannot be mounted at the same time

Default:3.3V

Select the voltage according to the application

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Title		
Size A4	Number	Revision
Date: 8/12/2024	Sheet of	
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RK3568_H(VCCIO1 Domain)

U100H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/	GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/	GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/	GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/	GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/	GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/	GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/	GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/	GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/	GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/	GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/	GPIO1_B3_d

VCCIO1

RK3568

D18 I2C3_SDA_M0 → I2C3_SDA_M0

E18 I2C3_SCL_M0 → I2C3_SCL_M0

A19 → I2S1_MCLK_M0_RK809

B19 → I2S1_SCLK_TX_M0_RK809

F18 → GPIO1_A4_d

A20 → I2S1_LRCK_TX_M0_RK809

C20 → PDM_CLK0_M0_RK809

B20 → I2S1_SDO0_M0_RK809

D20 → GPIO1_B0_d

E20 → GPIO1_B1_d

A21 → GPIO1_B2_d

B21 → I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17

C1000
100nF
X5R
10V
C0201

Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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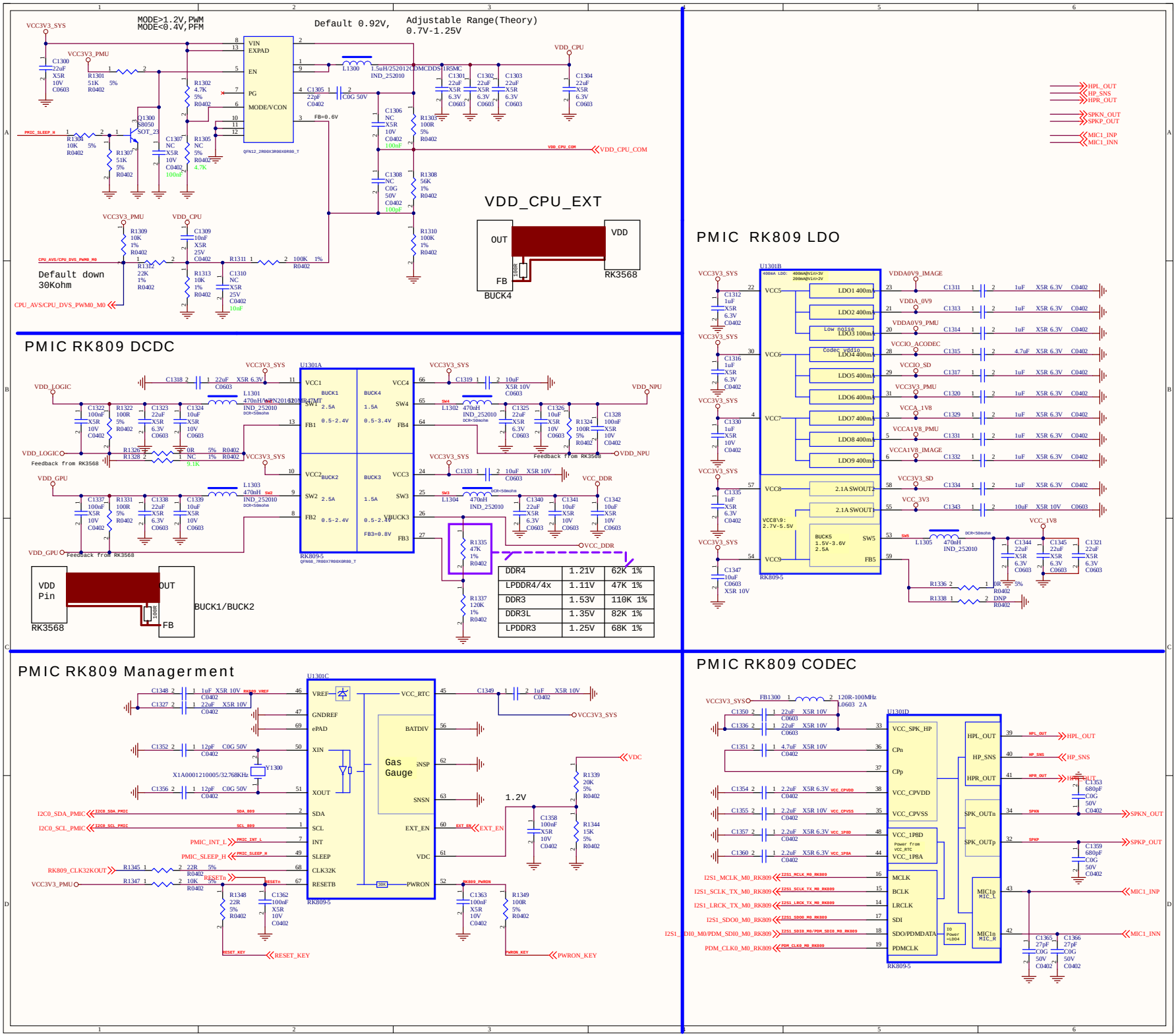
Title		
Size A4	Number	Revision
Date: 8/12/2024		Sheet of
File: I:\2024-8-9_RK3568开发板\..\10 RK3568_Audio_Interface.SchDoc		Drawn By:


MODE>1.2V,PWM
MODE<0.4V,PFM
Default 0.92V,
Adjustable Range(Theory)
0.7V-1.25V
VCC3V3_SYS
VCC3V3_PMU
VDD_CPU
VDD_CPU_COM
VDD_CPU_EXT
OUT
FB
VDD
RK3568
BUCK4
Default down
30Kohm
CPU_AVS/CPU_DVS_PWM0_M0
PMIC RK809 DCDC
VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
Feedback from RK3568
VDD
Pin
OUT
FB
RK3568
BUCK1/BUCK2
DDR4 1.21V 62K 1%
LPDDR4/4x 1.11V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.25V 68K 1%
PMIC RK809 LDO
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_3V3
VCC_1V8
LDO1 400mA
LDO2 400mA
LDO3 100mA
LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V-3.6V 2.5A
RK809-5
HPL_OUT
HP_SNS
HPR_OUT
SPKN_OUT
SPKP_OUT
MIC1_INP
MIC1_INN
PMIC RK809 Managerment
VDC
EXT_EN
PWRON
PWRON_KEY
RESET_KEY
RK809_CLK32KOUT
VCC3V3_PMU
I2C0_SDA_PMIC
I2C0_SCL_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RESETn
X1A0001210005/32.768KHz
Gas Gauge
1.2V
PMIC RK809 CODEC
FB1300 120R-100MHz
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
SPKN_OUT
SPKP_OUT
MIC1_INP
MIC1_INN