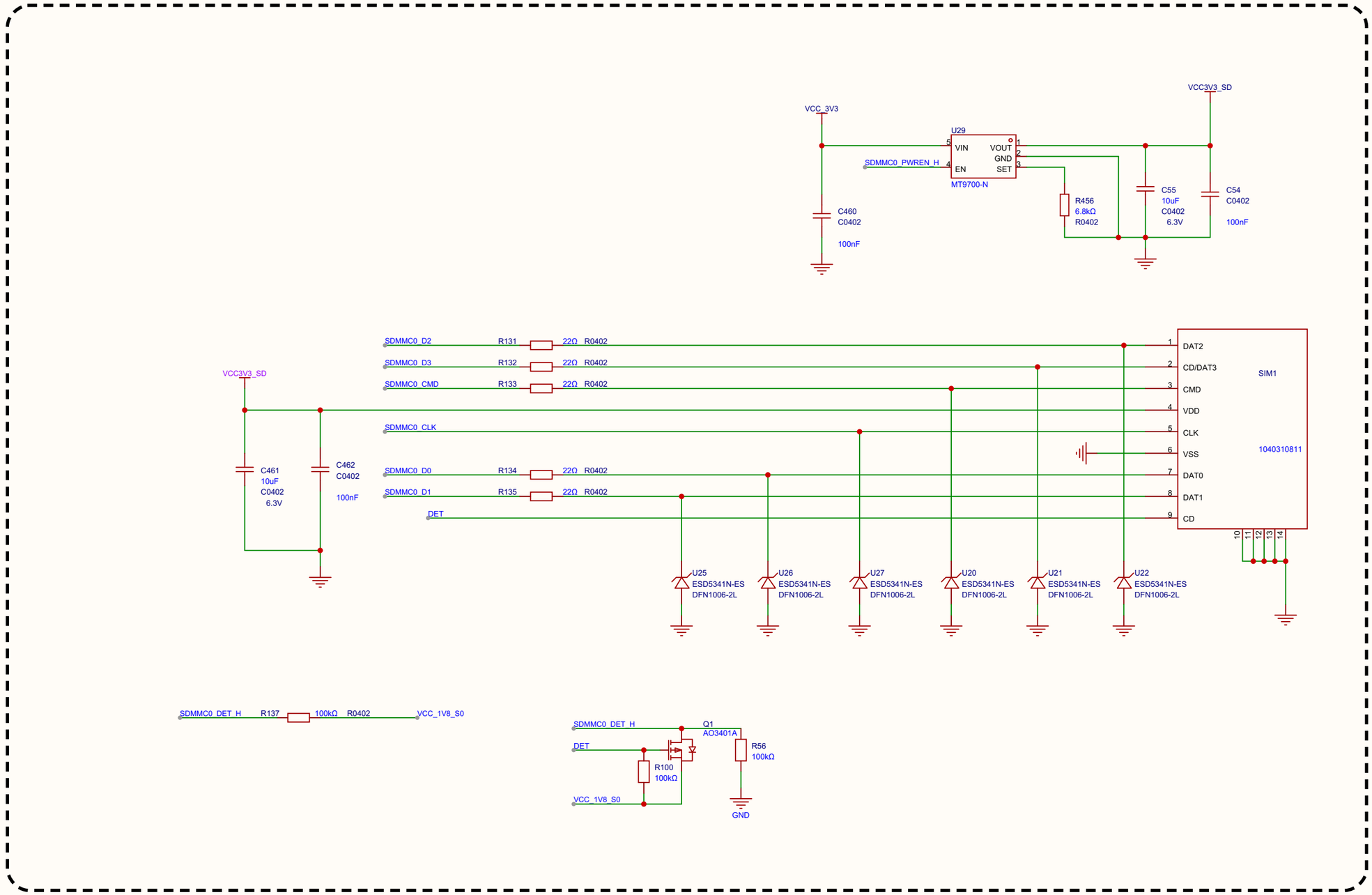
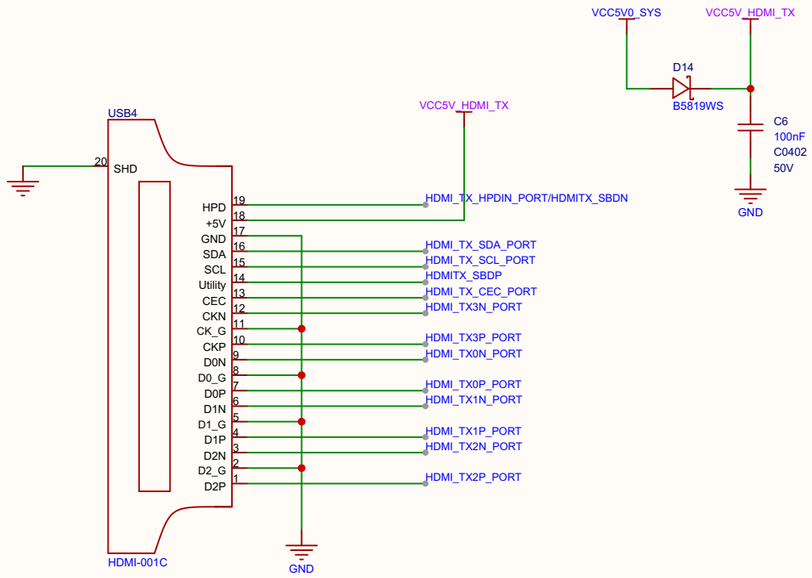


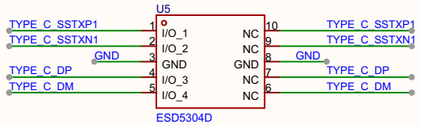
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		更新日期	2026-10-31
板子	A1-CM5-Base-V1.2	图页	TF
绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	尺寸	页 1 共 14
嘉立创EDA		V1.0	A4	嘉立创EDA

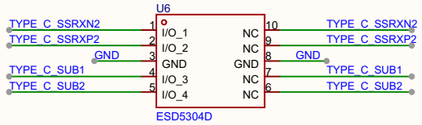
Support video output up to 4Kx2K@120Hz

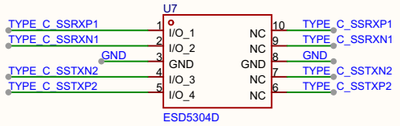


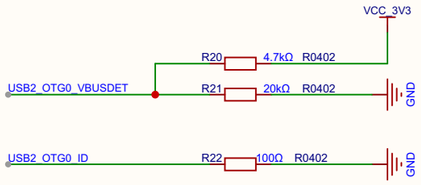
With Displayport Alternate Mode

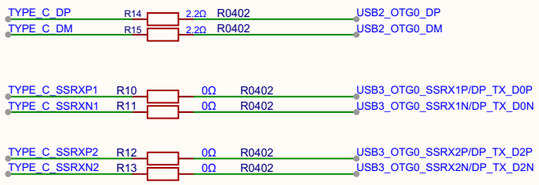
This is also the firmware download interface

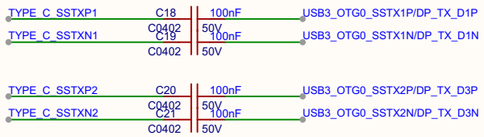


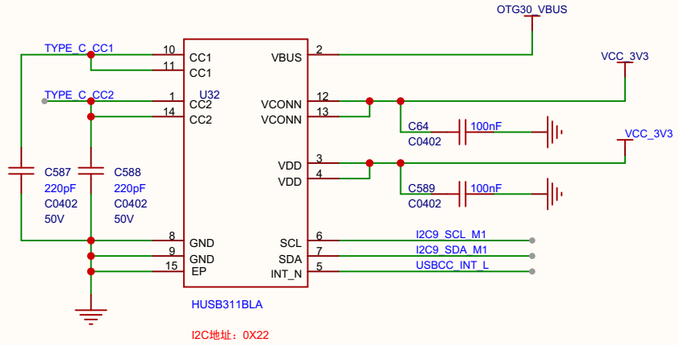


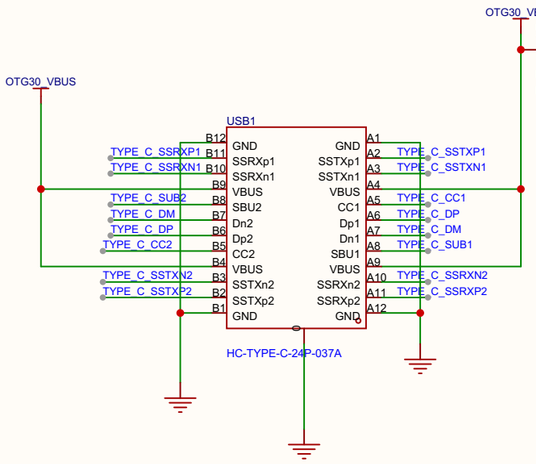


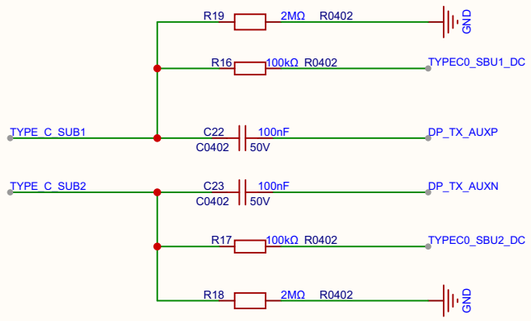


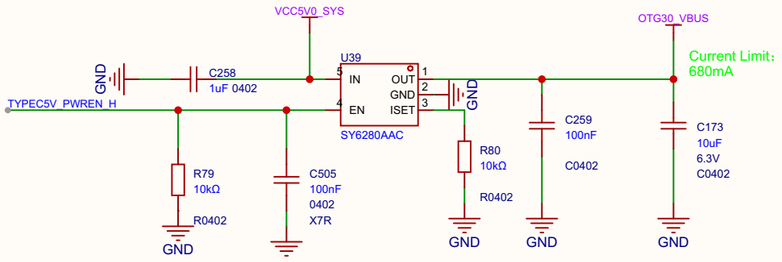


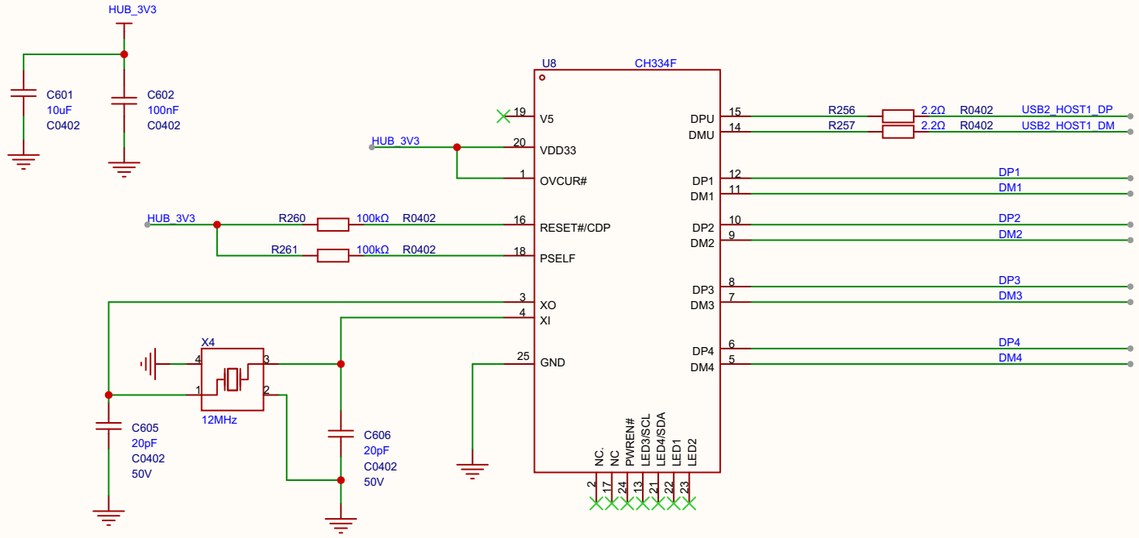


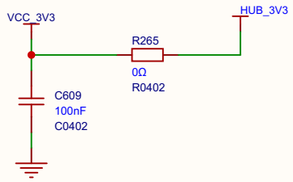


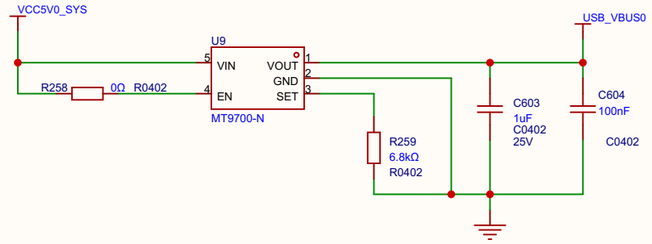


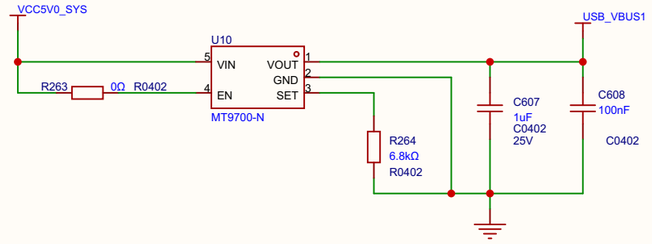


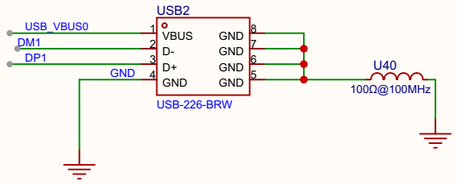


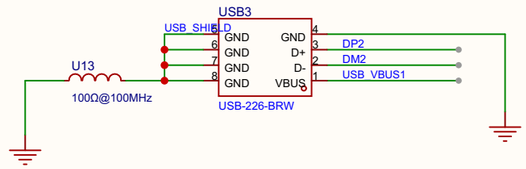

HUB_3V3
C601
10uF
C0402
C602
100nF
C0402
U8
CH334F
19
V5
20
VDD33
1
OVCUR#
16
RESET#/CDP
18
PSELF
3
XO
4
XI
25
GND
DPU
DMU
DP1
DM1
DP2
DM2
DP3
DM3
DP4
DM4
15
14
12
11
10
9
8
7
6
5
R256
R257
2.2Ω
R0402
USB2_HOST1_DP
USB2_HOST1_DM
DP1
DM1
DP2
DM2
DP3
DM3
DP4
DM4
R260
R261
100kΩ
R0402
X4
12MHz
C605
20pF
C0402
50V
C606
20pF
C0402
50V
NC.
NC
PWREN#
LED3/SCL
LED4/SDA
LED1
LED2
2
17
24
13
21
22
23


VCC_3V3
R265
0Ω
R0402
HUB_3V3
C609
100nF
C0402


VCC5V0_SYS
U9
VIN
EN
VOUT
GND
SET
MT9700-N
R258
0Ω
R0402
R259
6.8kΩ
R0402
C603
1uF
C0402
25V
C604
100nF
C0402
USB_VBUS0


VCC5V0_SYS
U10
VIN
EN
VOUT
GND
SET
MT9700-N
R263
0Ω
R0402
R264
6.8kΩ
R0402
C607
1uF
C0402
25V
C608
100nF
C0402
USB_VBUS1

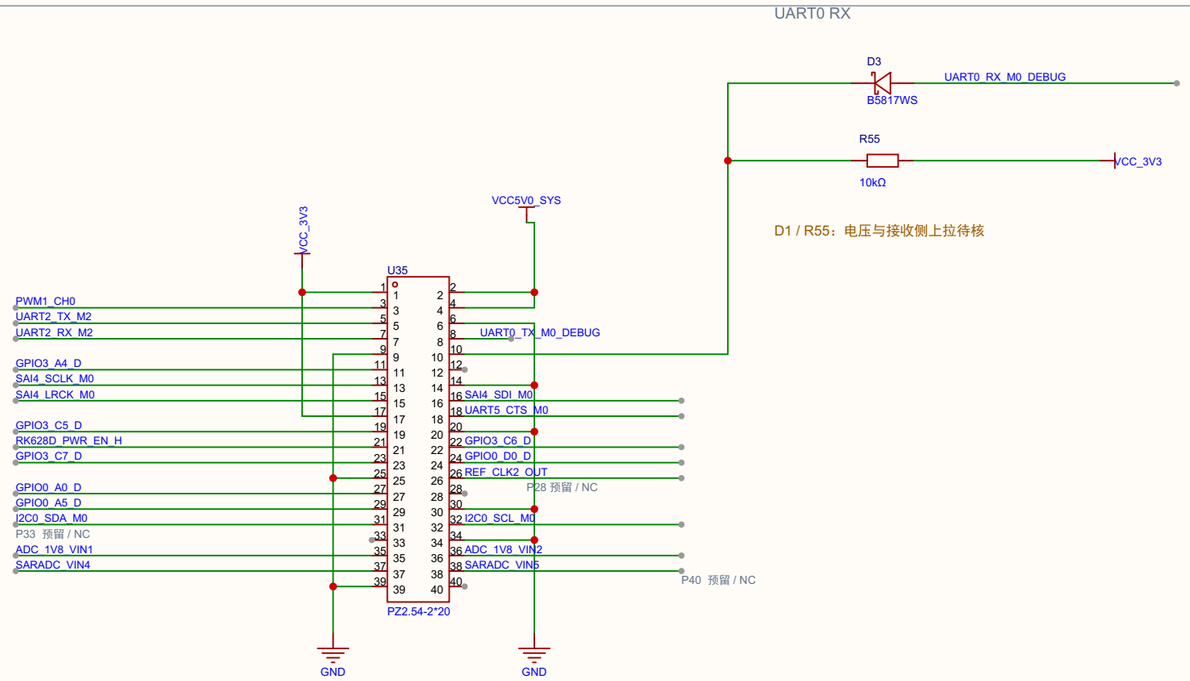

USB_VBUS0
DM1
DP1
GND
USB2
VBUS
D-
D+
GND
GND
GND
GND
GND
USB-226-BRW
U40
100Ω@100MHz


USB3
USB_SHELL
GND
GND
GND
GND
GND
D+
D-
VBUS
USB-226-BRW
U13
100Ω@100MHz
DP2
DM2
USB_VBUS1

40PIN GPIO / 自定义扩展接口

board-g_1 · A1 耳机检测已占用 GPIO0_A2 · 原生电压接口 / 非树莓派 HAT 定义

01 排针与调试串口



电源：P1/P17 = 3.3V；P2/P4 = 5V。所有 GND 保持原连接。

02 电压与接口说明

1.8V IO：P27 / P29（原图定义）

ADC：P35 / P36 为 ADC_1V8 输入

P37 / P38 为 SARADC，输入量程待核

其余信号的 IO 电压需核对核心板资料

不能因为排针有 3.3V 电源就默认全为 3.3V

I2C0：P31 = SDA；P32 = SCL

确认核心板已有上拉及其电压

SAI4：P12 MCLK / P13 SCLK

P15 LRCK / P16 SDI；不代表双向音频

UART5：P18 仅 CTS，不构成完整串口

P28 / P33 / P40：预留，不连接

引出前仍需核对核心板内部用途和复用

GPIO0_A2 → 耳机检测专用；P28 不再引出

03 固定触摸 / 显示资源

TP_INT：GPIO3_D0 → R48 → CN5.3

TP_RST：GPIO0_C1 → R45 → CN5.2

I2C9：CN5.4 / CN5.5，与 HUSB311 共用总线

LCD_RESET 与 PWM0_CH0_M0 保持屏接口原连接

以上资源不分配给 40Pin 外设；触摸信号保持固定

04 复用限制

SPI1_M2：P19 MISO / P22 MOSI / P23 CLK

硬件 CS0 = GPIO3_D0，与 TP_INT 冲突，禁止占用

硬件 CS1 与 CAM_CLK1_OUT_M0 复用；需要时另选 GPIO CS

CAN0_M2：P13 TX / P15 RX，与 SAI4 时钟二选一

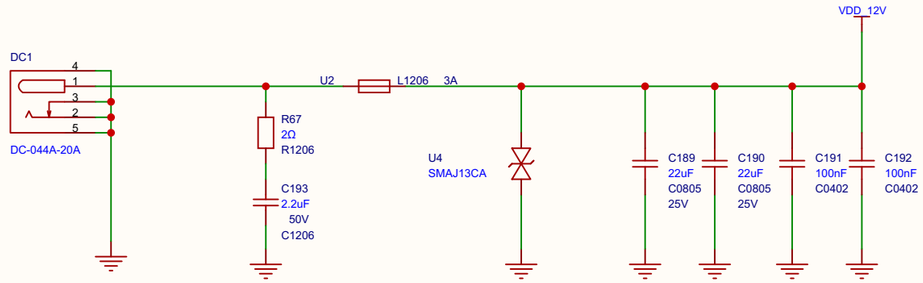
使用软件片选前，核对 GPIO、SPI 和外设的电压

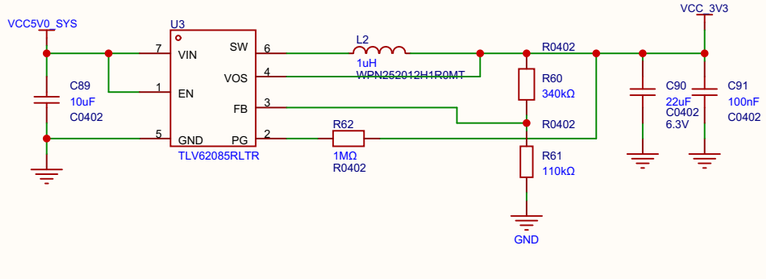
05 保留策略与原图备忘

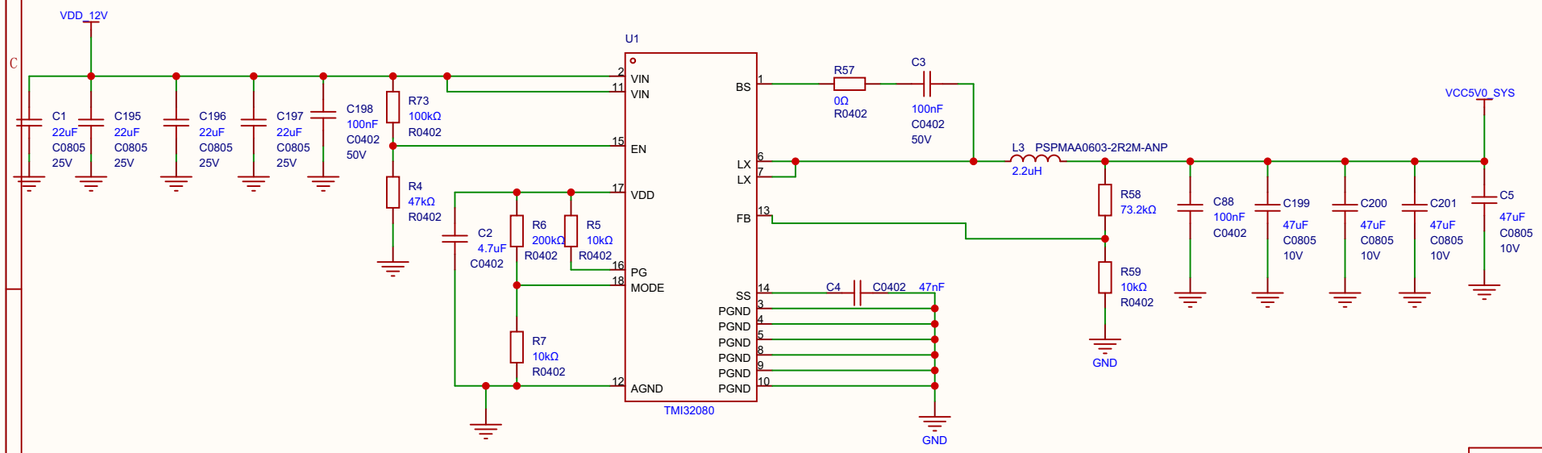
R37 不接排针；三路 CSI PWDN 不接。CSI 数据、I²C、MCLK 留在摄像头接口。

原图待核资源：I2C1 / RK806、HW_ID / HP_HOOK、PWM1_CH0_M3、PWM2_CH6_M3。仅作备忘，不新增连接。

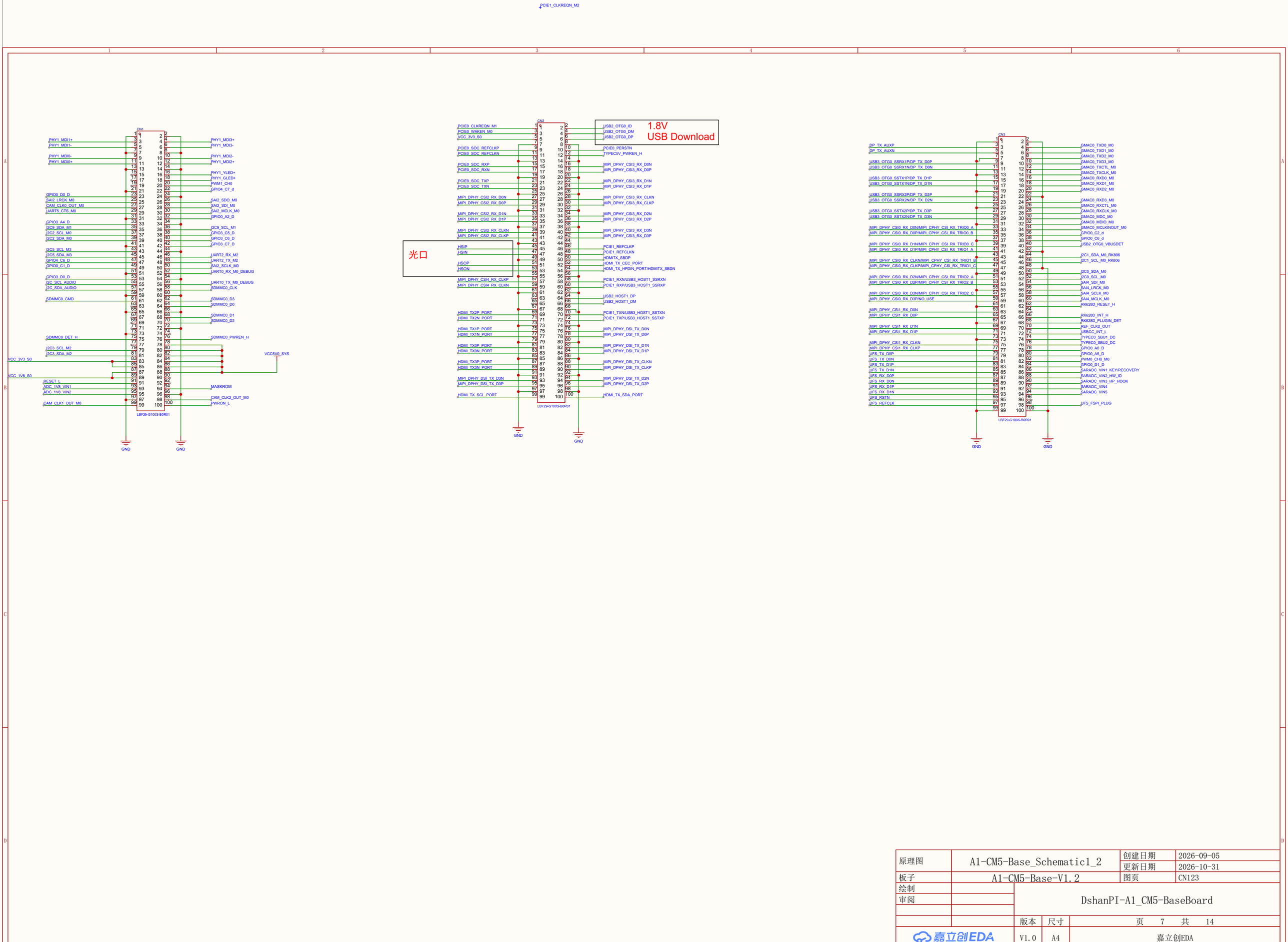
本页只整理布局；MIPI DSI 触摸、PCB 布线和固件配置均未改变。



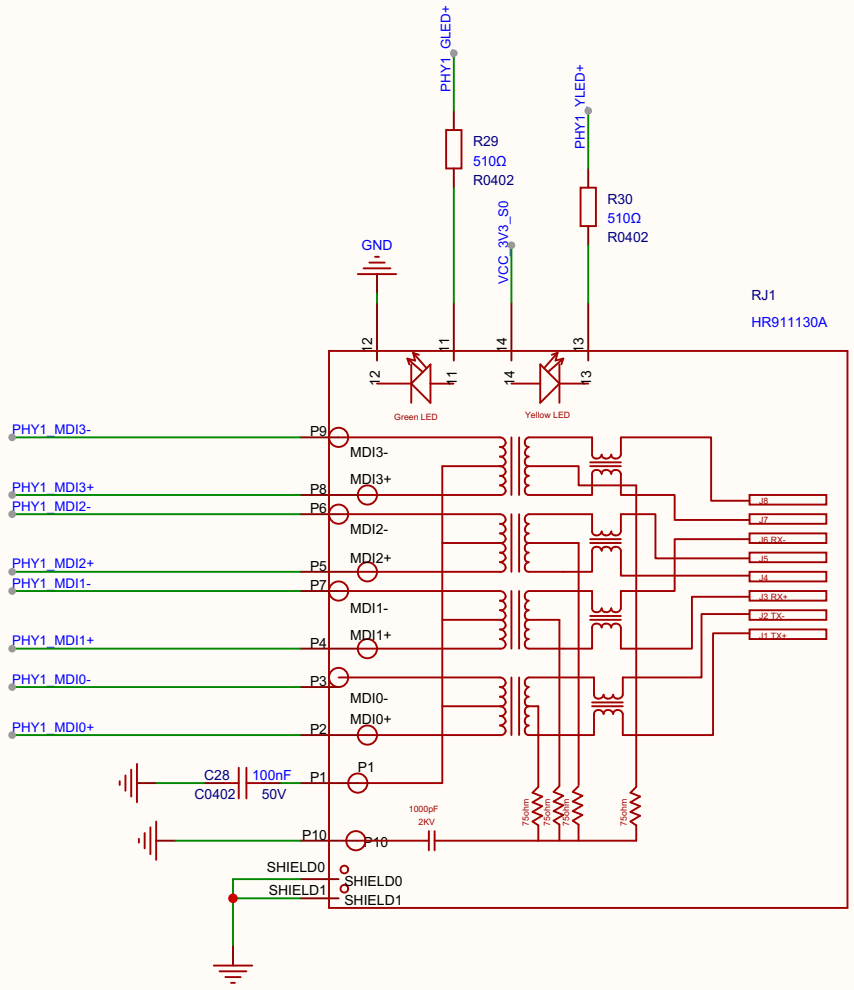




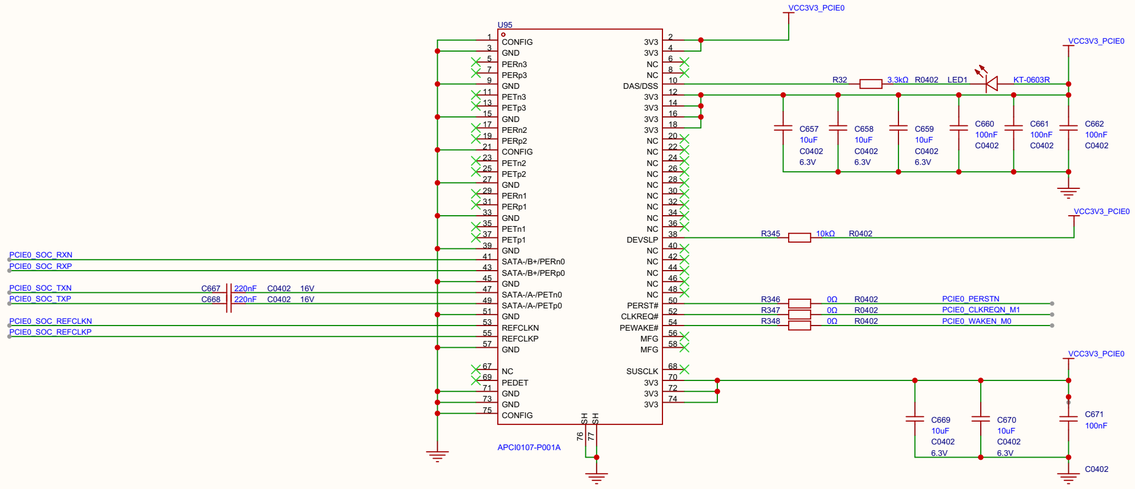
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绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本 / 尺寸	页 6 共 14
嘉立创EDA		V1.0 / A4	嘉立创EDA

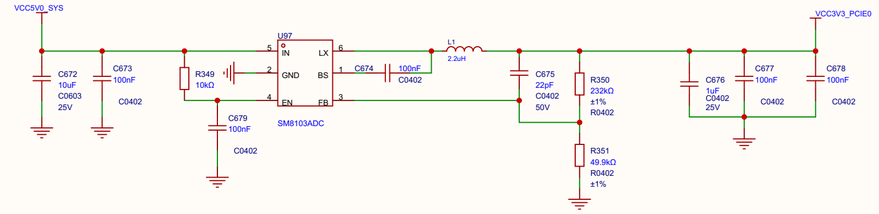


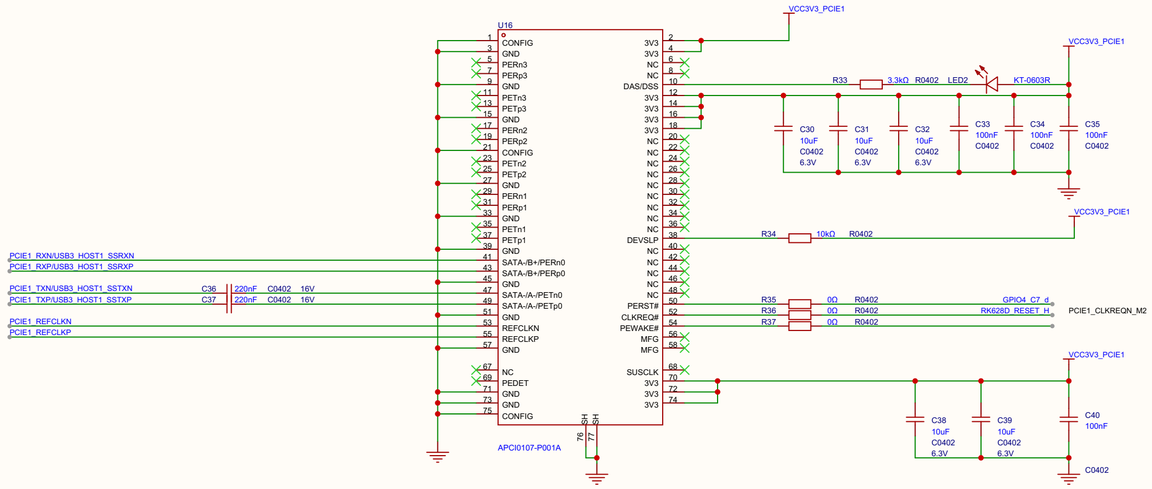
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绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	尺寸	页 7 共 14
嘉立创EDA		V1.0	A4	嘉立创EDA

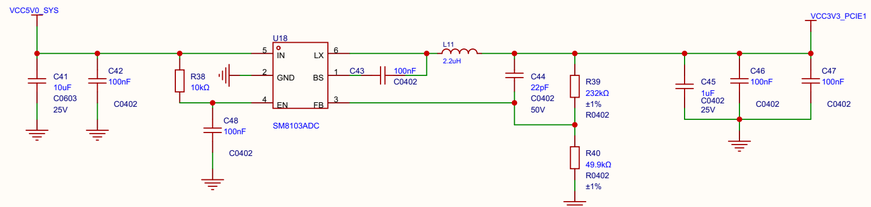


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板子	A1-CM5-Base-V1.2	图页	RGMC1
绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	尺寸	页 8 共 14
嘉立创EDA		V1.0	A4	嘉立创EDA

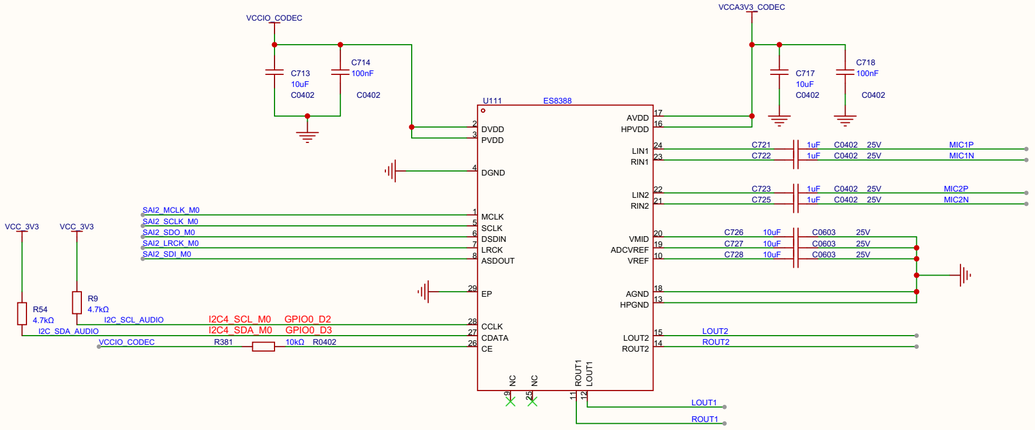


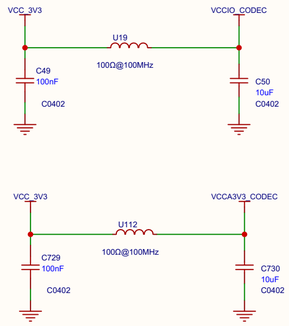




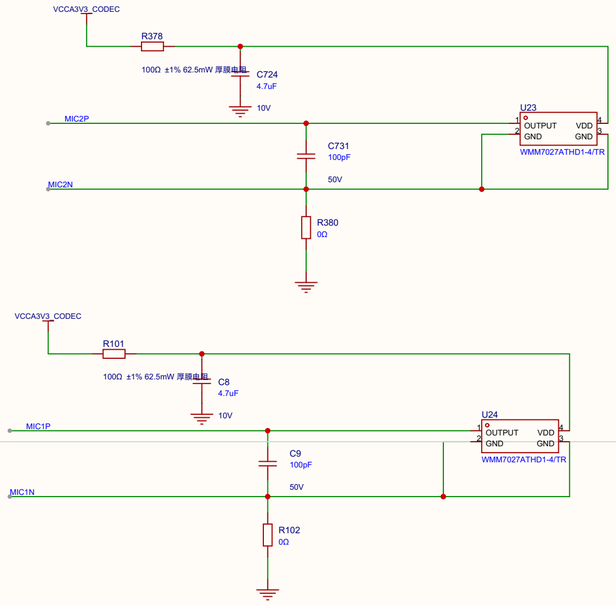


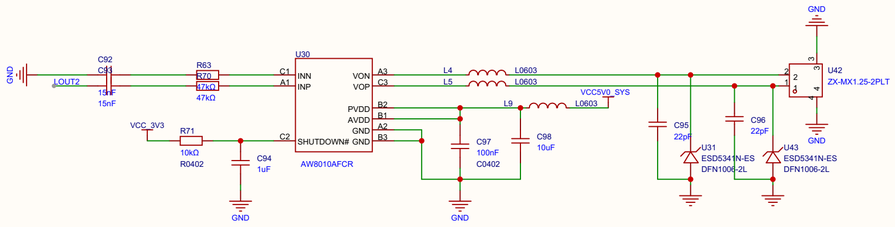
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板子	A1-CM5-Base-V1.2	更新日期	2026-10-31
绘制		图页	m.2 KEY
审阅		DshanPI-A1_CM5-BaseBoard	
		版本	尺寸
嘉立创EDA		V1.0	A4
		页 9 共 14	
		嘉立创EDA	

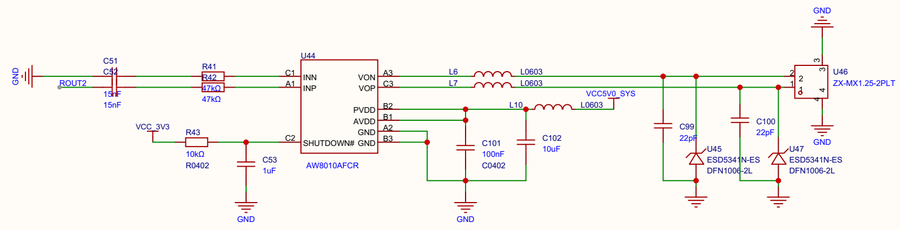




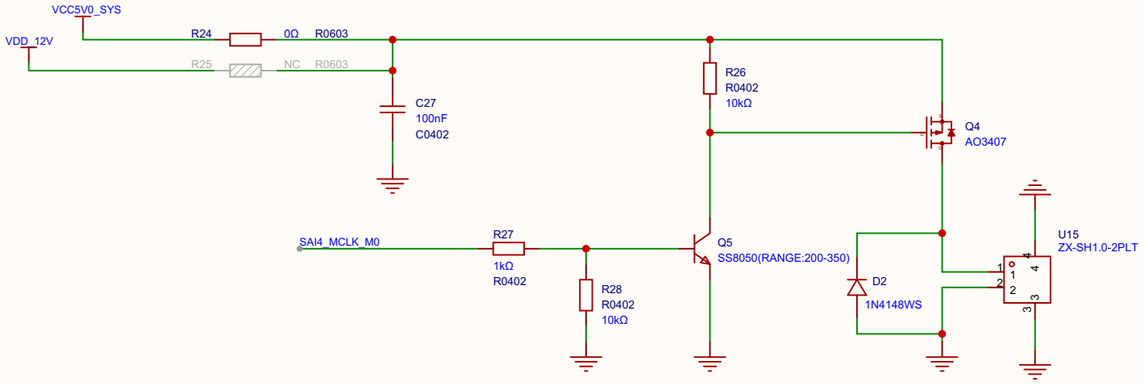
Analog MIC

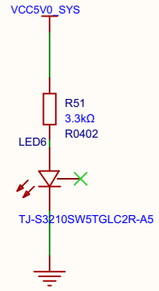




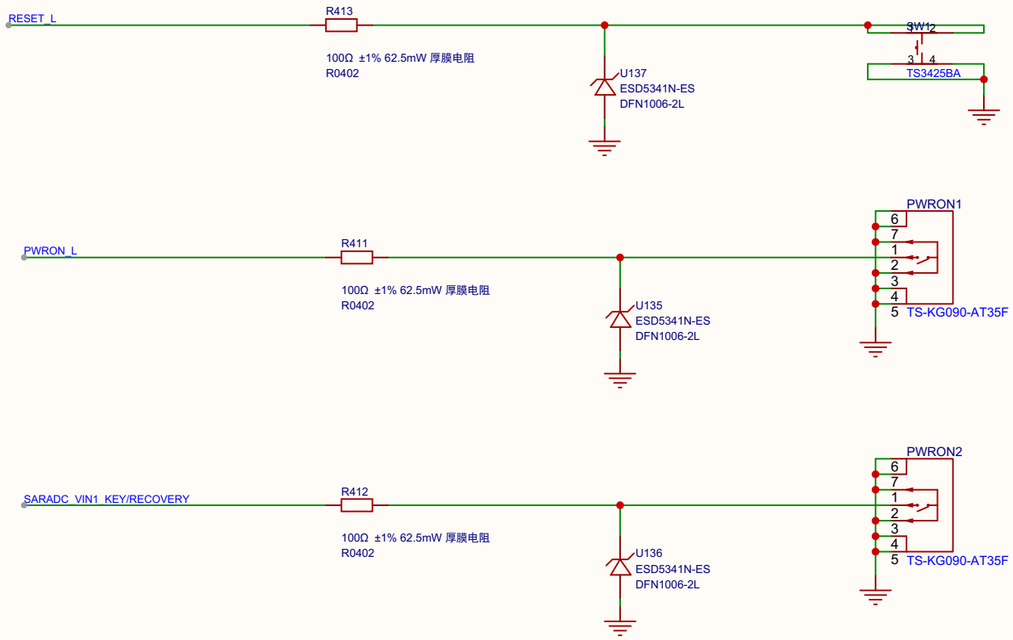


原理图	A1-CM5-Base_Schematic1_2	创建日期	2026-09-05
		更新日期	2026-10-31
板子	A1-CM5-Base-V1.2	图页	ES8388
绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	V1.0
		尺寸	A4
		页 10 共 14	
嘉立创EDA		嘉立创EDA	

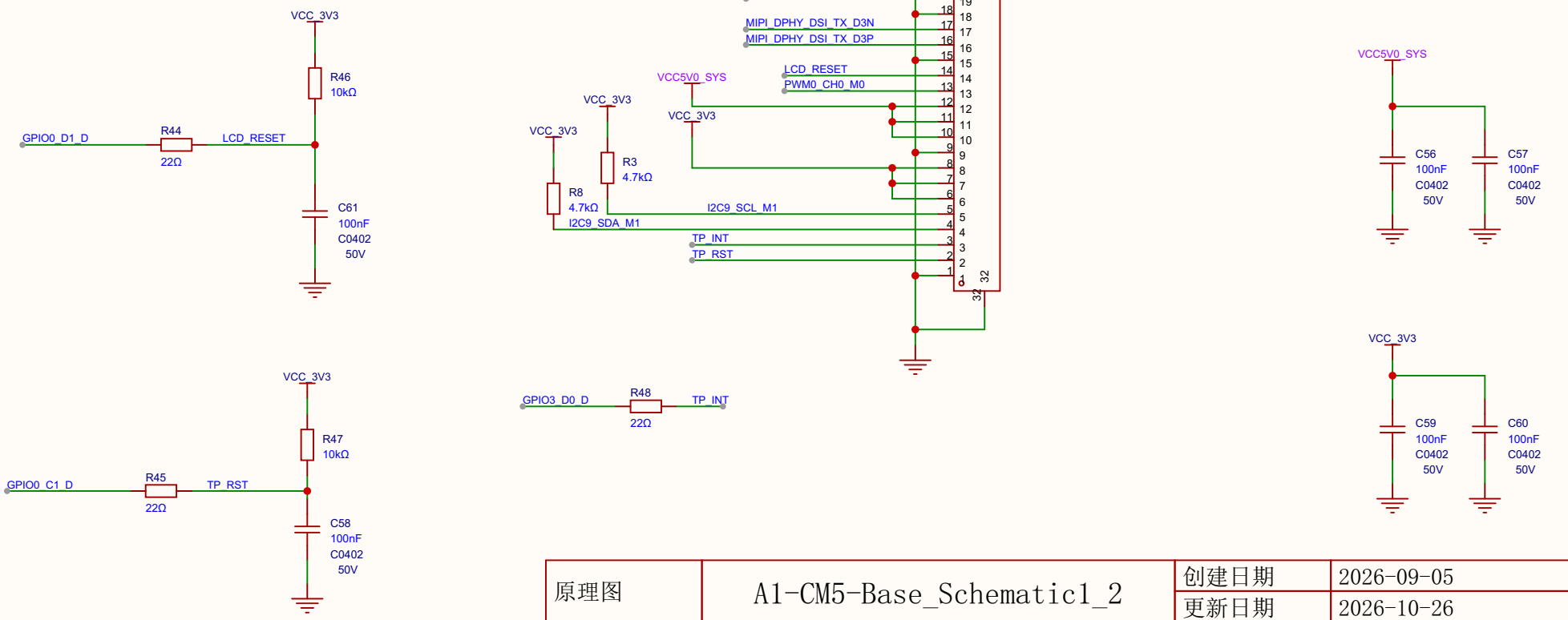




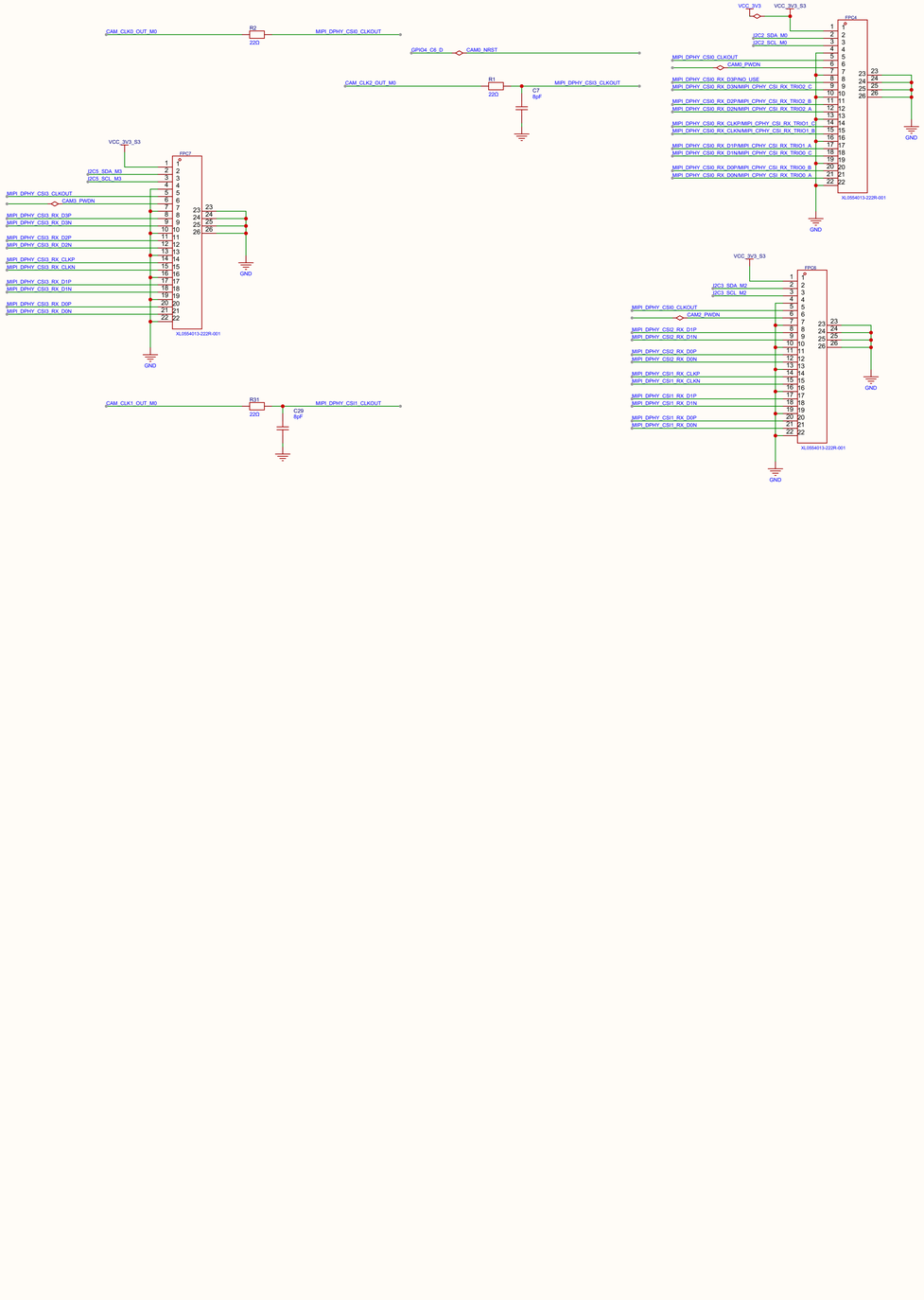




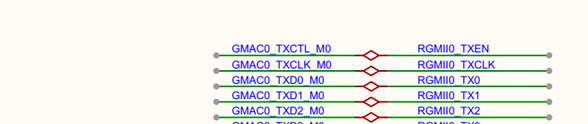
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		更新日期	2026-10-31
板子	A1-CM5-Base-V1.2	图页	KEY & RTC
绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	尺寸	页 11 共 14
嘉立创EDA		V1.0	A4	嘉立创EDA



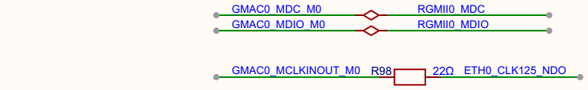
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板子	A1-CM5-Base-V1.2	图页	mipi dsi
绘制		DshanPI-A1_CM5-BaseBoard	
审阅			
		版本	尺寸	页 12 共 14
嘉立创EDA		V1.0	A4	嘉立创EDA

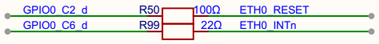


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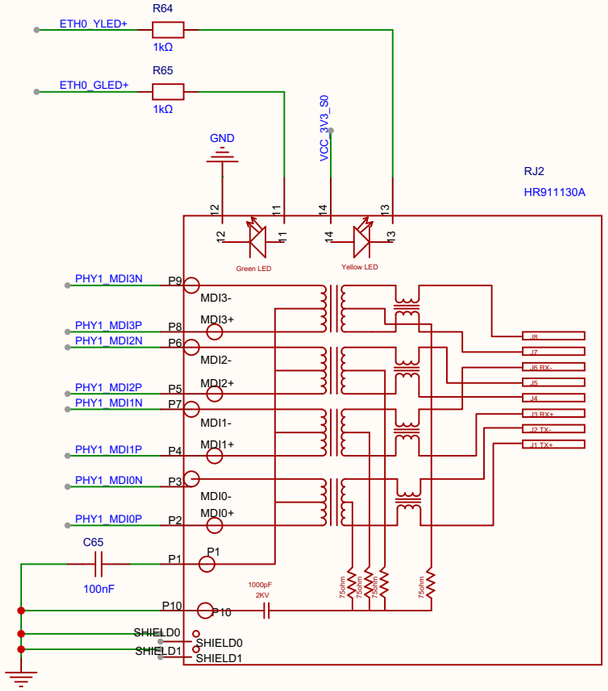


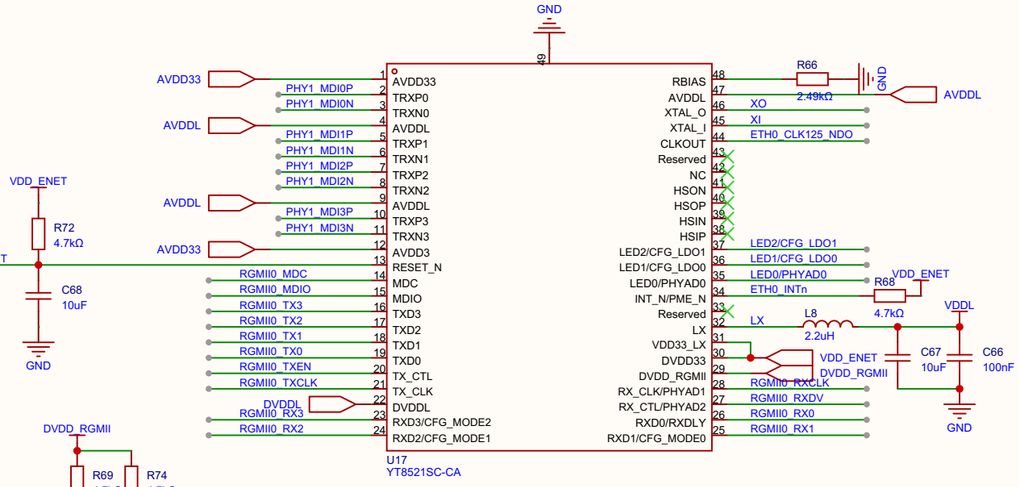


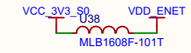


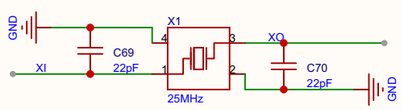


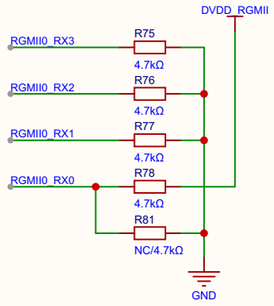


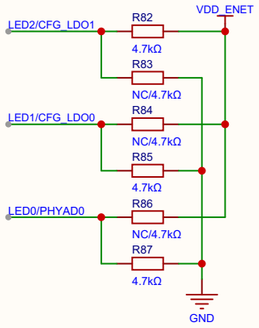


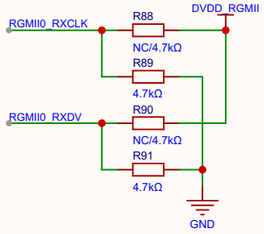


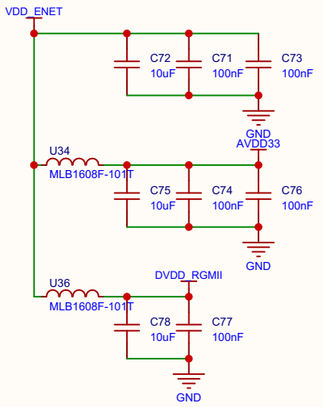


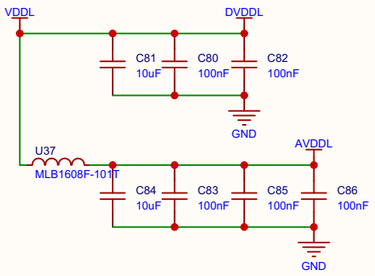












原理图	A1-CM5-Base_Schematic1_2	创建日期	2026-09-05
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绘制		DshanPI-A1_CM5-BaseBoard	
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		版本	尺寸	页 14 共 14
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