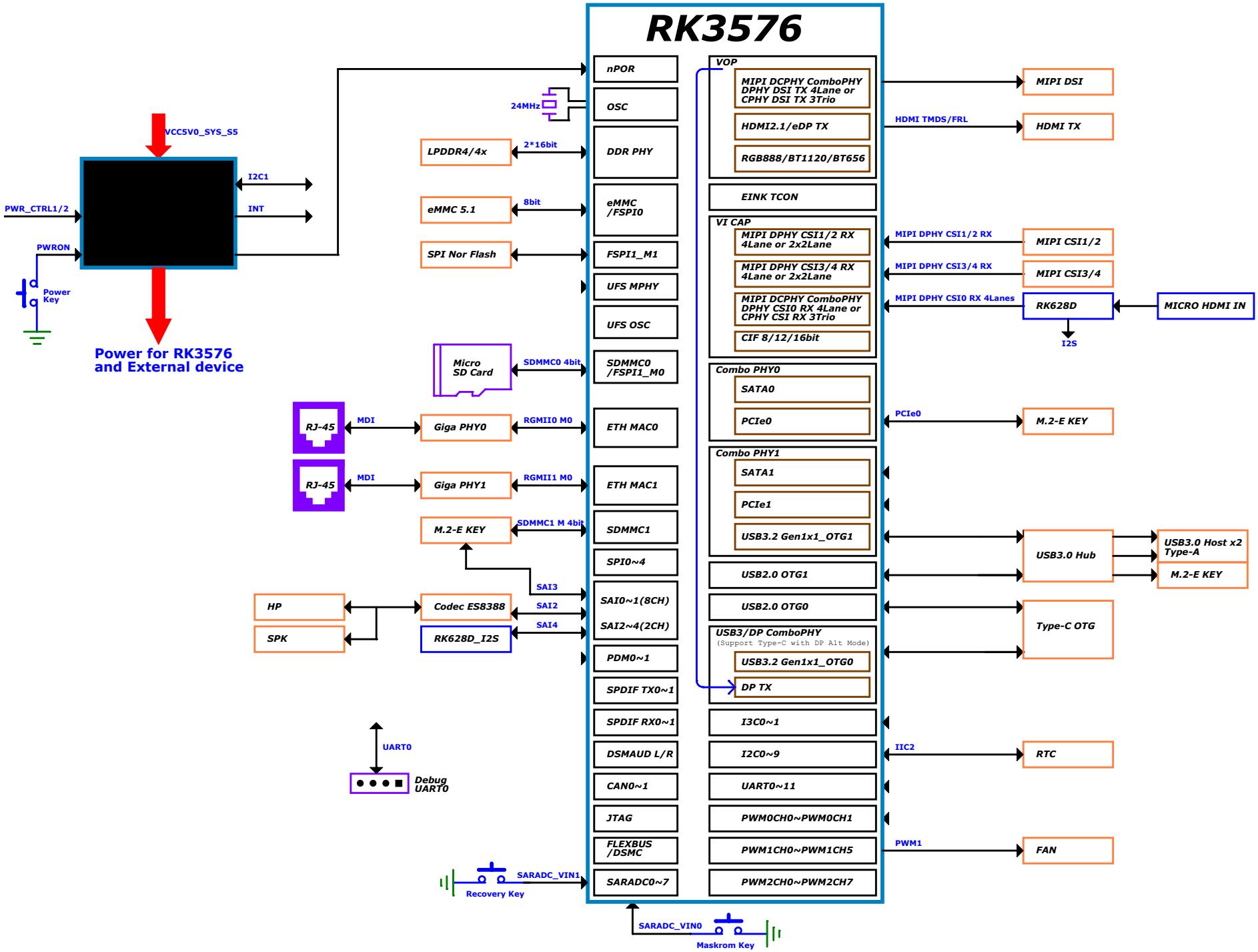
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	*2025-04-25*		*1: Draft version;*	
V1.1	*2025-07-17*			

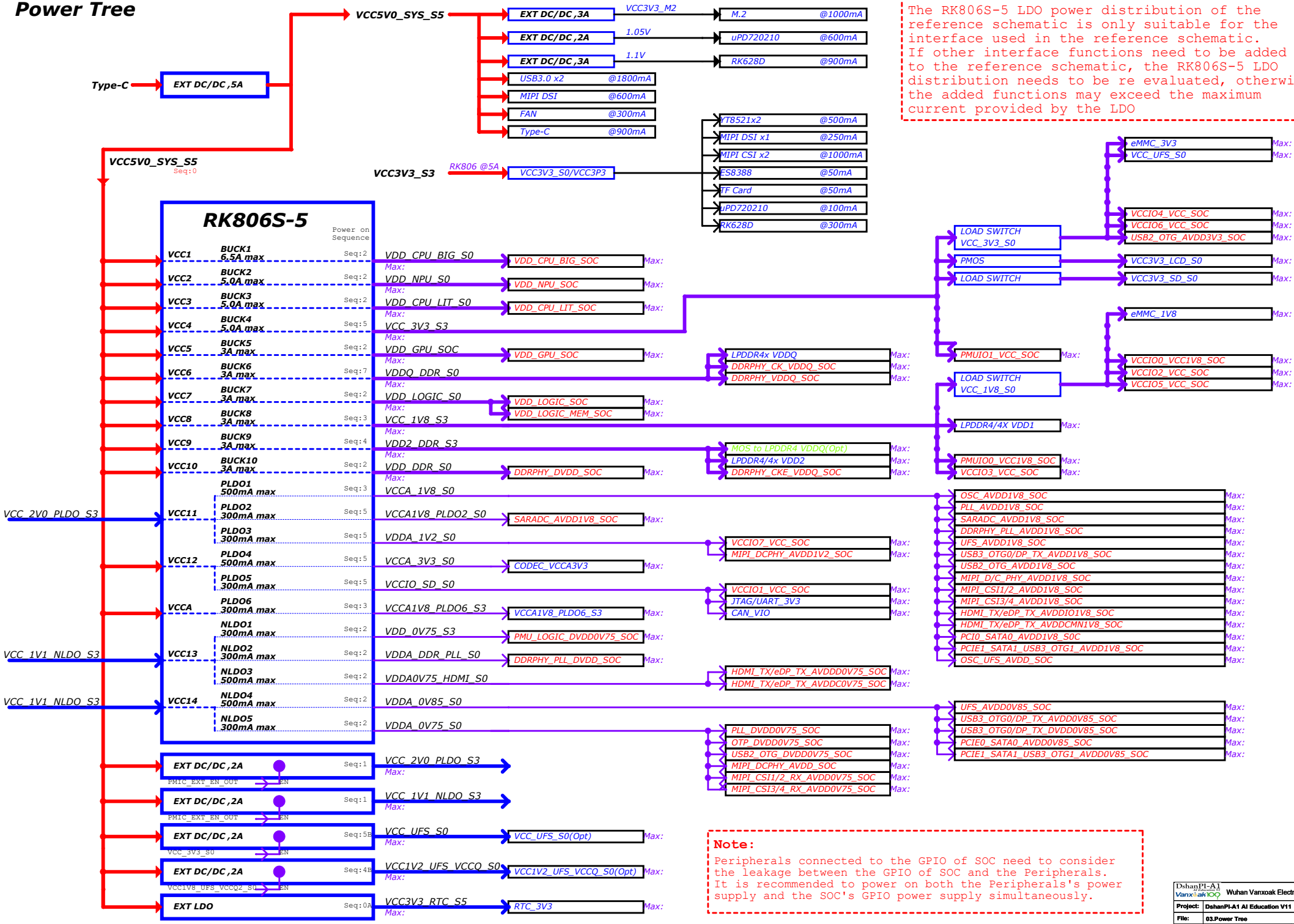
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	01.Revision History				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	1 of 39

RK3576 Ref Block Diagram(Typical Application Case)



Wuhan Vanxoak Electronics Co., Ltd	
Project:	DshanPI-A1 AI Education V11
File:	02.Block Diagram
Date: Friday, September 05, 2025	Rev: V1.1
Designed by: Cao Jun	Reviewed by: <Checker> Sheet: 2 of 39

Power Tree

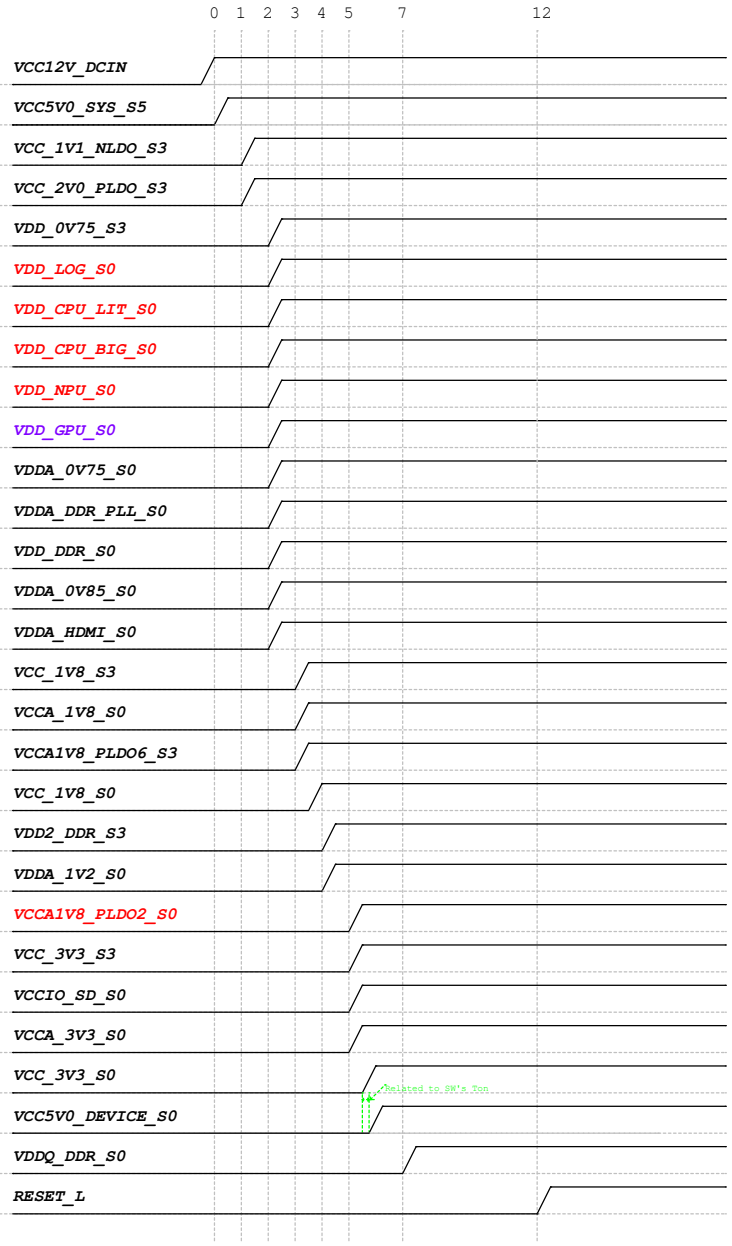


Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Note:
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals.
It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

Wuhan Vanxoak Electronics Co., Ltd	
Project:	DshanPI-A1 AI Education V11
File:	03.Power Tree
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	3 of 39

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

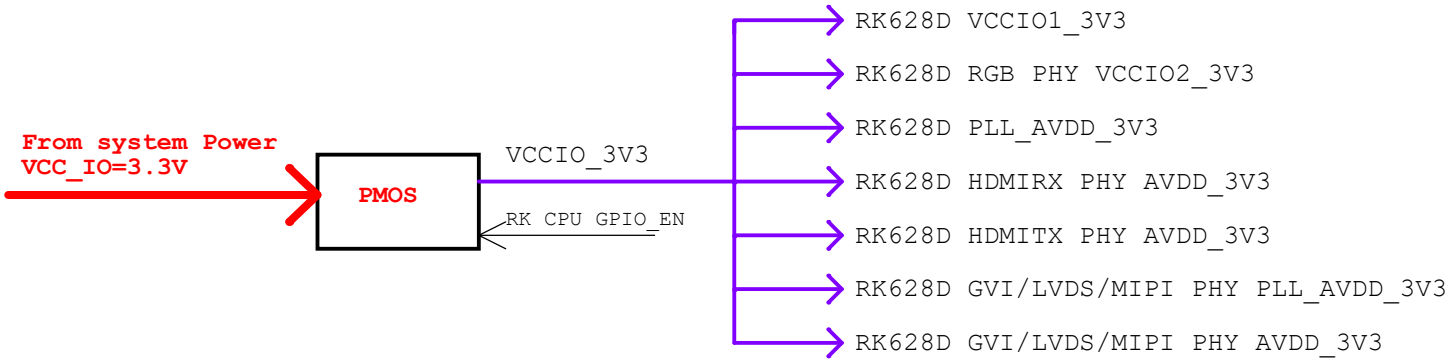
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

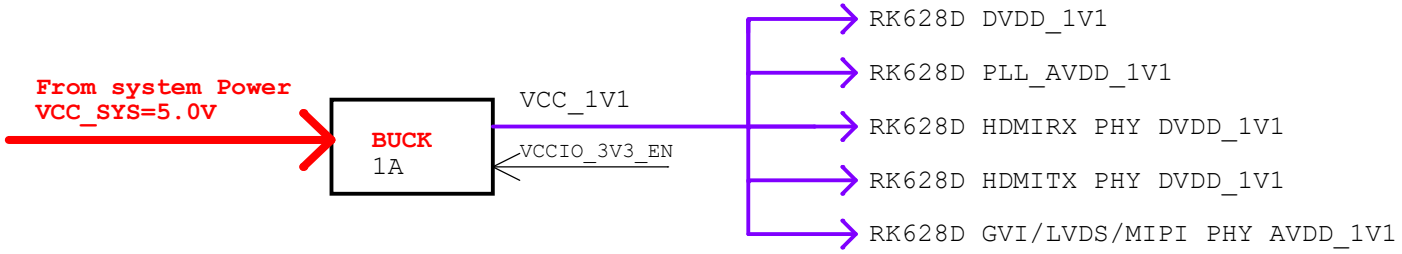
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

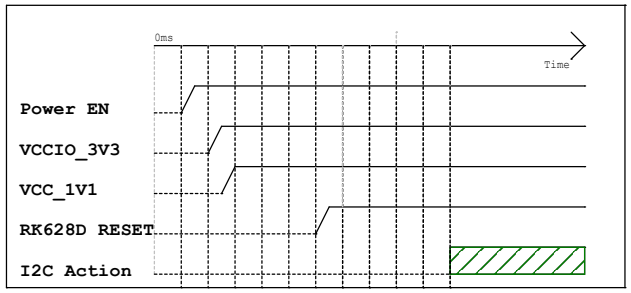
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

DshanPI-A1 AI Education V1 / Vanxoak 100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	04.Power Sequence and Map				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	4 of 39





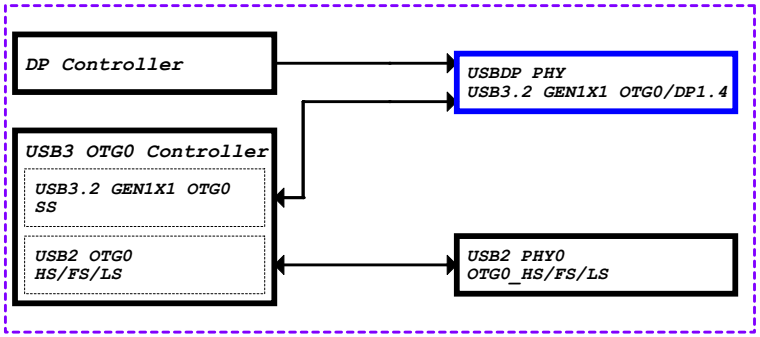
Power-on Sequence:



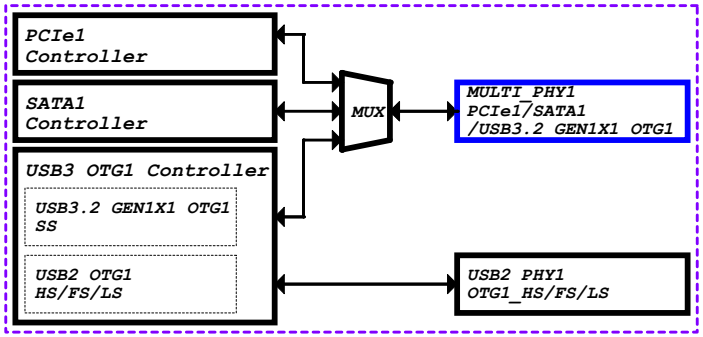
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	05.RK628D Power Diagram				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	5 of 39

MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



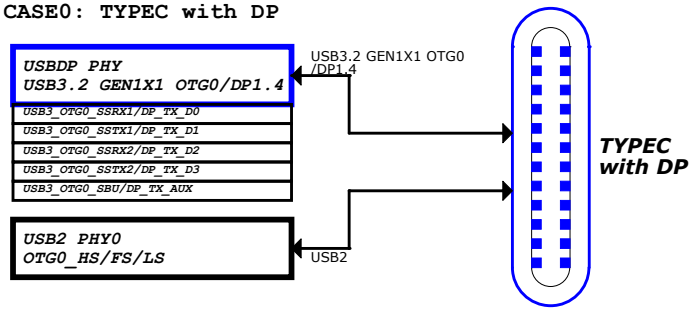
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



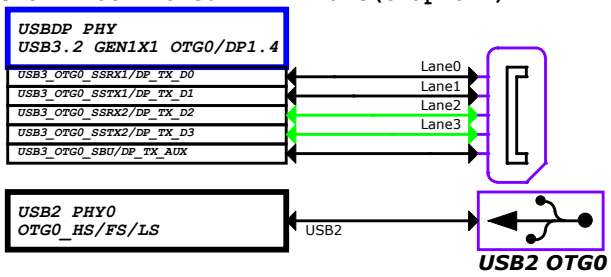
Note:
USB2 OTG1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

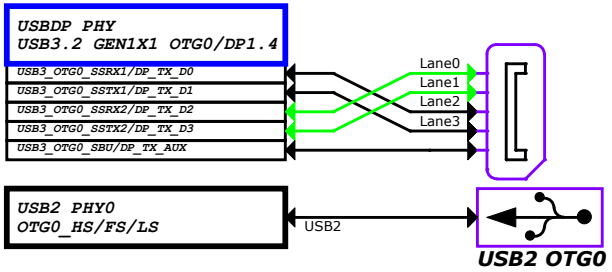
CASE0: TYPEC with DP



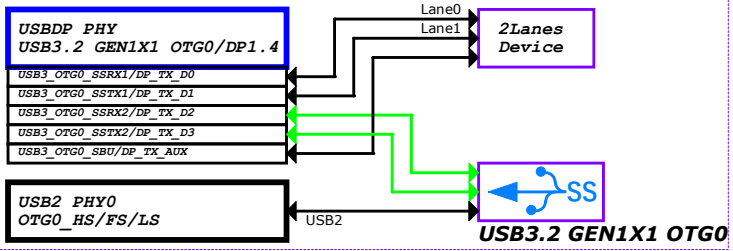
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



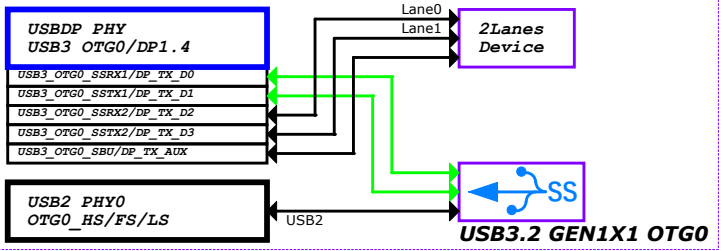
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



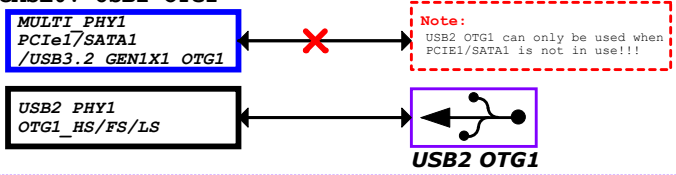
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



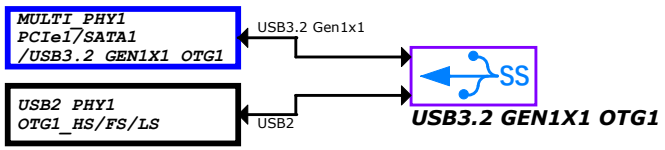
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB OTG1 Application

CASE0: USB2 OTG1

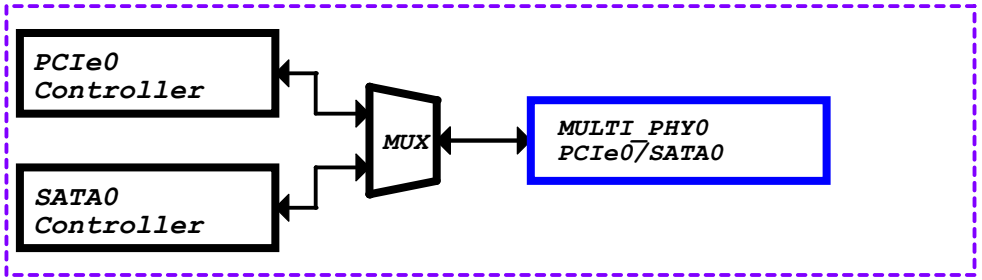


CASE1: USB3.2 GEN1X1 OTG1

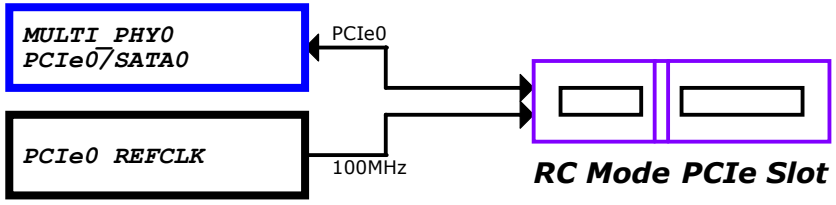


DshanPI-A1	Wuhan Vanxoak Electronics Co., Ltd
Project:	DshanPI-A1 AI Education V11
File:	06.USB/DP Configure Map
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	6 of 39

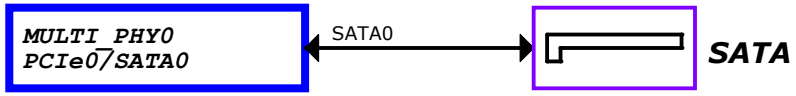
PCIe Combo PHY0--PCIe0/SATA0



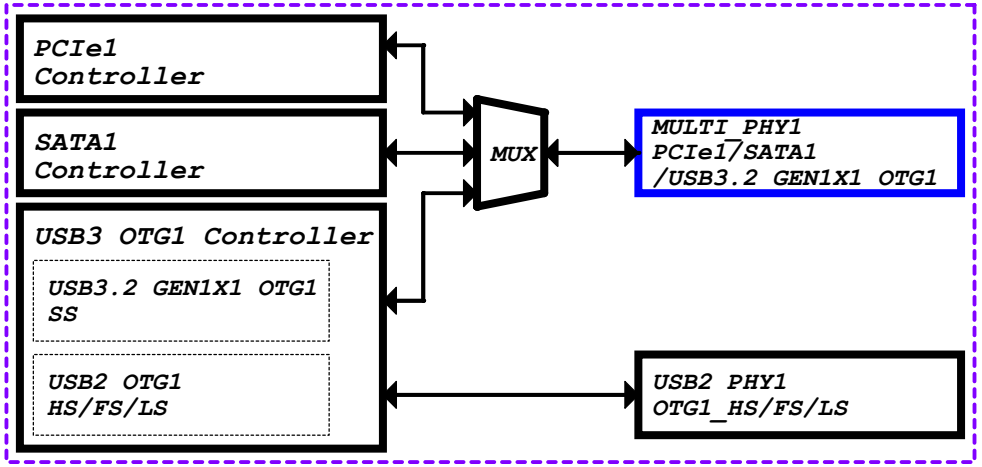
CASE0: PCIe x 1Lane



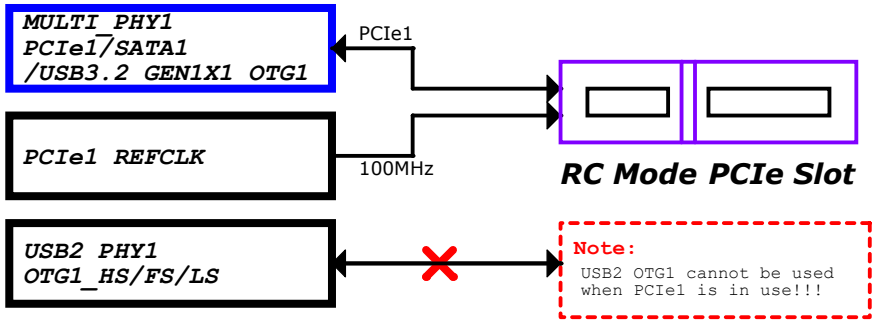
CASE1: SATA



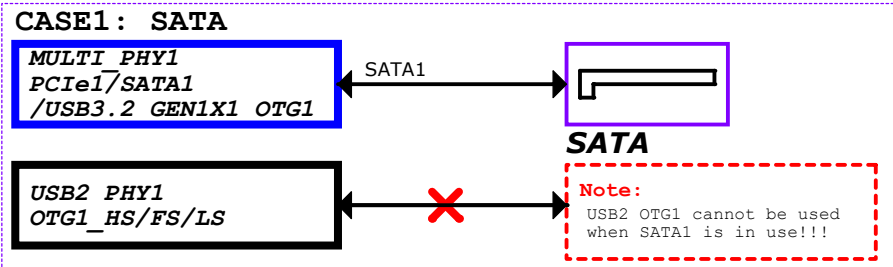
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



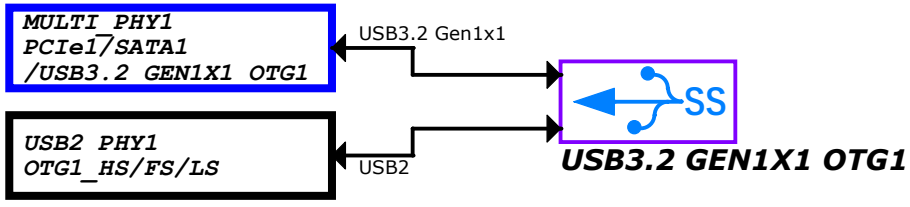
CASE0: PCIe x 1Lane



CASE1: SATA

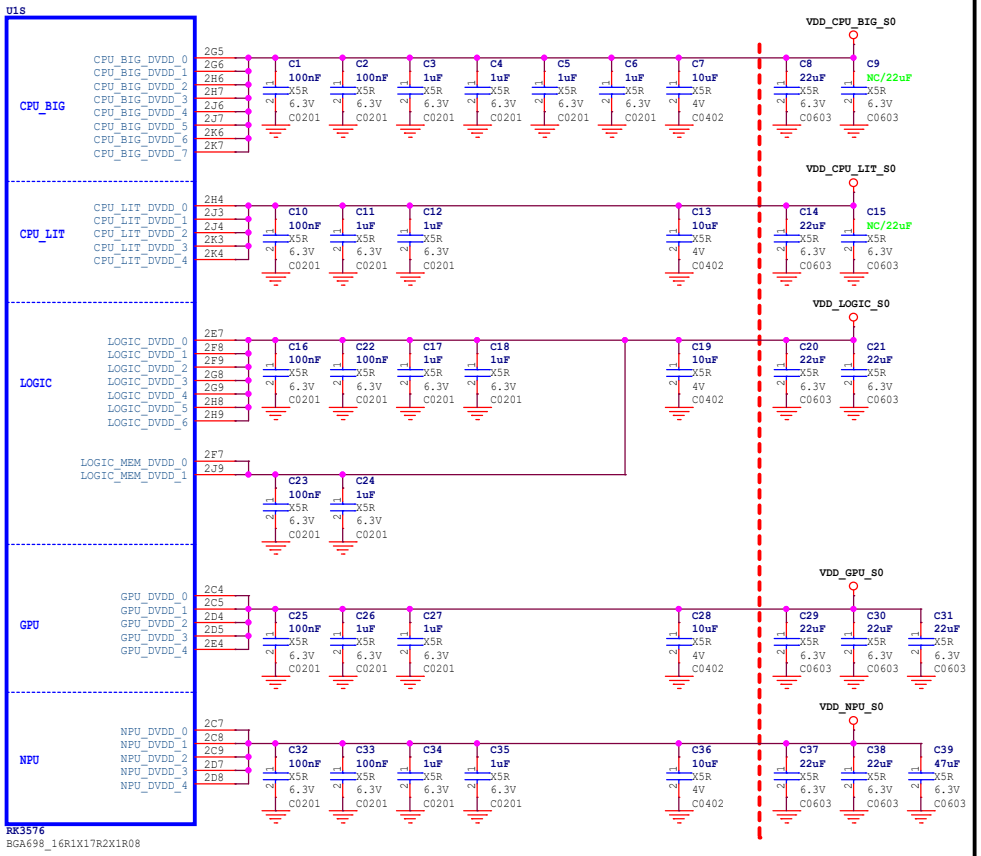


CASE2: USB3.2 GEN1X1 OTG1



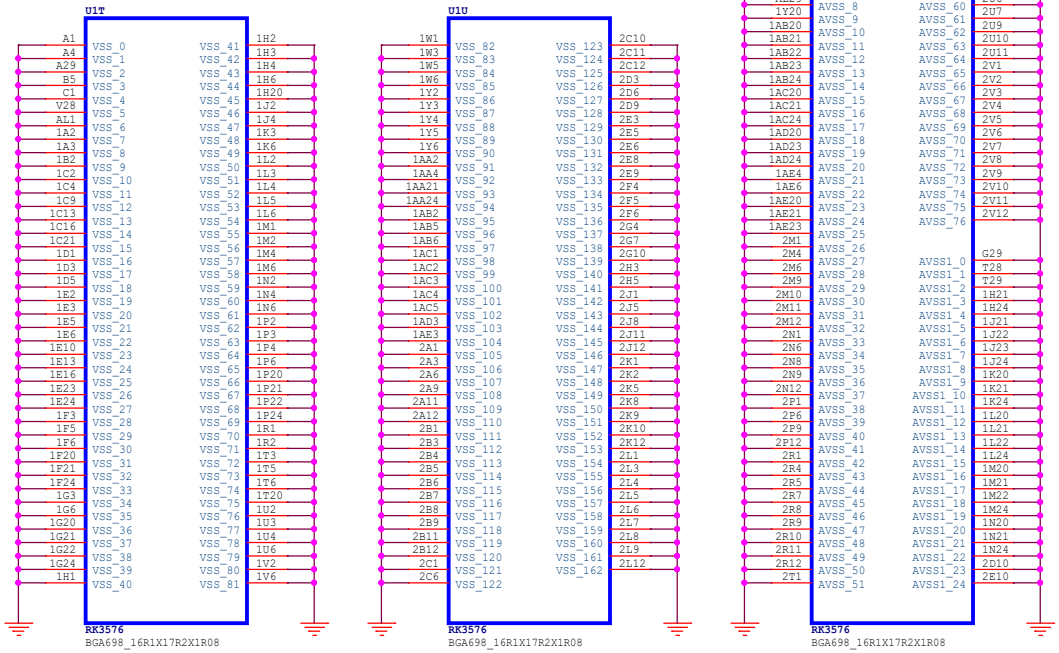
DshanPI-A1 AI Education V1	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	07.PCIe Combo PHY Configure Map				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	7 of 39

RK3576_S (Power)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

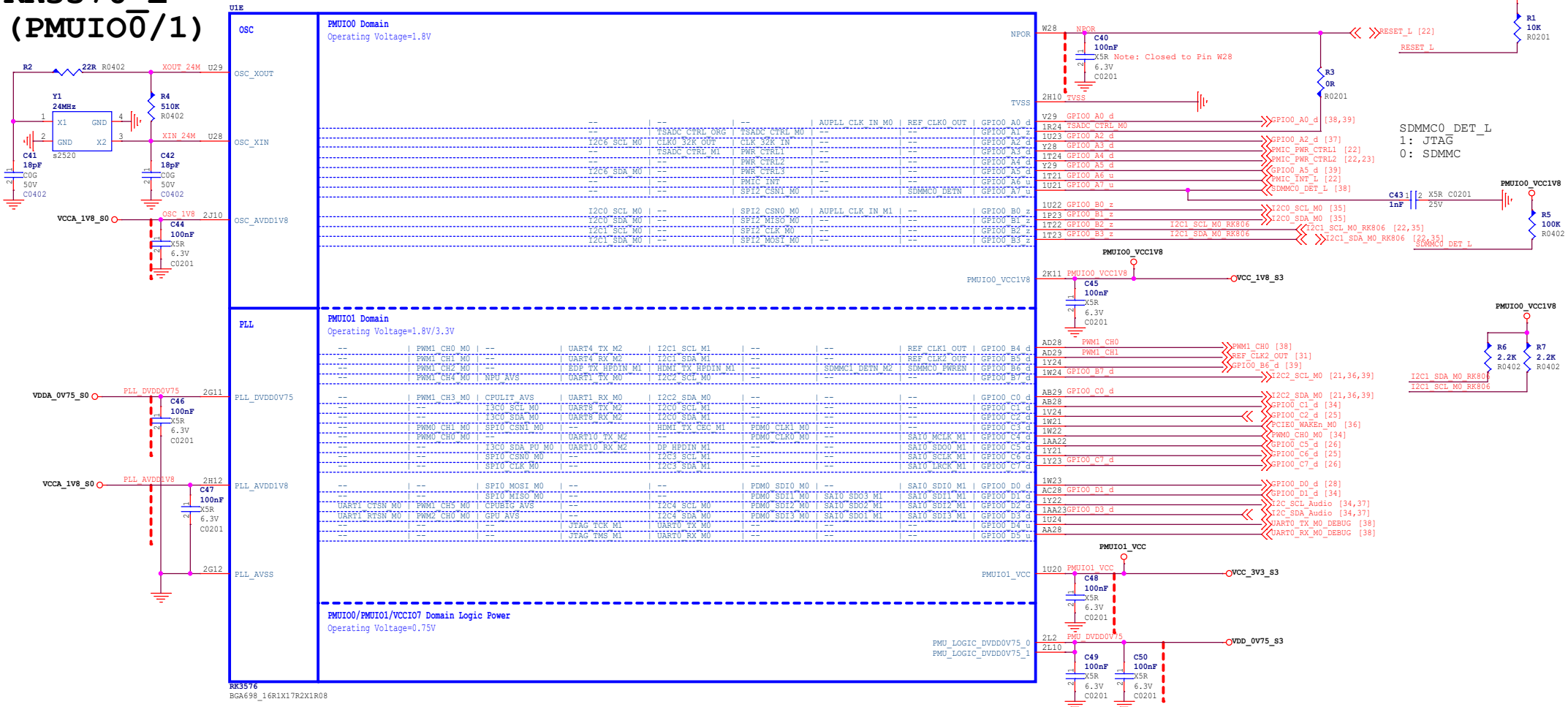
RK3576_T/U/V (GND)



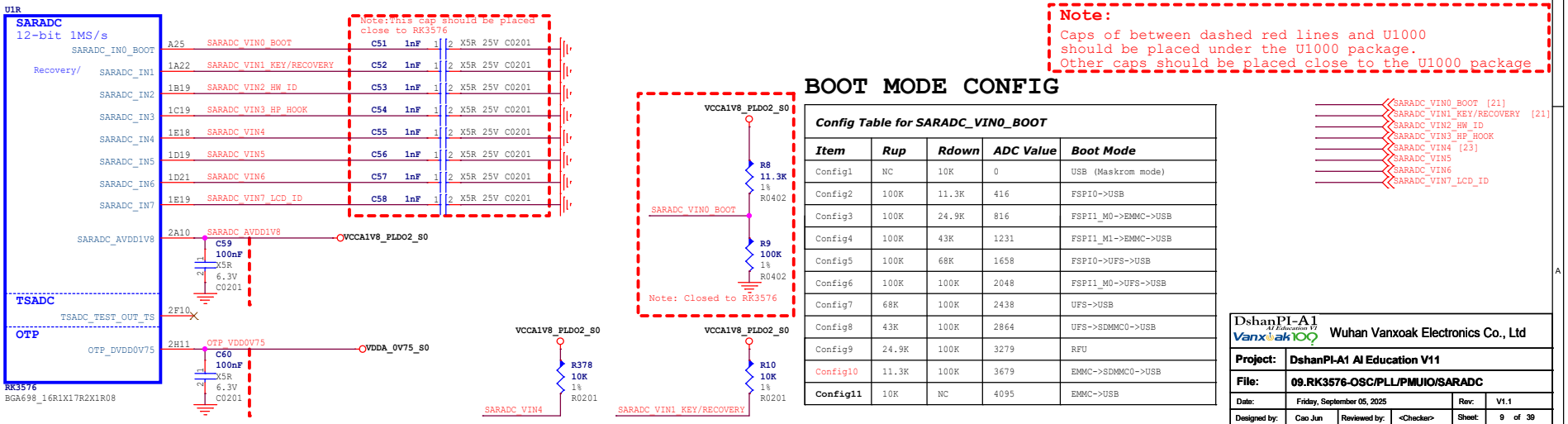
DshanPI-A1 AI Education V1
Vanxoak100
Wuhan Vanxoak Electronics Co., Ltd

Project:	DshanPI-A1 AI Education V11				
File:	08.RK3576-Power/GND				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	8 of 39

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

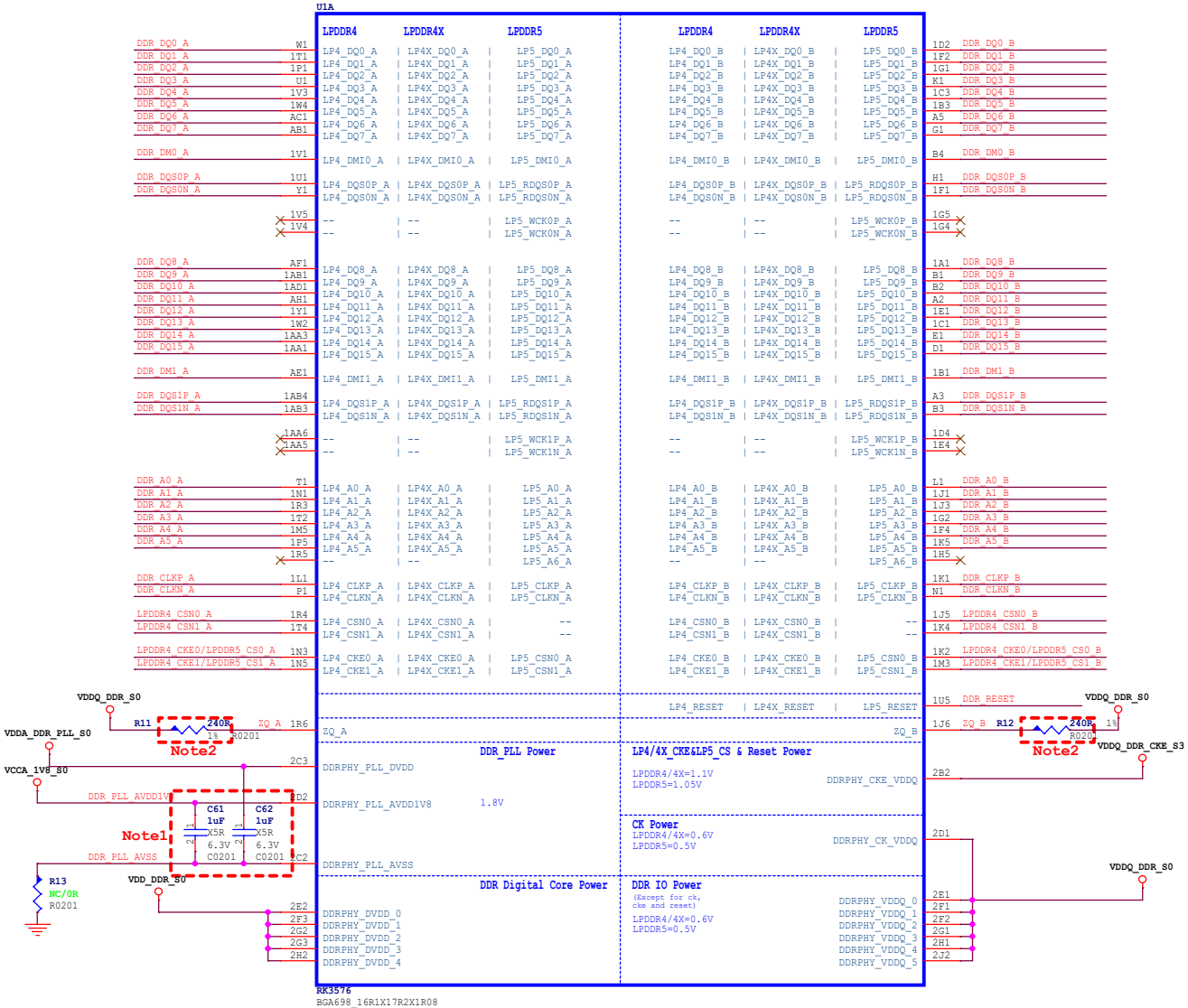
BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

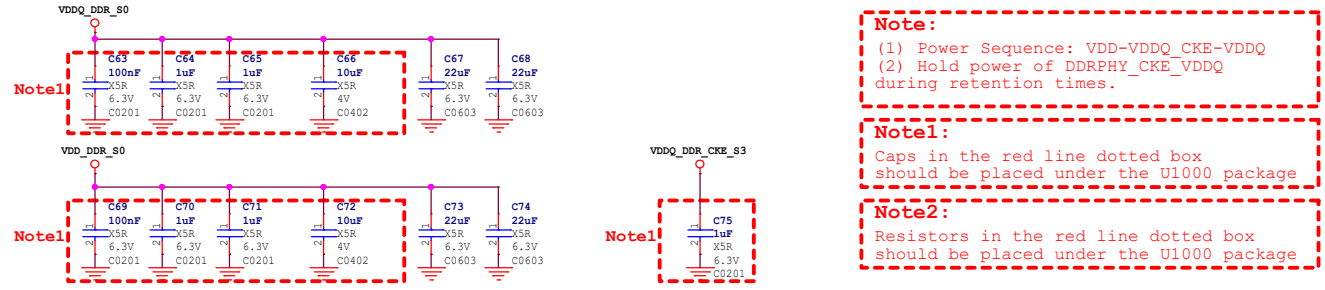
Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd			
Project:	DshanPI-A1 AI Education V11			
File:	09.RK3576-OSC/PLL/PMUIO/SARADC			
Date:	Friday, September 05, 2025		Rev:	V1.1
Designed by:	Cao Jun	Reviewed by: <Checker>	Sheet:	9 of 39

RK3576_A(DDRPHY)



DDR FILTER

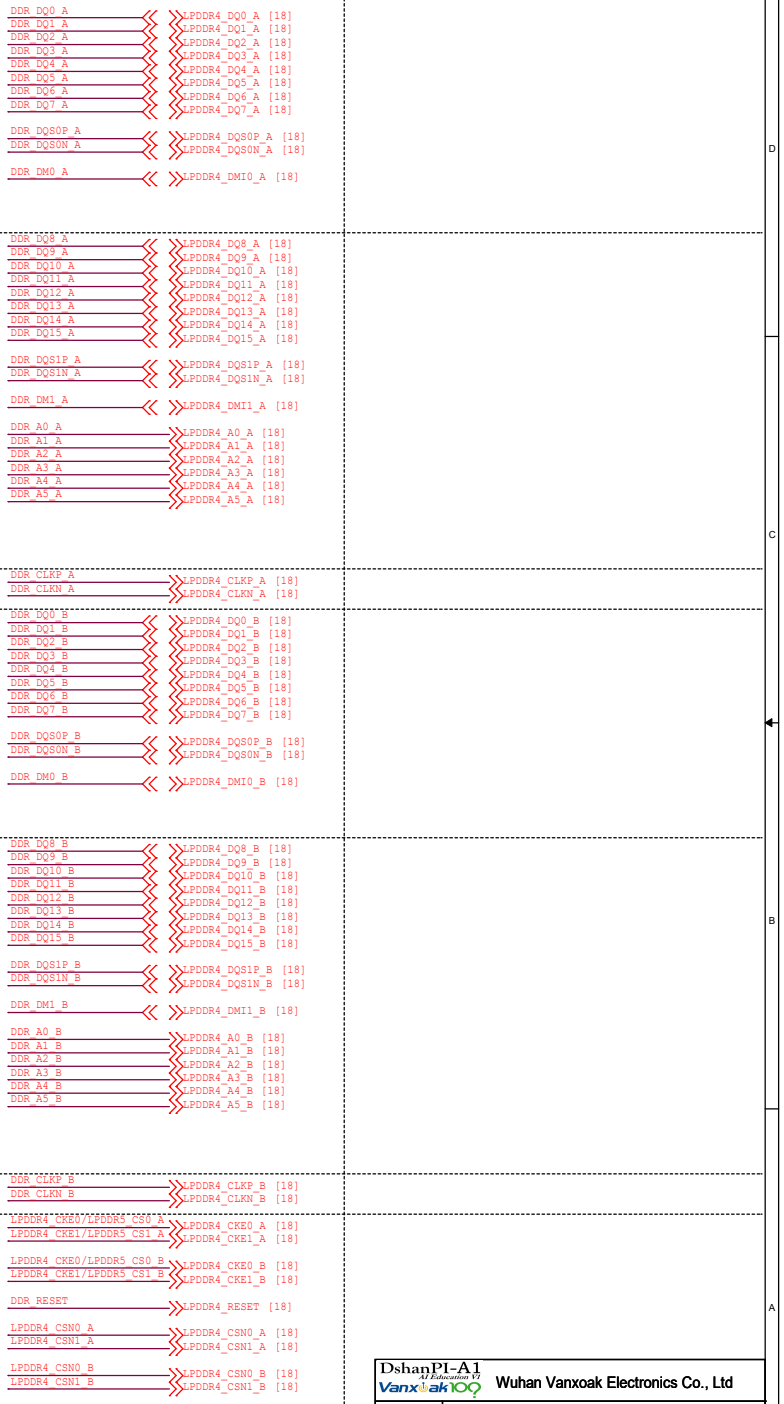


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDP
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

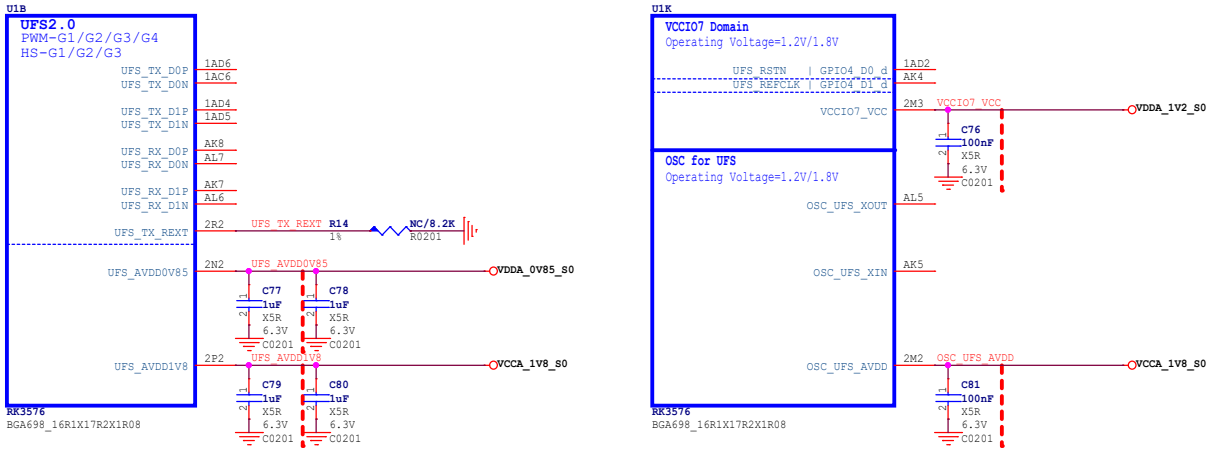
Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR4 Signal

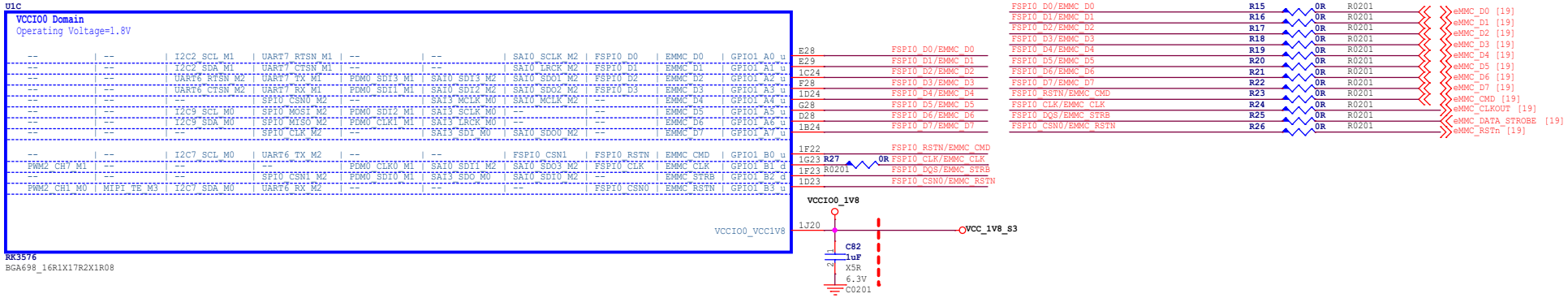


Wuhan Vanxoak Electronics Co., Ltd	
Project:	DshanPI-A1 AI Education V11
File:	10.RK3576-DDR PHY
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	10 of 39

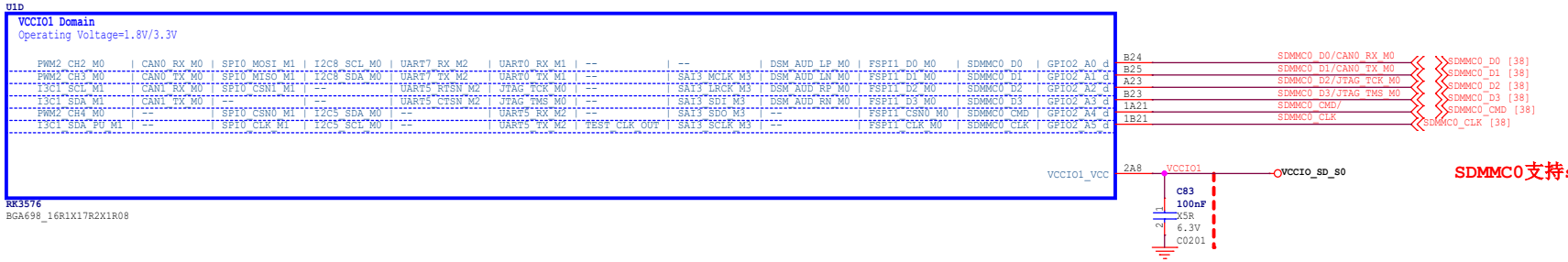
RK3576_B (UFS2.1)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



SDMMC0支持system boot

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	11.RK3576-eMMC/UFS/SD				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	11 of 39

RK3576_L (USB3/DP)

U1L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R08

Support:
Type-C With Displayport Alternate Mode

2T2 DP_TX_AUXP [30]
2T3 DP_TX_AUXN [30]
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P [30]
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N [30]
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P [30]
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N [30]
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P [30]
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N [30]
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P [30]
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N [30]

2T7 USB3_OTG0_DP_TX_REXT R28 8.2K 1% R0201

2M5 USB3_OTG0/DP_TX_AVDD0V85
2N5
VDDA_0V85_S0
C84 1uF X5R 6.3V C0201
C85 NC/1uF X5R 6.3V C0201

2N4 USB3_OTG0/DP_TX_AVDD1V8
VCCA_1V8_S0
C86 1uF X5R 6.3V C0201
C87 NC/1uF X5R 6.3V C0201

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

U1M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

RK3576
BGA698_16R1X17R2X1R08

40K
40K

AK9 USB2_OTG0_DP [30]
AL9 USB2_OTG0_DM [30]
2R6 USB2_OTG0_ID Note: There is an internal pull-up resistor connected to 1.8V
USB2_OTG0_ID [30]
2P3
USB2_OTG0_VBUSDET [30]
C88 100nF X5R 10V C0201
2R3 USB2_OTG0_REXT R29 200R 1% R0201

Note!!!
The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

2T4 USB2_HOST1_DP [28]
2T5 USB2_HOST1_DM [28]
2T9 USB2_OTG1_ID R30 10K 1% R0201
2T10 USB2_OTG1_VBUSDET
VCC5V0_SYS_S5
C89 100nF X5R 10V C0201
R33 NC/20K R0402
R31 NC/10K R0201
Option: For test
2U8 USB2_OTG1_REXT R32 200R 1% R0201

2P5 USB2_OTG_DVDD0V75
VDDA_0V75_S0
C90 100nF X5R 6.3V C0201

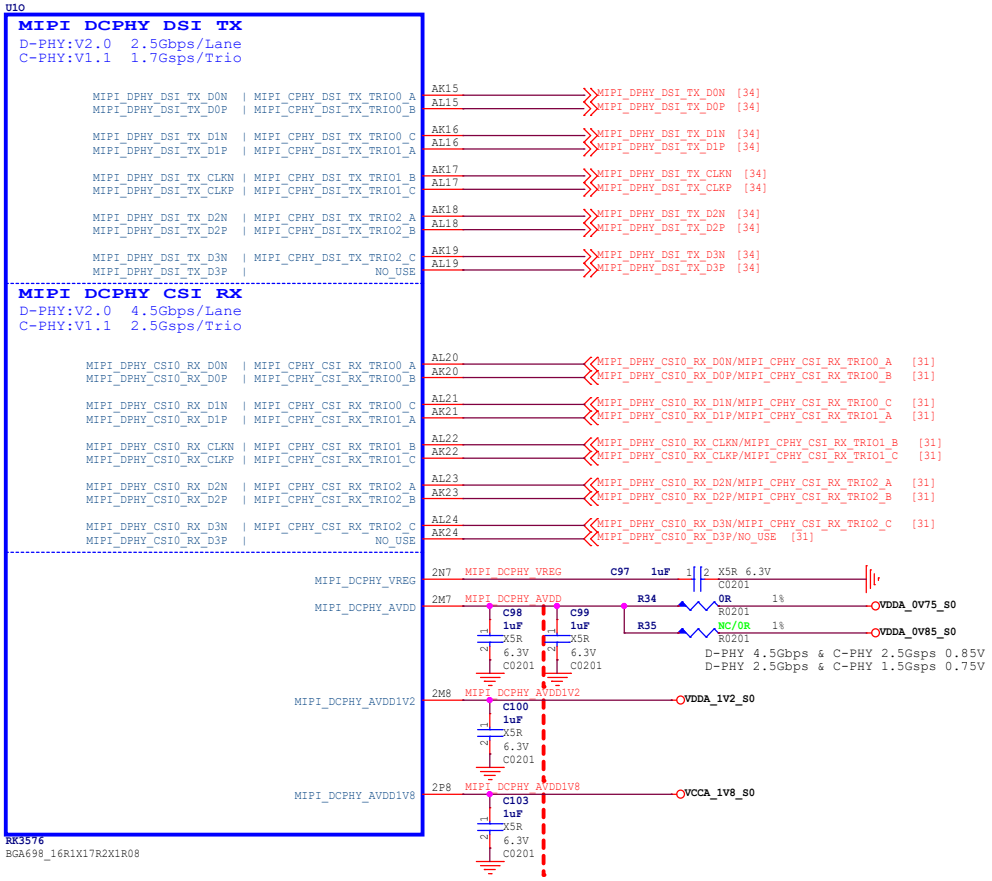
2P4 USB2_OTG_AVDD1V8
VCCA_1V8_S0
C91 100nF X5R 6.3V C0201
C92 NC/1uF X5R 6.3V C0201

2P7 USB2_OTG_AVDD3V3
VCC_3V3_S0
C93 100nF X5R 6.3V C0201

DshanPI-A1 AI Education V1
Vanxoak100
Wuhan Vanxoak Electronics Co., Ltd

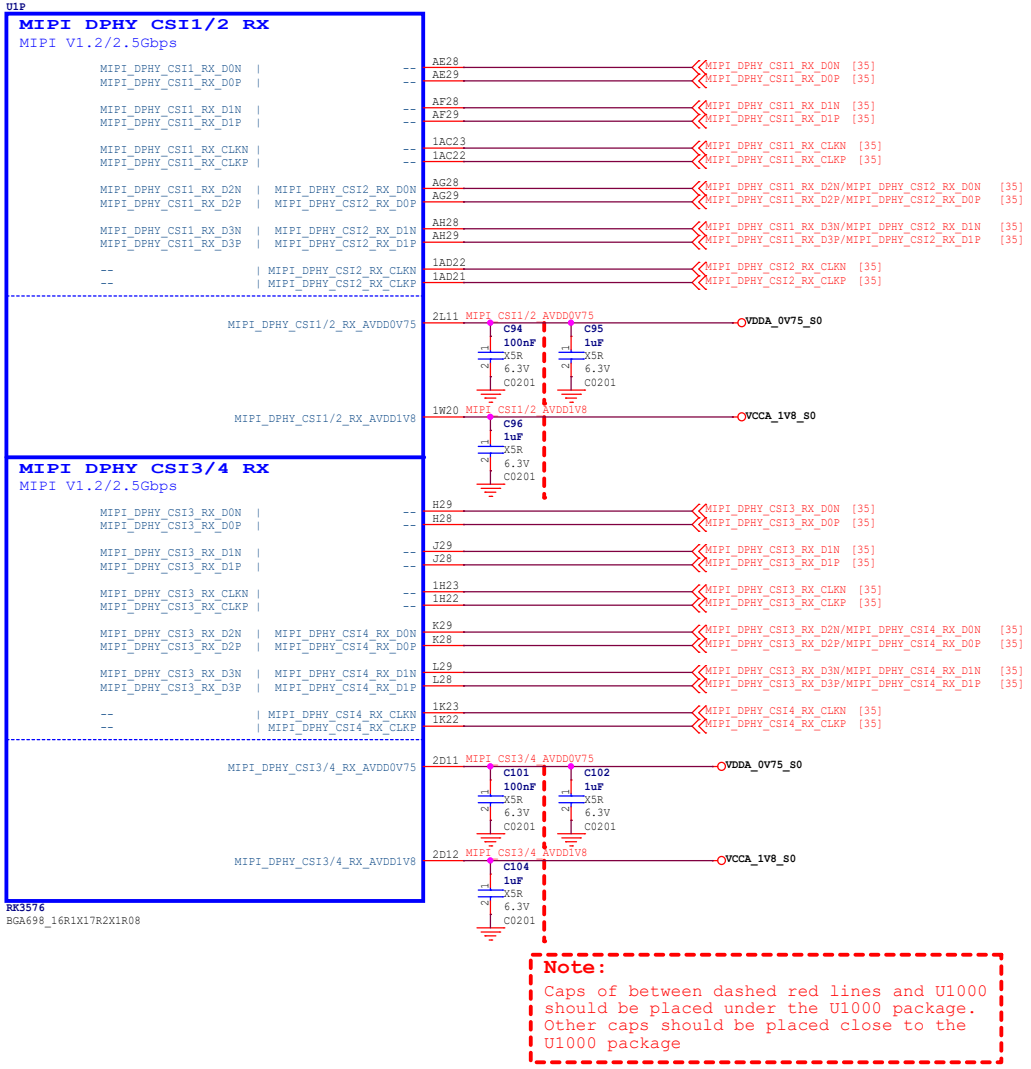
Project:	DshanPI-A1 AI Education V11				
File:	12.RK3576-TypeC/USB				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	12 of 39

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

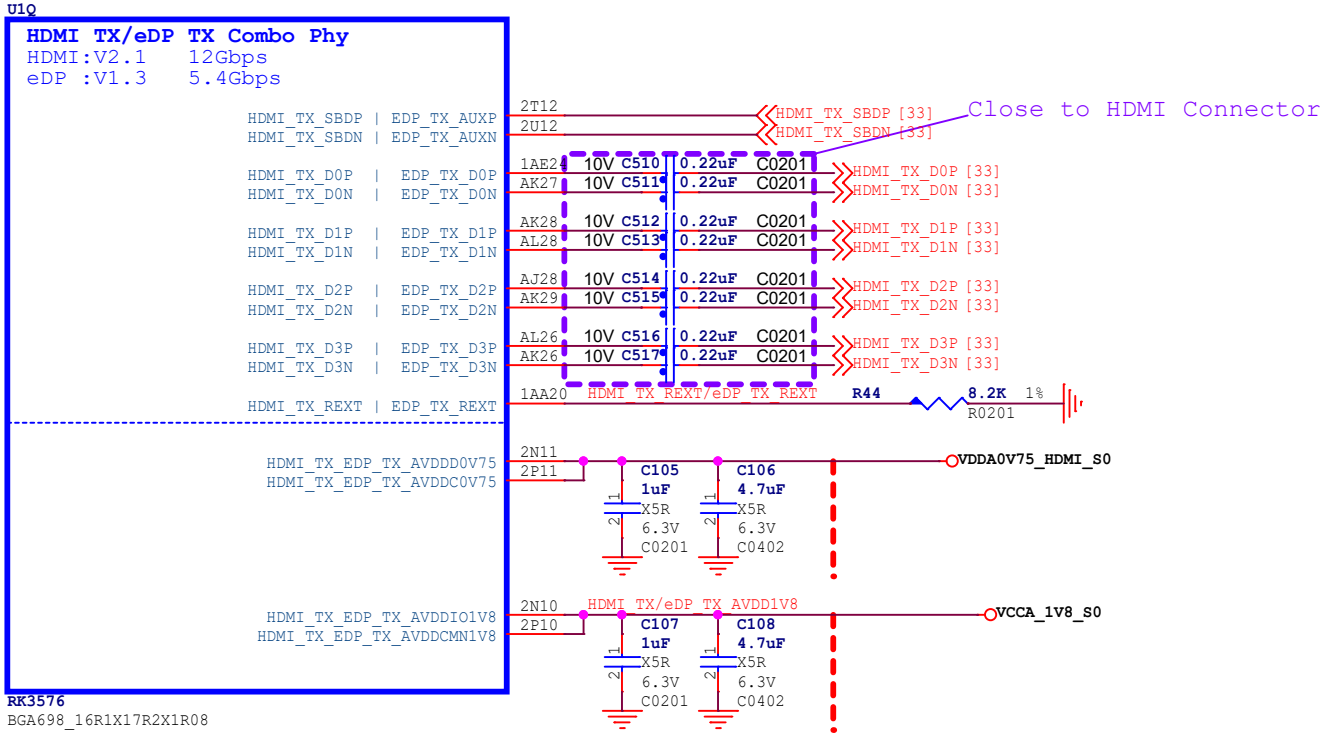


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	13.RK3576-MIPI DSI/CSI				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	13 of 39

RK3576_Q(HDMI/eDP)

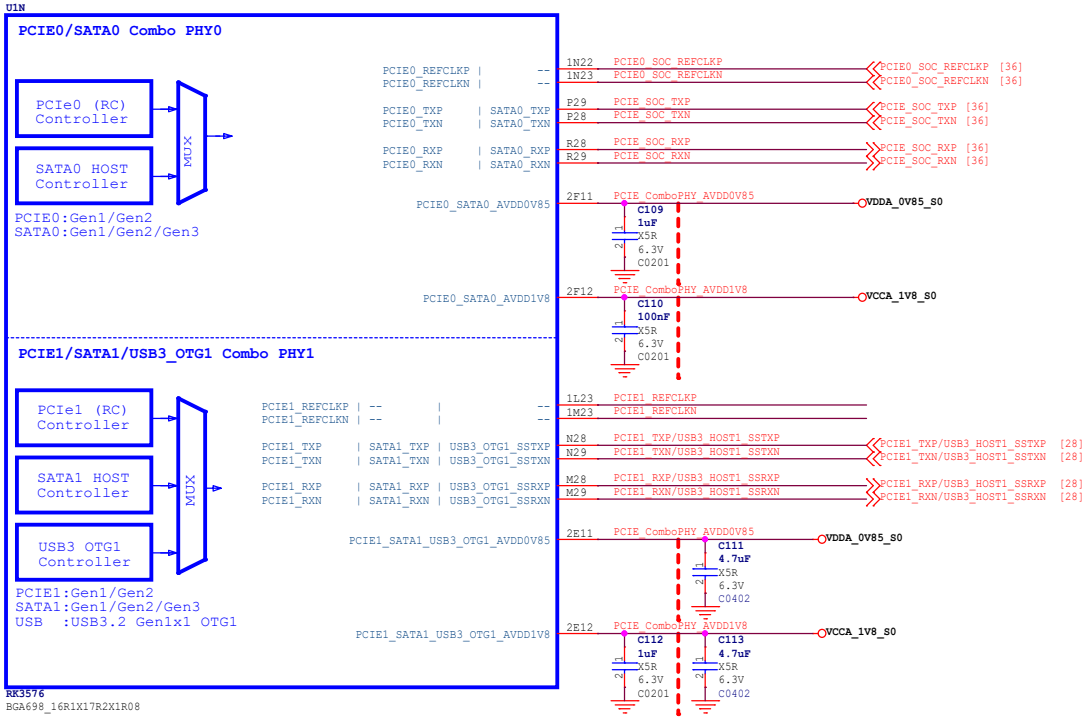
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	14.RK3576-HDMI/eDP				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	14 of 39

RK3576_N(PCIe/SATA/USB3)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	15.RK3576-PCIe/SATA/USB3				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	15 of 39

RK3576_F(VCCIO2)

U1F

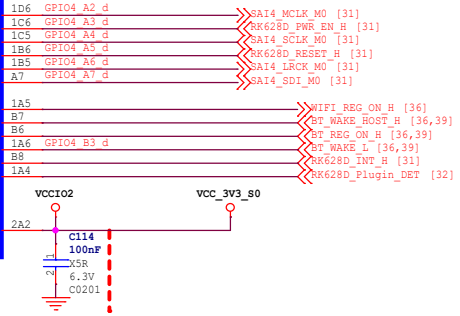
VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	GPIO4_A6_d
PWM2_CH8_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

RK3576

BGA698_16R1X17R2X1R08



RK3576_G(VCCIO3)

U1G

VCCIO3 Domain

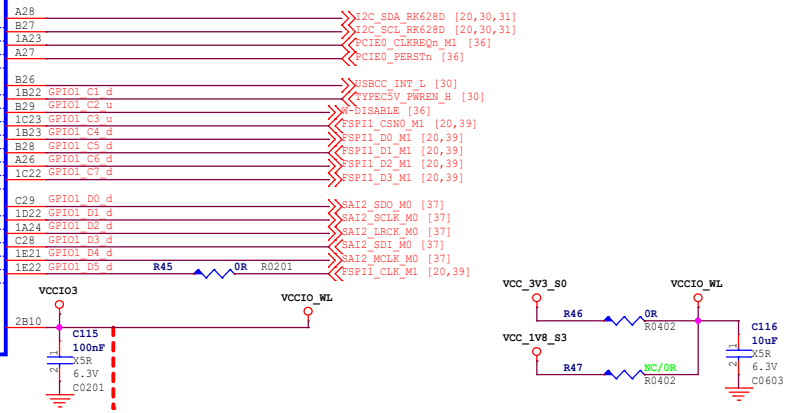
Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	--	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_RXCLK_M1	GPIO1_C1_d
PWM1_CH4_M1	--	SPI2_CSN1_M1	I2C8_SCL_M1	UART4_RTSN_M1	--	--	SPDIF_CSN1_M1	SPDIF_RSTN_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C8_SDA_M1	UART4_CTSN_M1	--	--	--	SPDIF_CSN0_M1	SDMMC1_DETN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	SPDIF1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	SPDIF1_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	SPDIF1_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	SPDIF1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

RK3576

BGA698_16R1X17R2X1R08

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



RK3576_J(VCCIO6)

U1J

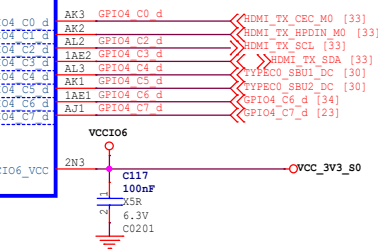
VCCIO6 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RP_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

RK3576

BGA698_16R1X17R2X1R08



DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	16.RK3576-GPIO VCCIO2/3/6				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	16 of 39

RK3576_H(VCCIO4)

U1H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d
--	--	PCIE0_CLKREQN_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d
--	--	PCIE1_CLKREQN_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_RXD2_M0	VI_CIF_D2	GPIO2_C3_d
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDO0_M0	SAI2_SDO_M1	--	ETH1_RXD3_M0	VI_CIF_D1	GPIO2_C4_d
PWM0_CH3_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d
PWM1_CH4_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d
PWM0_CH1_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d

RK3576

BGA698_16R1X17R2X1R08

B22 SDMMC1_D0_M1 [36]
B20 SDMMC1_D1_M1 [36]
B19 GPIO2_B0_d
1A18 GPIO2_B1_d
SDMMC1_D2_M1 [36]
SDMMC1_D3_M1 [36]
1A17 SDMMC1_CMD_M1 [36]
1B16 SDMMC1_CLK_M1 [36]
A19 UART7_CTSN_M0 [36,39]
1C18 UART7_RTSN_M0 [36,39]
A21 UART7_TX_M0 [36,39]
B21 UART7_RX_M0 [36,39]

A17 GMAC1_RXD2_M0 [26]
1A15 GMAC1_RXD3_M0 [26]
1D15 GMAC1_RXCLK_M0 [26]
A15 GPIO2_C3_d R48 0R R0201 GMAC1_TXD2_M0 [26]
1A13 GPIO2_C4_d R49 0R R0201 GMAC1_TXD3_M0 [26]
1C15 GPIO2_C5_d R50 0R R0201 GMAC1_TXCLK_M0 [26]
1A14 GPIO2_C6_d R51 0R R0201 GMAC1_TXD0_M0 [26]
B15 GPIO2_C7_d R52 0R R0201 GMAC1_TXD1_M0 [26]

B16 GPIO2_D0_d R53 0R R0201 GMAC1_TXCTL_M0 [26]
1A16 GMAC1_RXD0_M0 [26]
B17 GMAC1_RXD1_M0 [26]
B18 GMAC1_RXCTL_M0 [26]
1B13 GPIO2_D4_d R54 0R R0201 GMAC1_MDC_M0 [26]
1B15 GPIO2_D5_d R55 0R R0201 GMAC1_MDIO_M0 [26]
1D18 GPIO2_D6_d WIFI_WAKE_HOST_H [36]
1E15 GPIO2_D7_d GMAC1_MCLKINOUT_M0 [26]

1D16 SAI3_SCLK_M2 [36,39]
1B18 SAI3_LRCK_M2 [36,39]
1A20 GPIO3_A2_d SAI3_SDO_M2 [36,39]
1A19 SAI3_SDI_M2 [36,39]

VCCIO4
2A7 VCCIO4_VCC
C118 NC/100nF X5R 6.3V C0201
C119 1uF X5R 6.3V C0201
VCC_1V8_S0

RK3576_I(VCCIO5)

U1I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH1_PTP_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d
PWM3_CH0_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART12_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS1_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d
PWM2_CH5_M3	I3C1_SCL_M2	--	UART12_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKF	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d

RK3576

BGA698_16R1X17R2X1R08

1D13 GPIO3_A4_d
A9 GPIO3_A5_d R56 0R R0201 GMAC0_MDIO_M0 [25]
1A7 GPIO3_A6_d R57 0R R0201 GMAC0_MDC_M0 [25]
B13 GMAC0_RXCTL_M0 [25]

B14 GPIO3_B0_d
1A11 GMAC0_MCLKINOUT_M0 [25]
A13 GMAC0_RXD1_M0 [25]
A11 GPIO3_B3_d R58 0R R0201 GMAC0_RXD0_M0 [25]
B10 GPIO3_B4_d R59 0R R0201 GMAC0_TXCTL_M0 [25]
1A9 GPIO3_B5_d R60 0R R0201 GMAC0_TXD1_M0 [25]
B11 GPIO3_B6_d R61 0R R0201 GMAC0_TXD0_M0 [25]
1D12 GMAC0_TXCLK_M0 [25]
UART2_RX_M2 [35]

1E9 UART2_TX_M2 [35]
1B10 I2C5_SDA_M3 [39]
B9 GPIO3_C2_d R62 0R R0201 GMAC0_TXD3_M0 [25]
1A8 GPIO3_C3_d R63 0R R0201 GMAC0_TXD2_M0 [25]
1D9 I2C5_SCL_M3 [39]
1B9 GPIO3_C5_d
1D7 GPIO3_C5_d [35]
1C7 GPIO3_C6_d [35]
GPIO3_C7_d [39]

1C12 GPIO3_D0_d [39]
1A12 GMAC0_RXCLK_M0 [25]
1A10 GMAC0_RXD3_M0 [25]
B12 GMAC0_RXD2_M0 [25]
1E12 GPIO3_D4_d I2C3_SCL_M2 [35]
1D10 I2C3_SDA_M2 [35]
1C10 GPIO3_D6_d UART5_CTS_M0 [35]
1E7 CAM_CLK0_OUT_M0 [35]

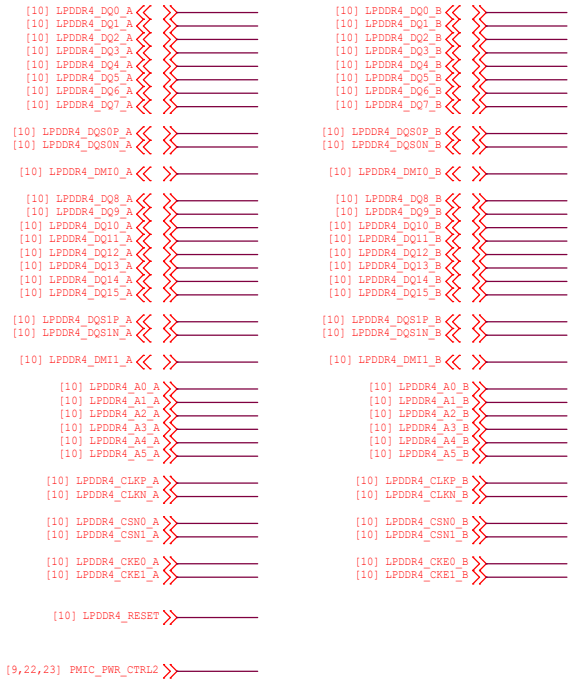
1B12 CAM_CLK1_OUT_M0 [35]
1B7 CAM_CLK2_OUT_M0 [35]

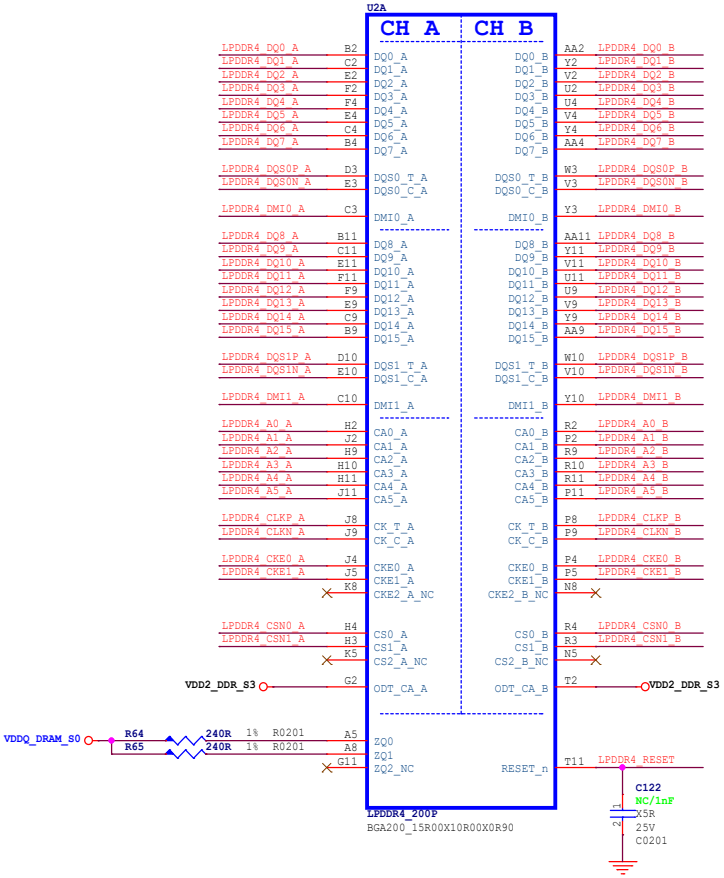
VCCIO5_VCC_0
VCCIO5_VCC_1
2A4
2A5
VCCIO5
VCC_1V8_S0
C120 NC/100nF X5R 6.3V C0201
C121 1uF X5R 6.3V C0201

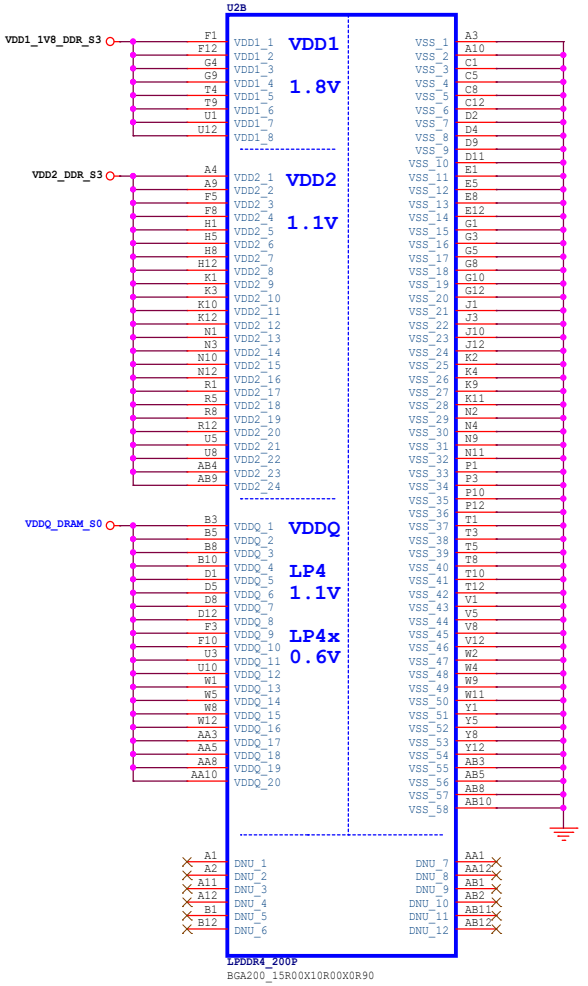
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd		
Project:	DshanPI-A1 AI Education V11		
File:	17.RK3576-GPIO VCCIO4/5		
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by: <Checker>	Sheet: 17 of 39

LPDDR4/4X



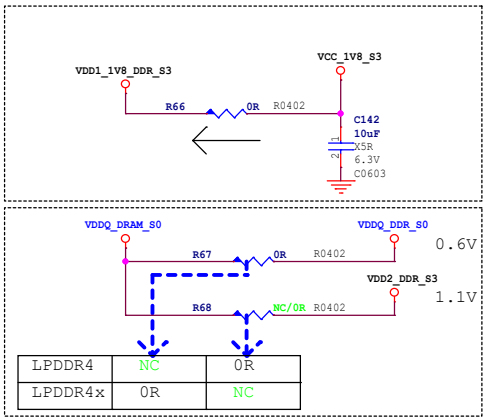


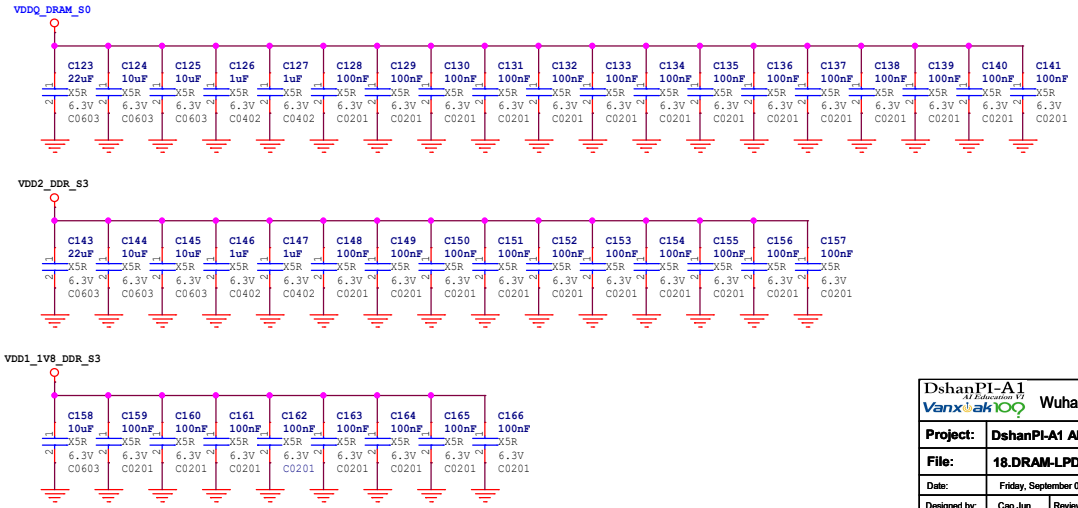


Note:

Sequence:VDD1-VDD2-VDDQ

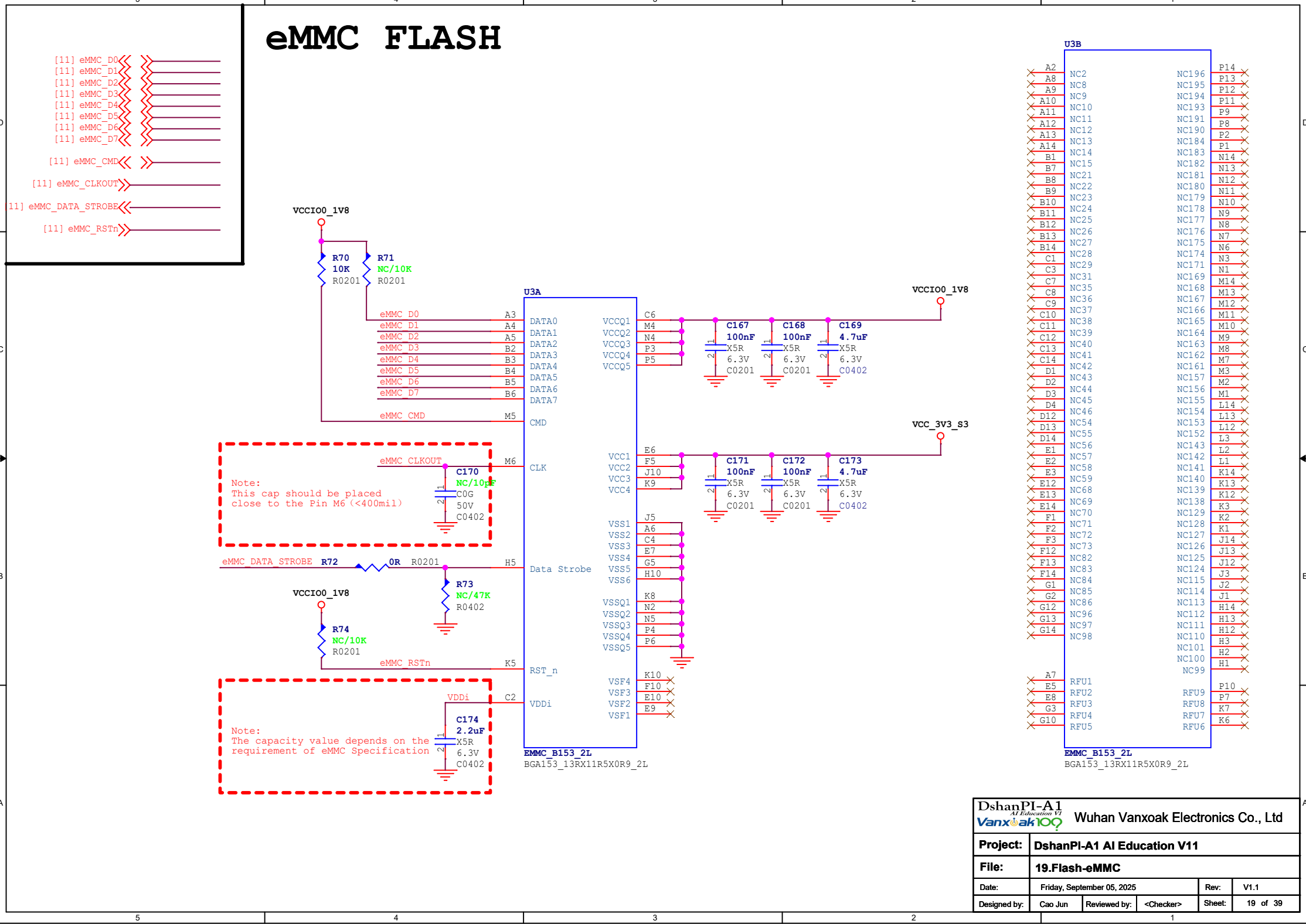
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65





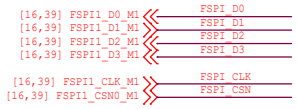
DshanPI-A1 AI Education V1	Wuhan Vanxoak Electronics Co., Ltd
Project:	DshanPI-A1 AI Education V11
File:	18.DRAM-LPDDR4X_1X32bit_200P
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	18 of 39

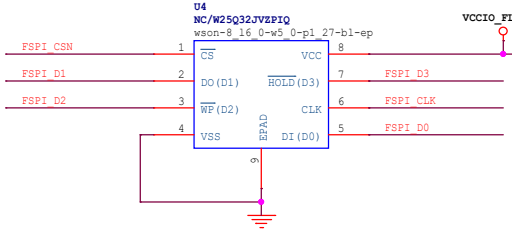
eMMC FLASH



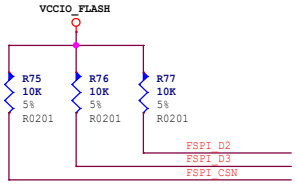
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	19.Flash-eMMC				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	19 of 39

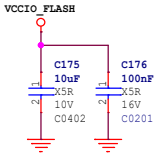
SPI Flash



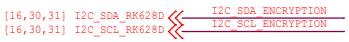


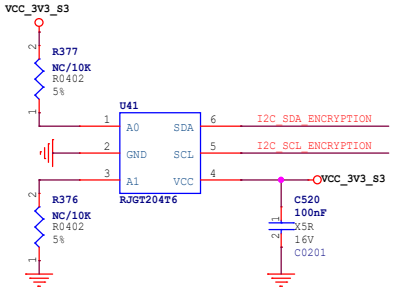
Voltage:3.3V





Encryption

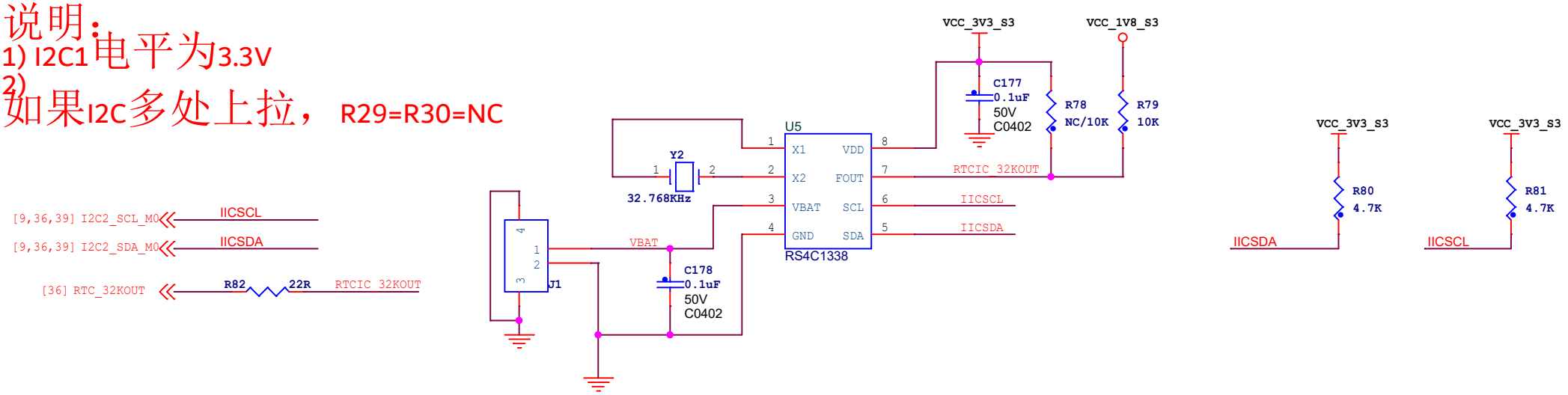


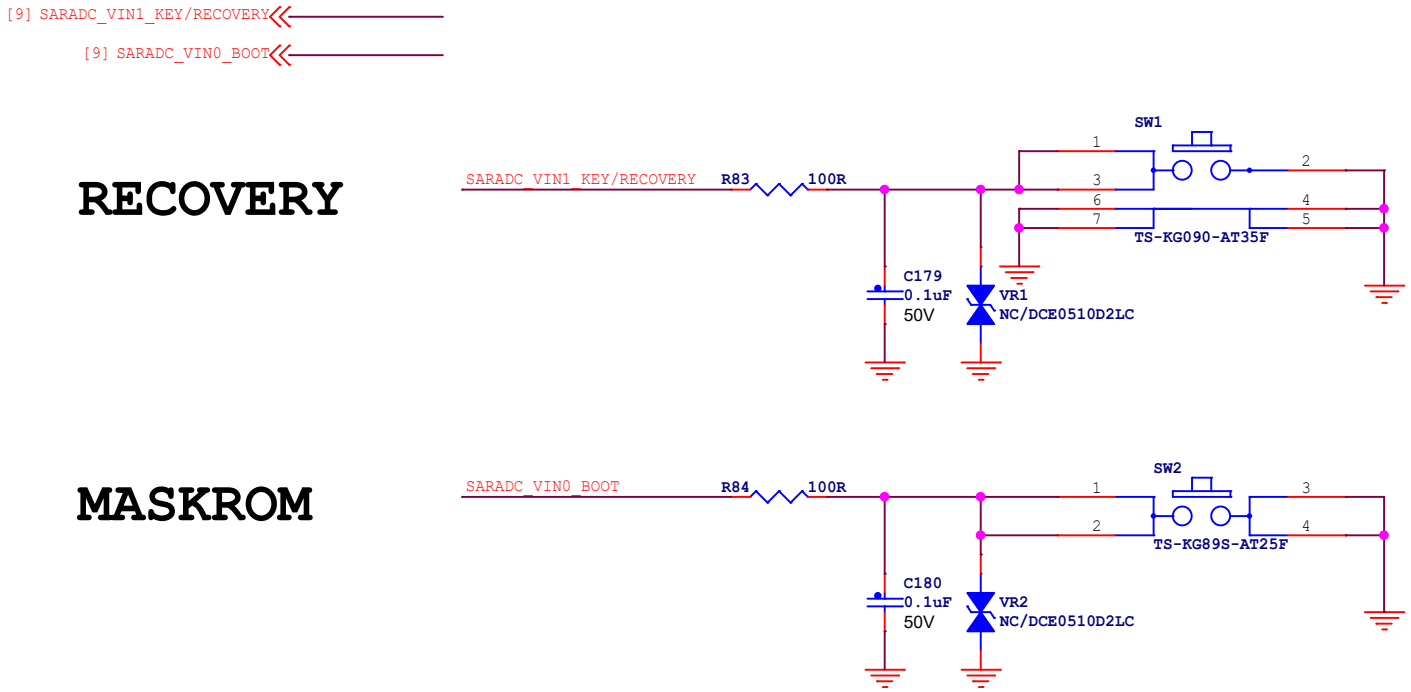


A0	A1	Adress
1	0	0x69
NC	NC	0x68

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	20.Flash-SPI Flash/Encryption				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	20 of 39

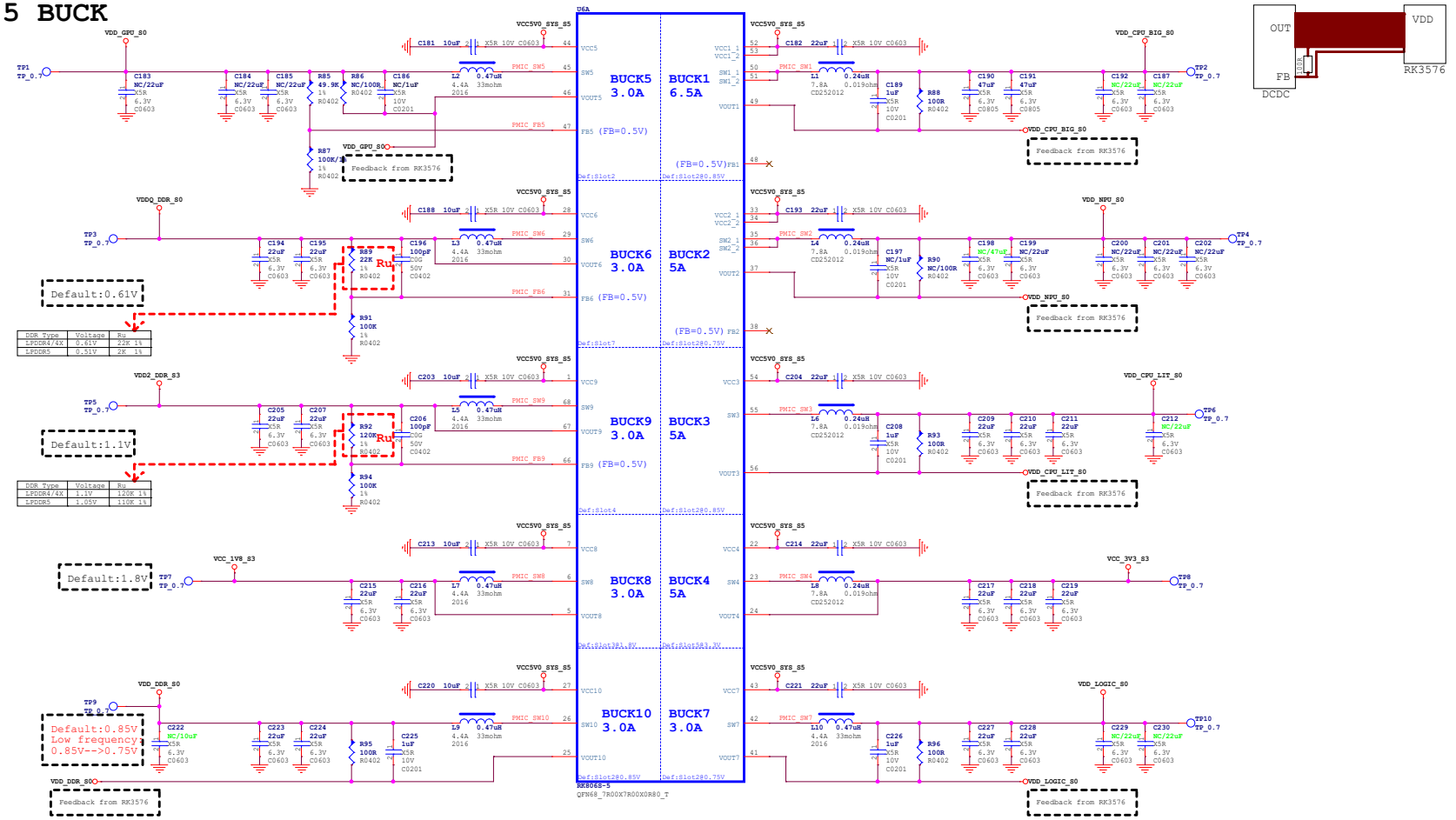
说明：
1) I2C1电平为3.3V
2)
如果I2C多处上拉， R29=R30=NC





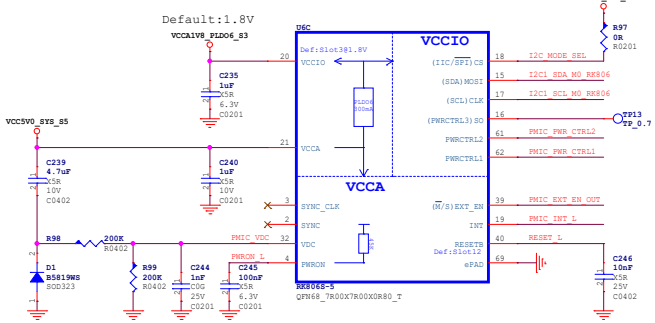
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	21.RTC/MASKROM/RECOVERY				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	21 of 39

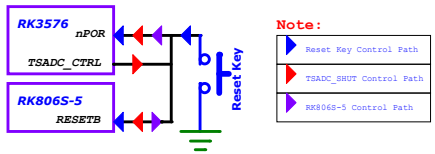
PMIC RK806S-5 BUCK



PMIC RK806S-5 Managerment

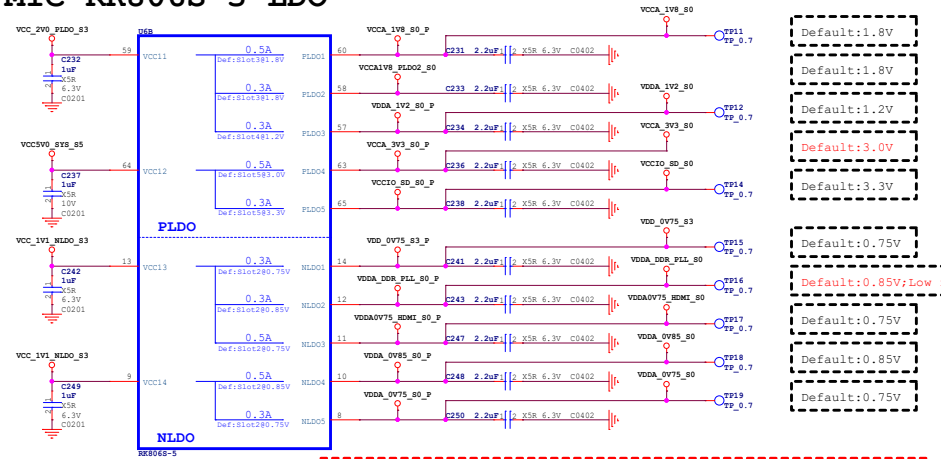
Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND





Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806S-5 Control Path

PMIC RK806S-5 LDO

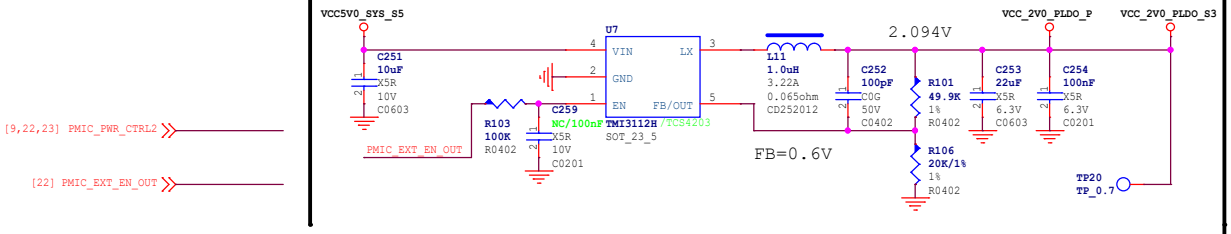


Note:

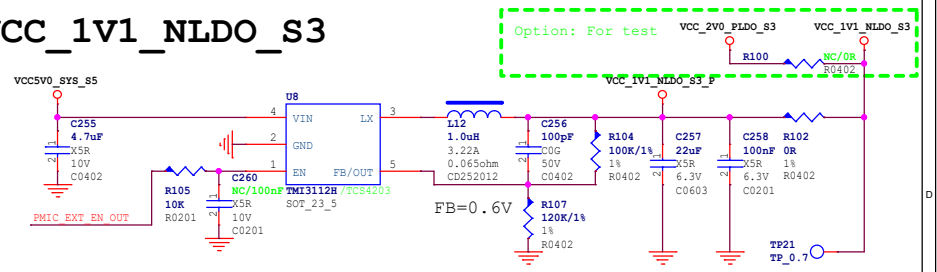
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

DshanPI-A1	Wuhan Vanxoak Electronics Co., Ltd		
Project:	DshanPI-A1 AI Education V11		
File:	22.Power-PMIC RK806S-5		
Date:	Friday, September 05, 2025	Rev:	V1.1
Designed by:	Cao Jun	Reviewed by: <Checker>	Sheet: 22 of 39

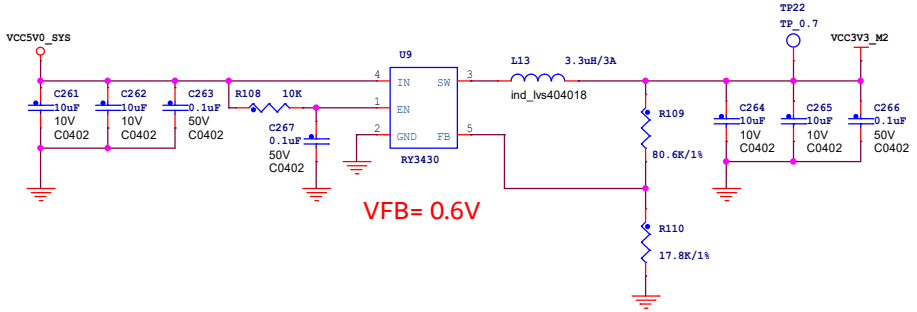
VCC_2V0_PLDO_S3



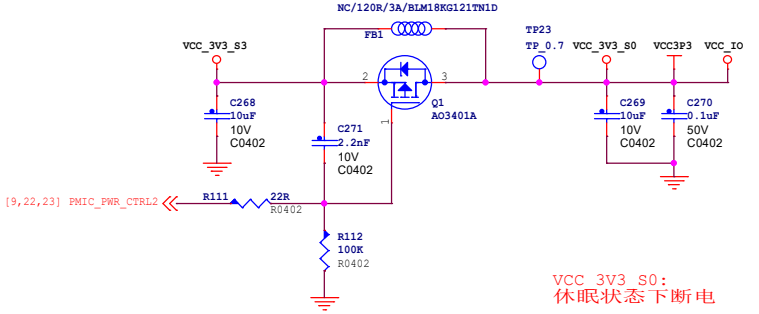
VCC_1V1_NLDO_S3



VCC3V3_M2



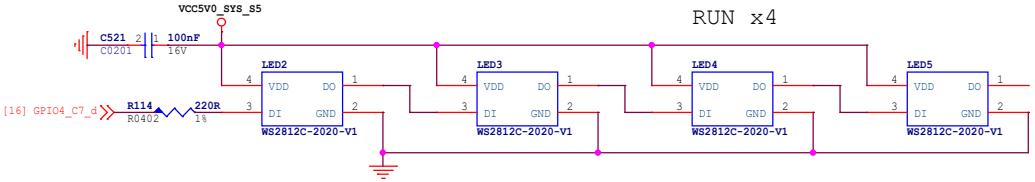
VCC_3V3_S0



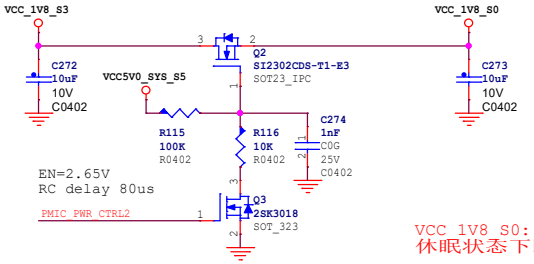
VCC_3V3_S0:
休眠状态下断电
VCC_3V3_S3:
休眠状态下保持上电

LED

POWER

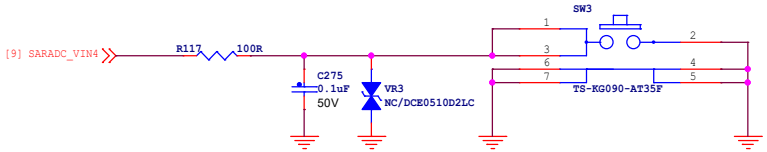


VCC_1V8_S0



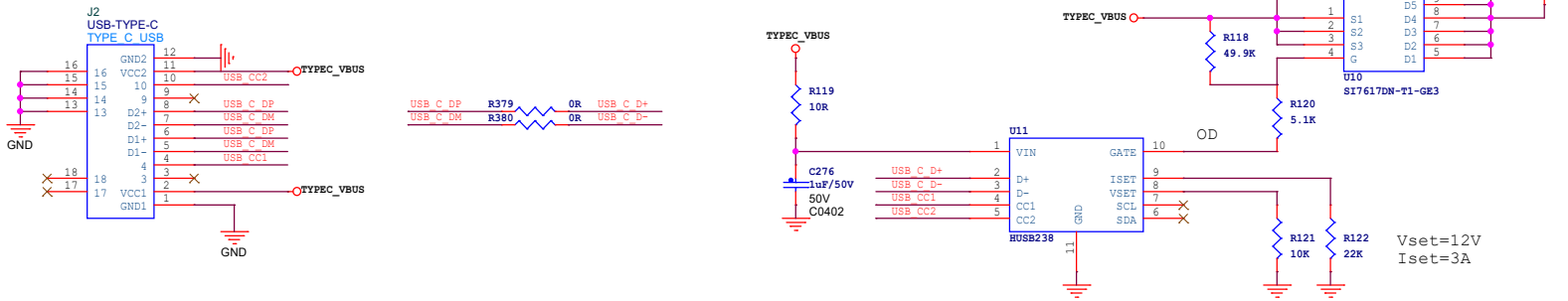
VCC_1V8_S0:
休眠状态下断电
VCC_1V8_S3:
休眠状态下保持上电

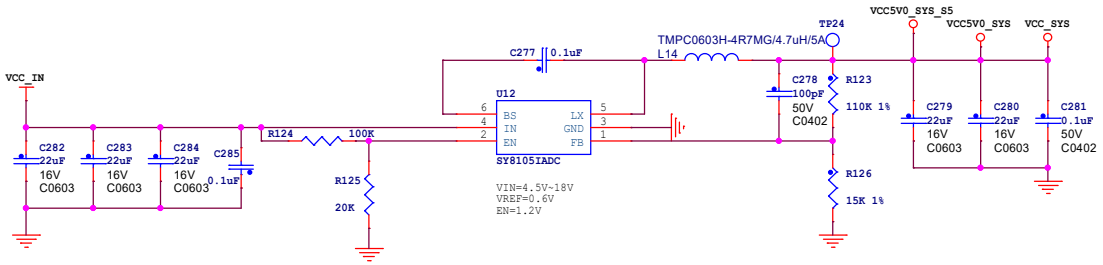
USER KEY

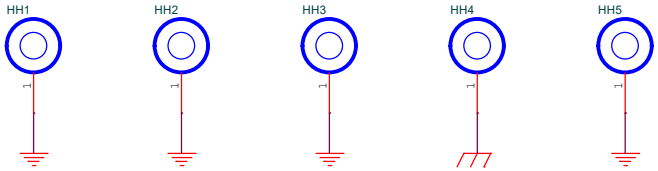


DshanPI-A1 AI Education V11 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	23.Power-Ext Discrete/LED/KEY				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	23 of 39

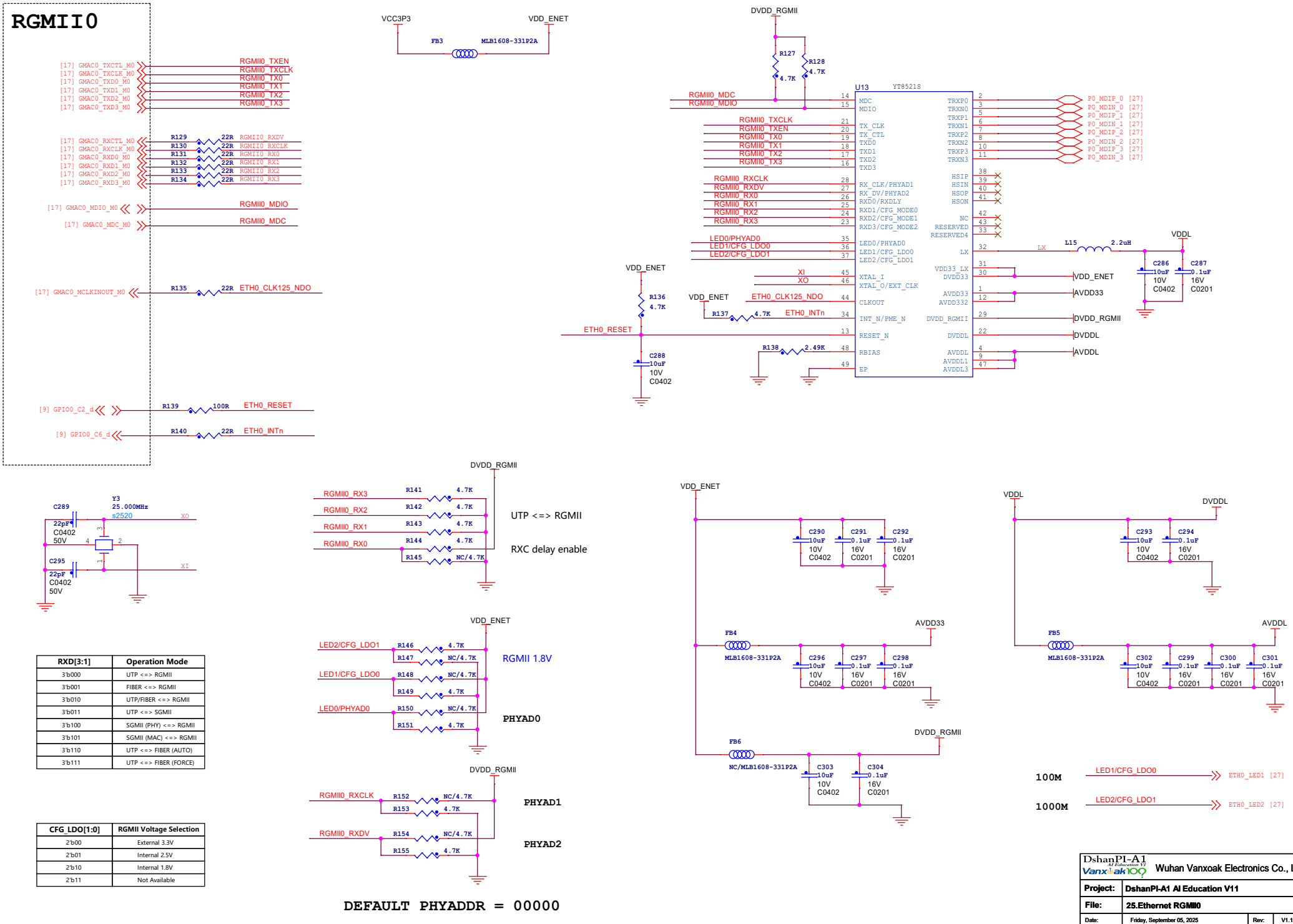
Power DC IN







DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	24.Power-DC IN				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	24 of 39

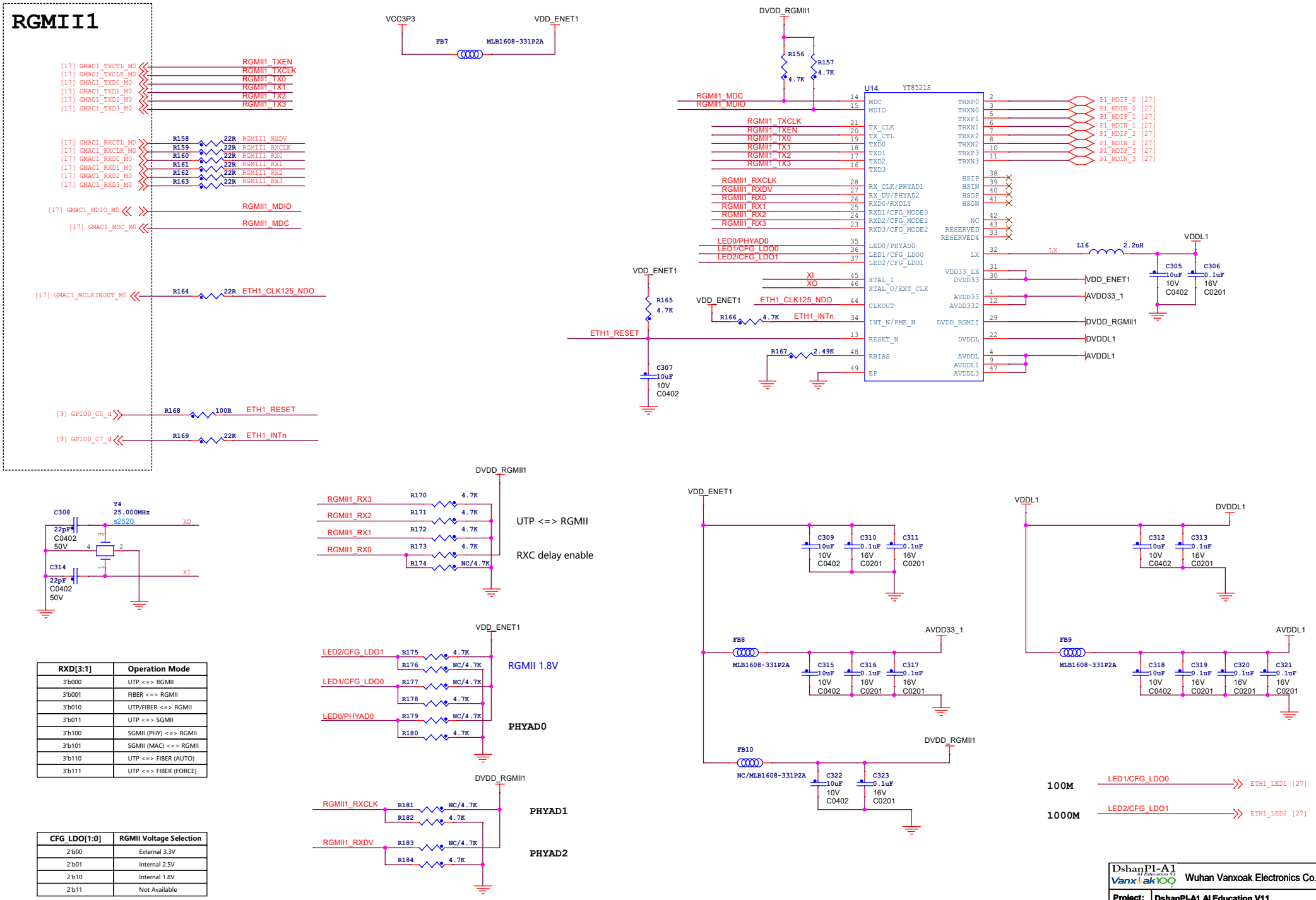


RXD[3:1]	Operation Mode
3'b000	UTP <=> RGMII
3'b001	FIBER <=> RGMII
3'b010	UTP/FIBER <=> RGMII
3'b011	UTP <=> SGMII
3'b100	SGMII (PHY) <=> RGMII
3'b101	SGMII (MAC) <=> RGMII
3'b110	UTP <=> FIBER (AUTO)
3'b111	UTP <=> FIBER (FORCE)

CFG_LDO[1:0]	RGMII Voltage Selection
2'b00	External 3.3V
2'b01	Internal 2.5V
2'b10	Internal 1.8V
2'b11	Not Available

DEFAULT PHYADDR = 00000

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd
Project:	DshanPI-A1 AI Education V11
File:	25.Ethernet RGMII0
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	25 of 39



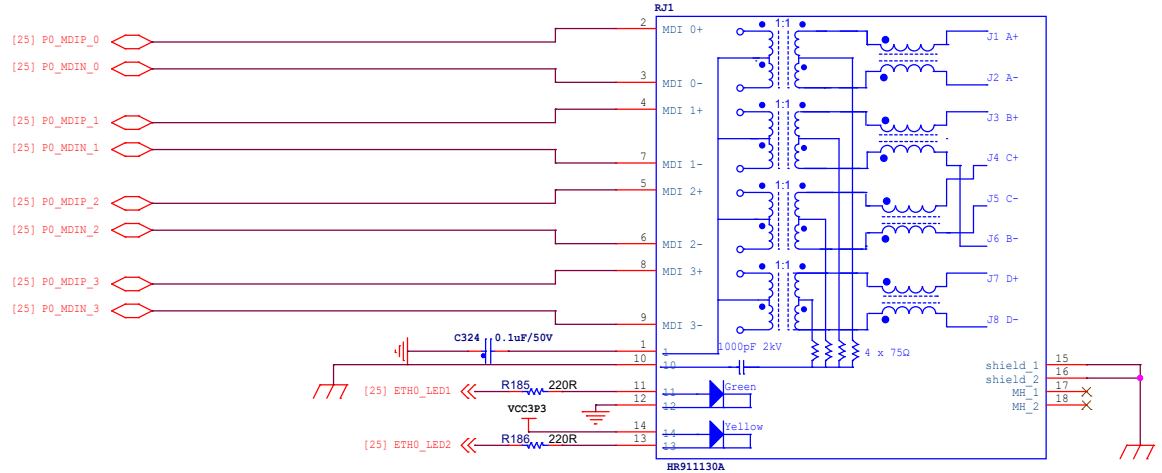
RXD[3:1]	Operation Mode
3'b000	UTP <=> RGMII
3'b001	FIBER <=> RGMII
3'b010	UTP/FIBER <=> RGMII
3'b011	UTP <=> SGMII
3'b100	SGMII (PHY) <=> RGMII
3'b101	SGMII (MAC) <=> RGMII
3'b110	UTP <=> FIBER (AUTO)
3'b111	UTP <=> FIBER (FORCE)

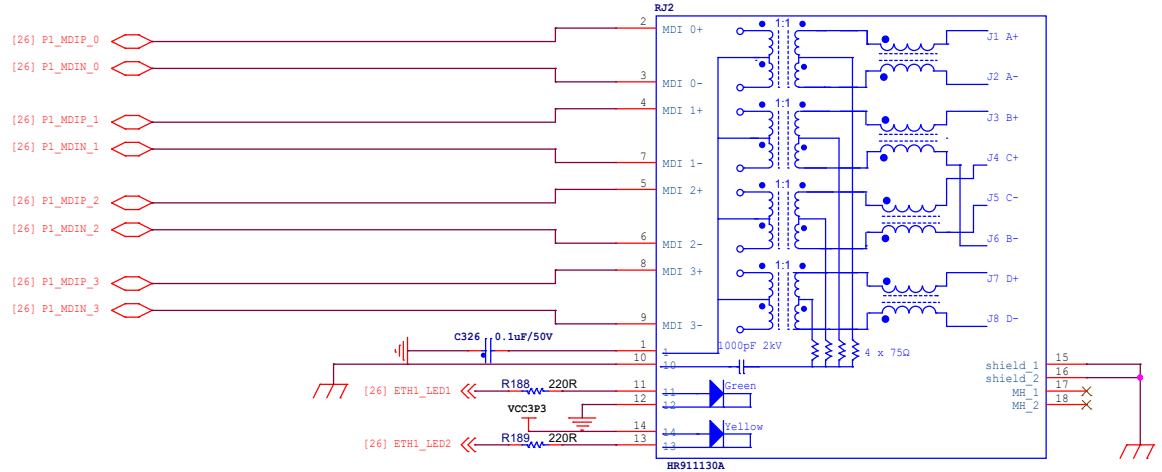
CFG_LDO[1:0]	RGMII Voltage Selection
2'b00	External 3.3V
2'b01	Internal 2.5V
2'b10	Internal 1.8V
2'b11	Not Available

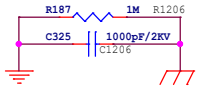
DEFAULT PHYADDR = 00000

DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd
Project:	DshanPI-A1 AI Education V11
File:	26.Ethernet RGMII1
Date:	Friday, September 05, 2025
Rev:	V1.1
Designed by:	Cao Jun
Reviewed by:	<Checker>
Sheet:	26 of 39

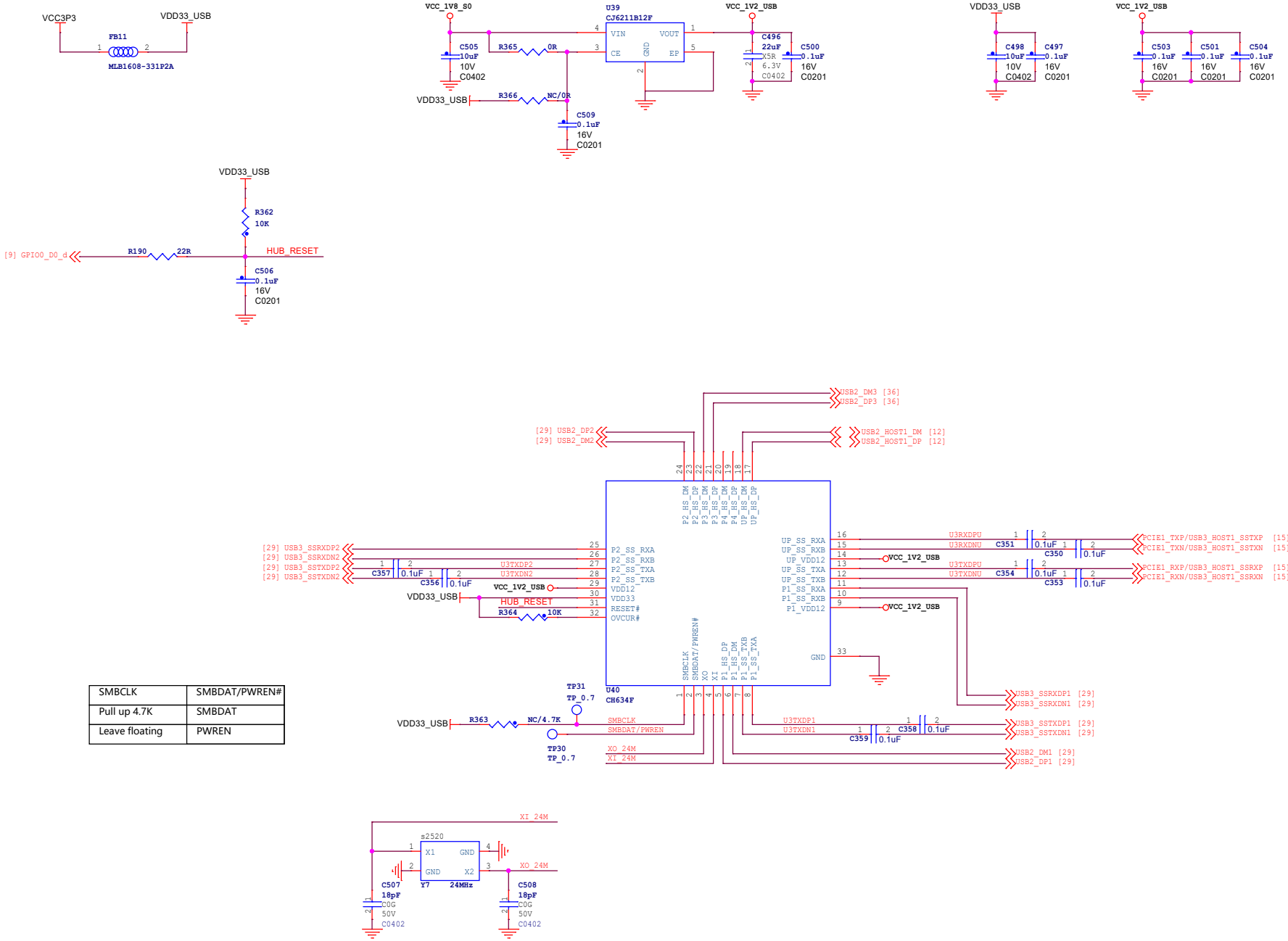
RJ45 x2







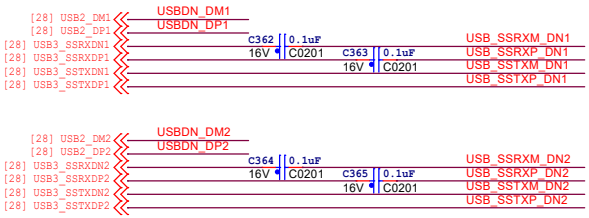
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	27.RJ45				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	27 of 39

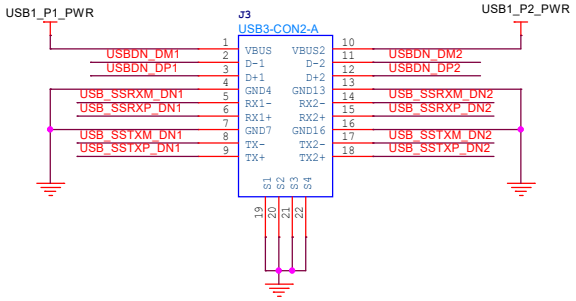


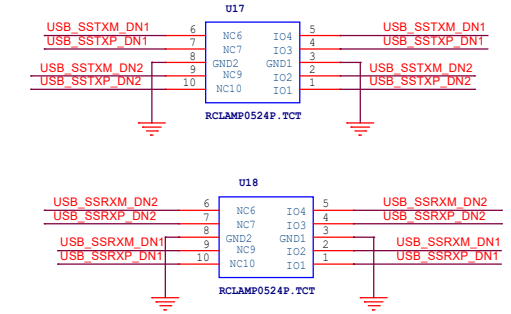
SMBCLK	SMBDAT/PWREN#
Pull up 4.7K	SMBDAT
Leave floating	PWREN

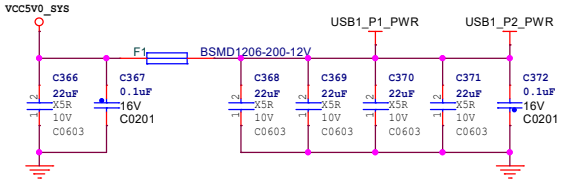
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	28.USB3.0 Hub				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	28 of 39

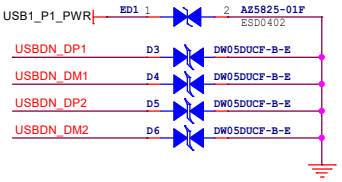
USB3.0 x2





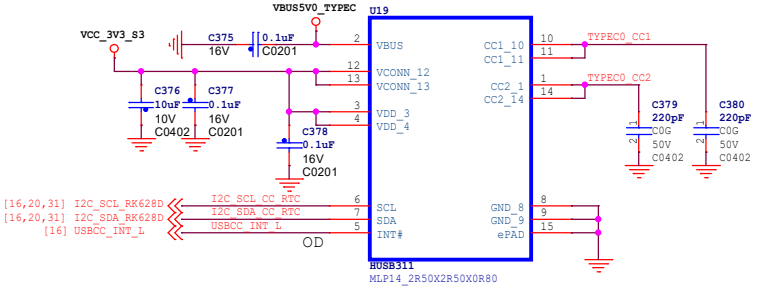


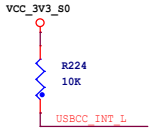




DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	29.USB3.0 Host				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	29 of 39

Type-C

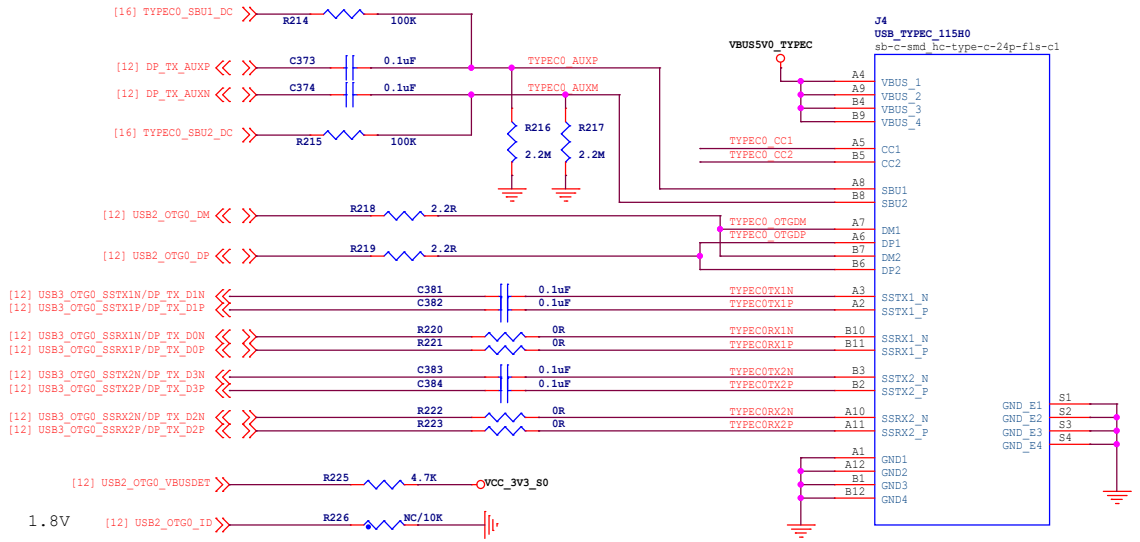


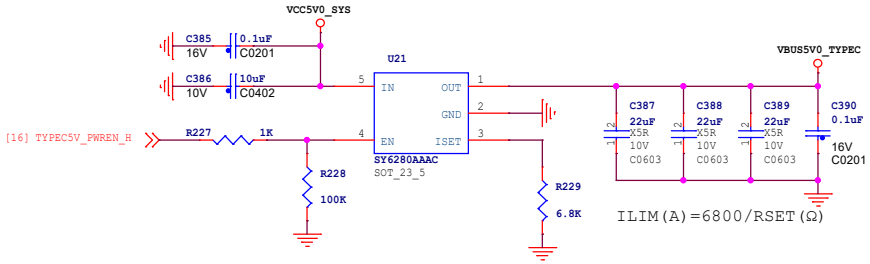


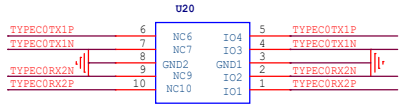
Note:

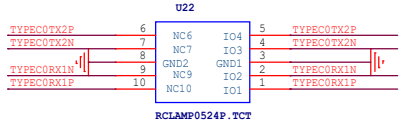
7bit address=0x4E

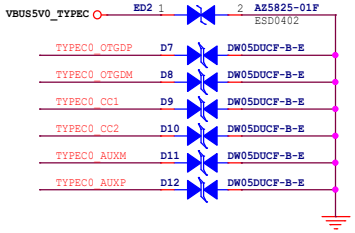
VBUS of HUSB311: 4 to 21 TYP = 5V
VDD of HUSB311: 3 to 5.5 TYP = 3.3V
VCONN of HUSB311: 3 to 5.5











DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	30.Type-C				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	30 of 39

Description:

24Mhz Crystal Selection:

Selection 1:

Independent 24MHz crystal.
Applicable application scenarios:
1.Application scenarios without HDMI_TX and GVI_TX.

Selection 2:

24 MHz clock provided by RKSoc is used for OSC_ IN.
Applicable application scenarios:
1.All application scenarios.

[9] REF_CLK2_OUT C394 100pF C0402 C0G 50V RK628D_OSCIN; C393 18pF C0402 C0G 50V; TP29 TP_0.7 RK628D_OSCOUT

Source of SOC_CLKout_24Mhz
Such as:

RK3288	PIN M23 -TEST_CLKO
RK3399	PIN U28 -TEST_CLKO

Description:

RK628D
PCB Footprint:
BGA144 8*8mm
0.65pitch

Description:

Application 1

Connect to RK CPU

HDMI_RX Signal

[32] HDMI_HPD — HDMIRX_HPD
[32] HDMI_CEC — HDMIRX_CEC
[32] I2C_SDA_HDMI — HDMI_RX_SDA
[32] I2C_SCL_HDMI — HDMI_RX_SCL
[32] HDMI_TXCP — HDMIRX_CLKP
[32] HDMI_TXCN — HDMIRX_CLKN
[32] HDMI_TX0P — HDMIRX_D0P
[32] HDMI_TX0N — HDMIRX_D0N
[32] HDMI_TX1P — HDMIRX_D1P
[32] HDMI_TX1N — HDMIRX_D1N
[32] HDMI_TX2P — HDMIRX_D2P
[32] HDMI_TX2N — HDMIRX_D2N

Note:

HDMI Signal:
Differential routing
Impedance 100ohm

Description:

Application 2

Connect to RK CPU

RGB_RX Signal

Description:

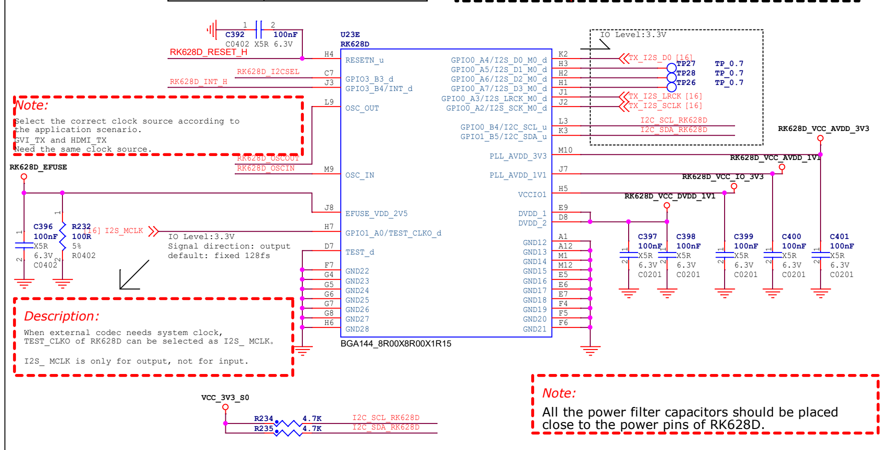
Connect to RK CPU

[16] RK628D_PWR_EN_H — 3.3V — RK628D Power Control
[16] RK628D_RESET_H — 3.3V — RK628D Reset
[16] RK628D_INT_H — 3.3V — RK628D INT
[16,20,30] I2C_SDA_RK628D — 3.3V — RK628D I2C Control
[16,20,30] I2C_SCL_RK628D — 3.3V
[16,32] RK628D_Plugin_DET — 3.3V — HDMI_Plugin_DET

I2C address configuration:

I2C_SEL	I2C_ADDR
0	7'b1010000
1	7'b1010001

Description:
I2C address can be changed by resistance.
GPIO3_B3 Pull-up or drop-down.

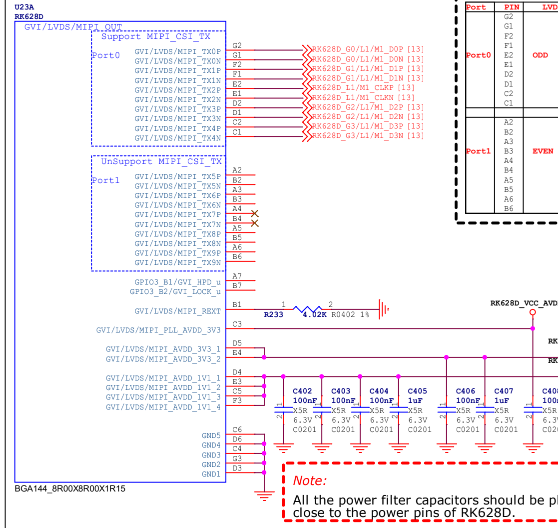


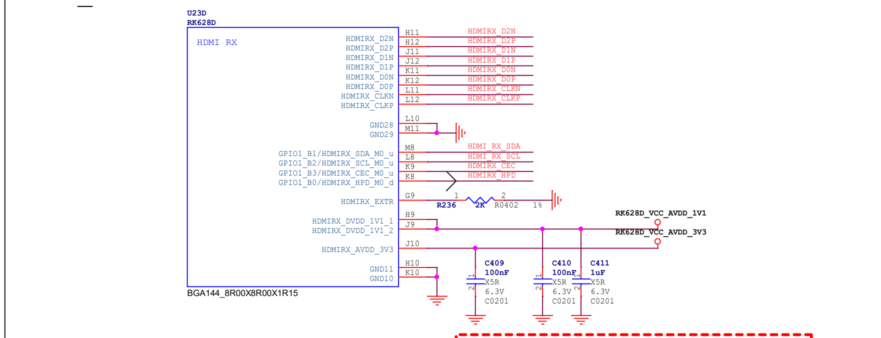
GVI/LVDS/MIPI_DSI/MIPI_CSI_TX

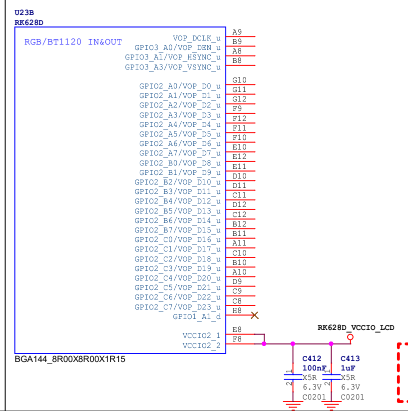
Description:

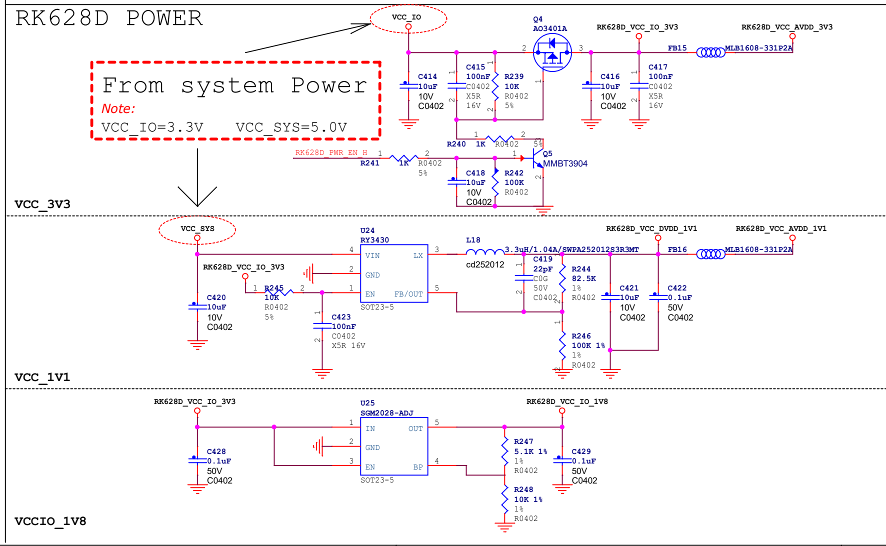
LVDS/MIPI/GVI Signal relationship:

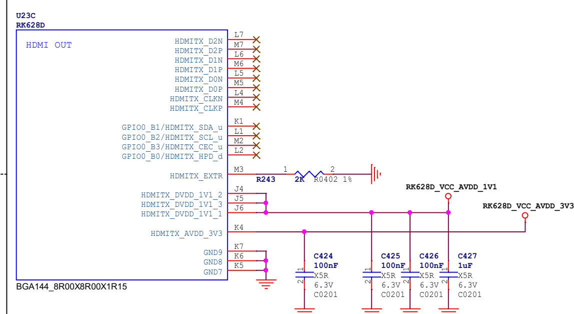
Port	PIN	LVDS Mode		MIPI DSI TX Mode	GVI Mode	MIPI CSI TX
Port0	G2	LVDS0_D0P	ODD	Left	DSI0_D0P	GVI_D0P	CSI0_D0P
	G1	LVDS0_D0N			DSI0_D0N	GVI_D0N	CSI0_D0N
	F2	LVDS0_D1P			DSI0_D1P	GVI_D1P	CSI0_D1P
	F1	LVDS0_D1N			DSI0_D1N	GVI_D1N	CSI0_D1N
	E2	LVDS0_CLKP			DSI0_CLKP		CSI0_CLKP
	E1	LVDS0_CLKN			DSI0_CLKN		CSI0_CLKN
	D2	LVDS0_D2P			DSI0_D2P	GVI_D2P	CSI0_D2P
	D1	LVDS0_D2N			DSI0_D2N	GVI_D2N	CSI0_D2N
	C2	LVDS0_D3P			DSI0_D3P	GVI_D3P	CSI0_D3P
	C1	LVDS0_D3N			DSI0_D3N	GVI_D3N	CSI0_D3N
Port1	A2	LVDS1_D0P	EVEN	Right	DSI1_D0P	GVI_D4P	NC
	B2	LVDS1_D0N			DSI1_D0N	GVI_D4N	
	A3	LVDS1_D1P			DSI1_D1P	GVI_D5P	
	B3	LVDS1_D1N			DSI1_D1N	GVI_D5N	
	A4	LVDS1_CLKP			DSI1_CLKP		
	B4	LVDS1_CLKN			DSI1_CLKN		
	A5	LVDS1_D2P			DSI1_D2P	GVI_D6P	
	B5	LVDS1_D2N			DSI1_D2N	GVI_D6N	
	A6	LVDS1_D3P			DSI1_D3P	GVI_D7P	
	B6	LVDS1_D3N			DSI1_D3N	GVI_D7N	







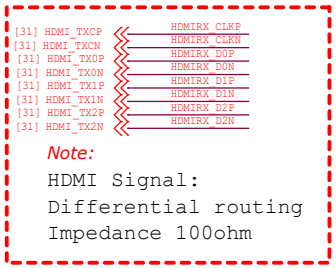


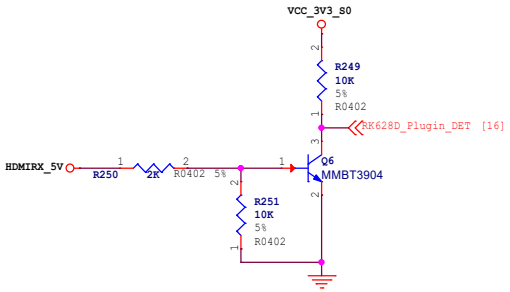


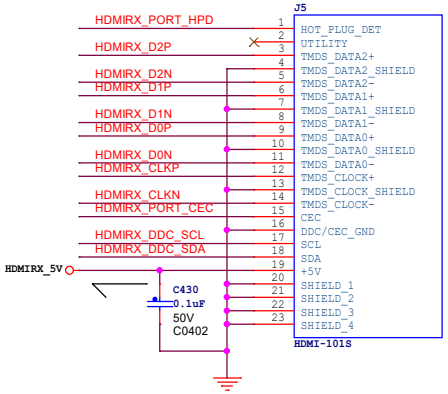
Note:
All the power filter capacitors should be placed close to the power pins of RK628D.

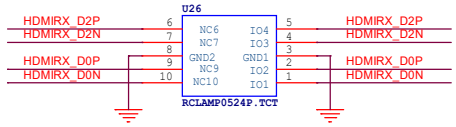
DshanPI-A1	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	31.RK628D Part				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	31 of 39

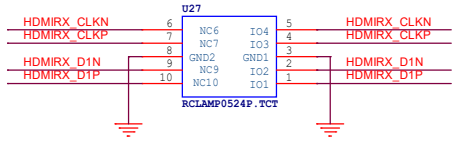
HDMI IN Function

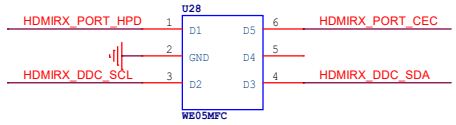


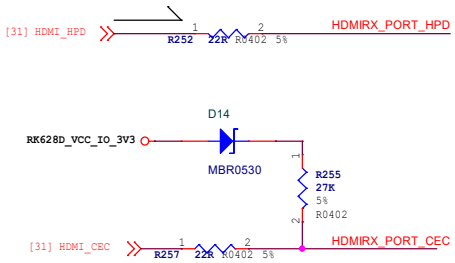


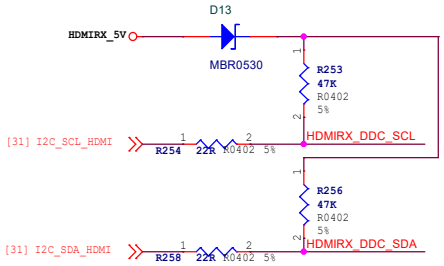












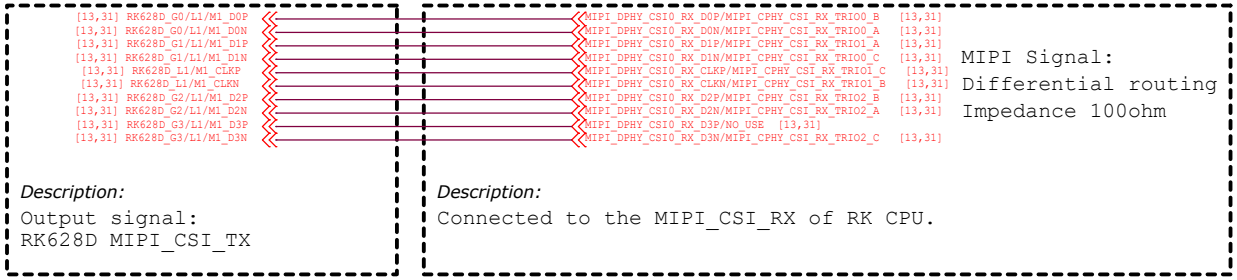
Description:

Default state:HDMIRX_HPD =0, RK628D_Plugin_DET=1.

When connecting the HDMI cable, RK628D_Plugin_DET will be pulled down(RK628D_Plugin_DET=0).

The RK CPU will detect low level(RK628D_Plugin_DET=0),
then RK CPU control RK628D by I2C signal,HDMIRX_HPD/HDMIRX_PORT_HPD will be set to 1.

MIPI_CSI_TX & I2S_TX

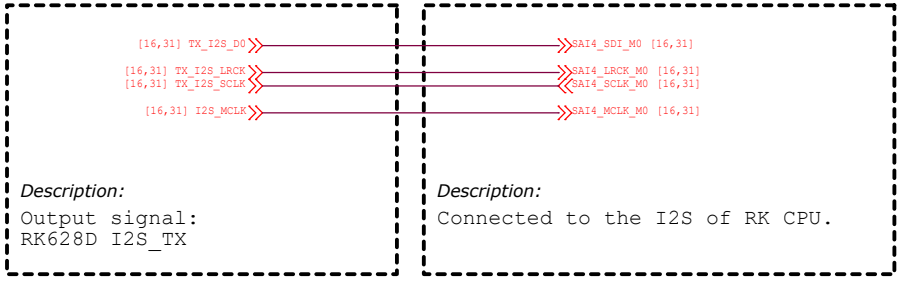


Description:

Output signal:
RK628D MIPI_CSI_TX

Description:

Connected to the MIPI_CSI_RX of RK CPU.



Description:

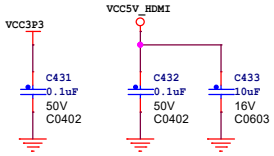
Output signal:
RK628D I2S_TX

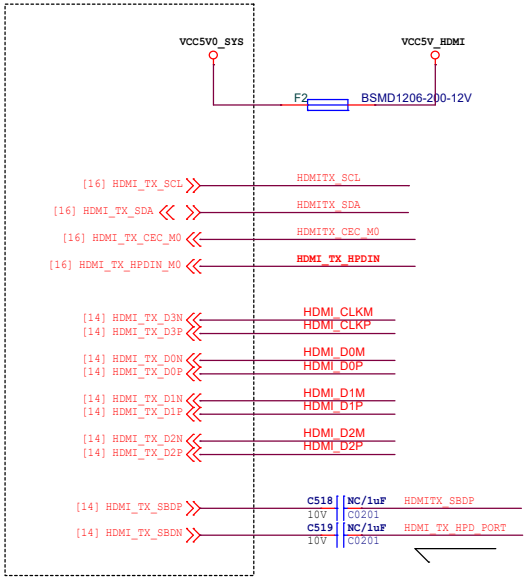
Description:

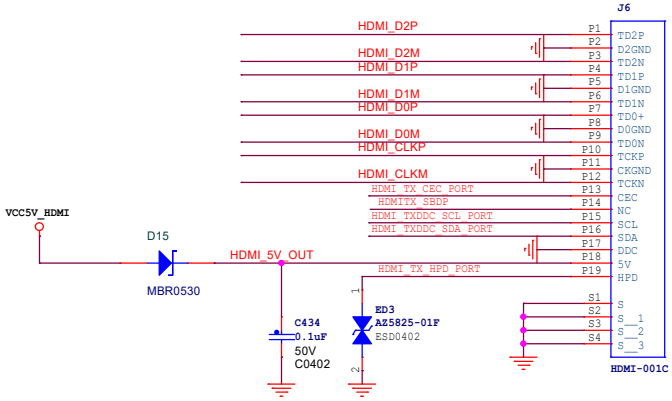
Connected to the I2S of RK CPU.

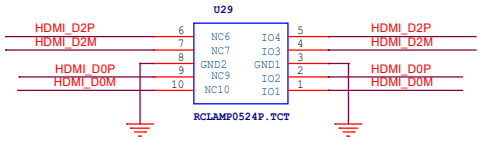
DshanPI-A1 AI Education V1 / Vanxoak 100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	32.HDMI IN				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	32 of 39

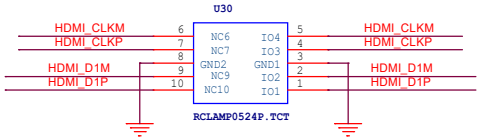
HDMI 2.0

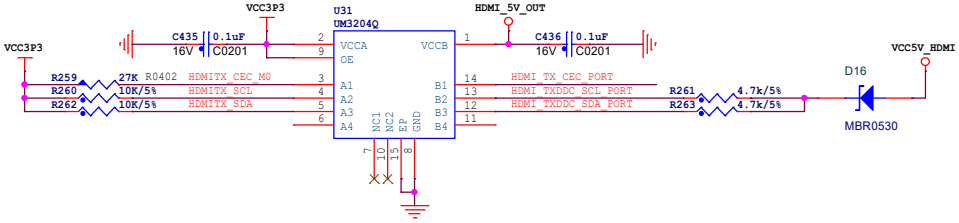


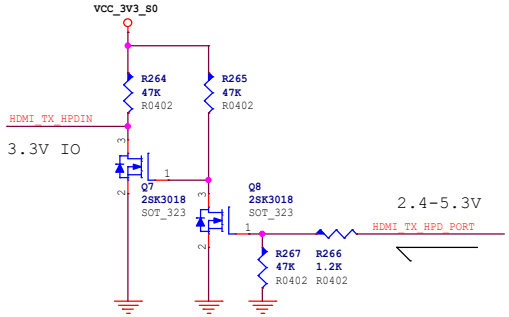


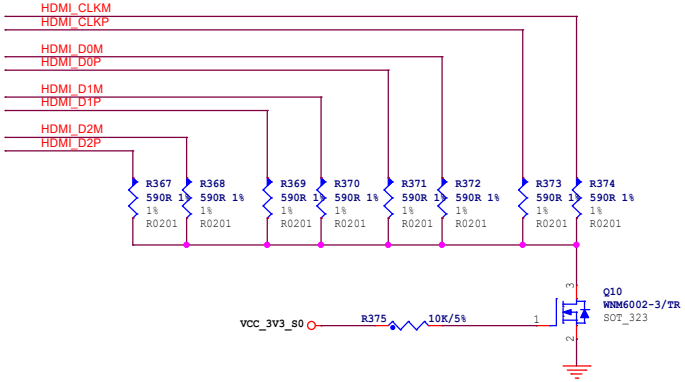






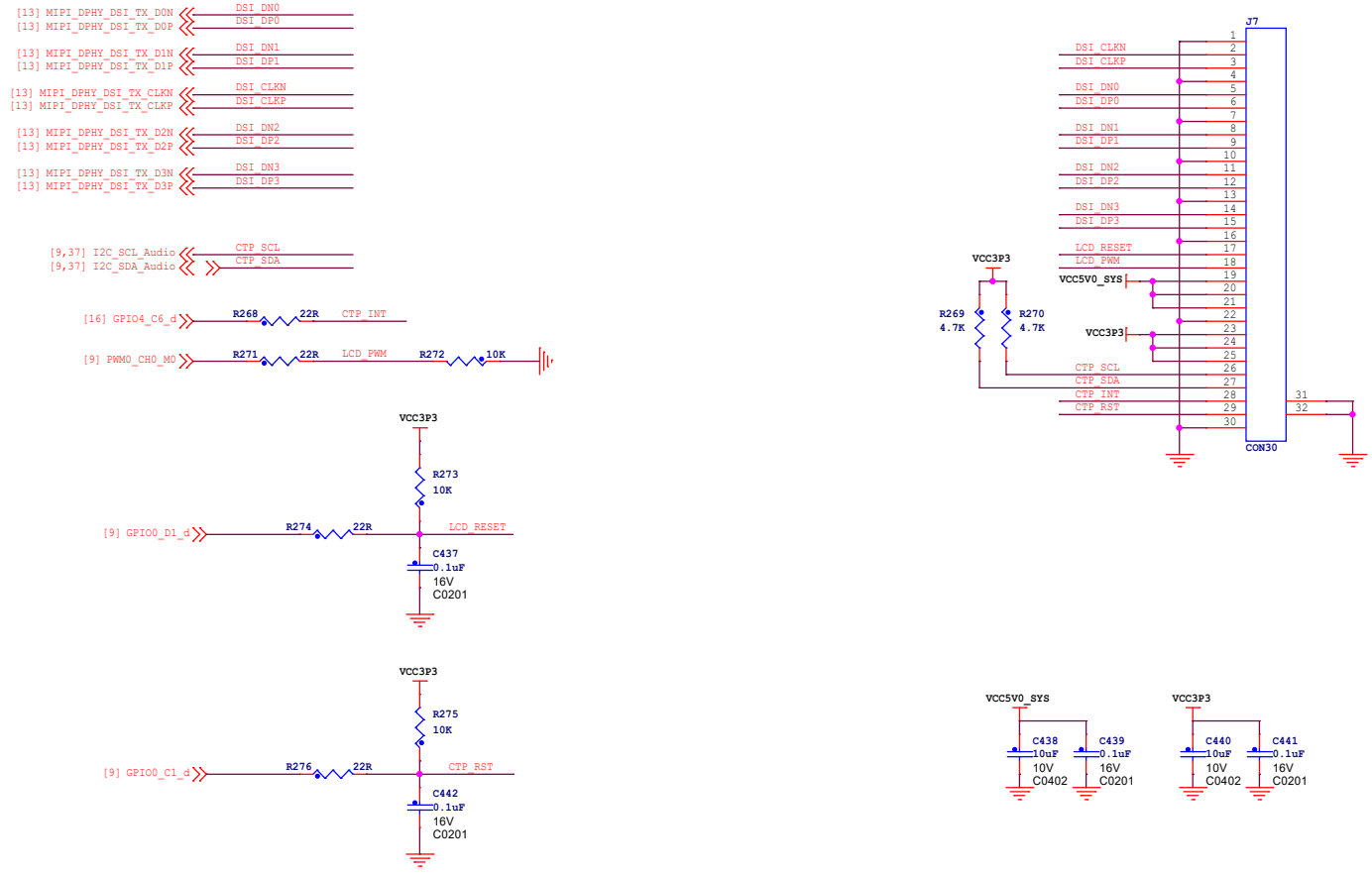






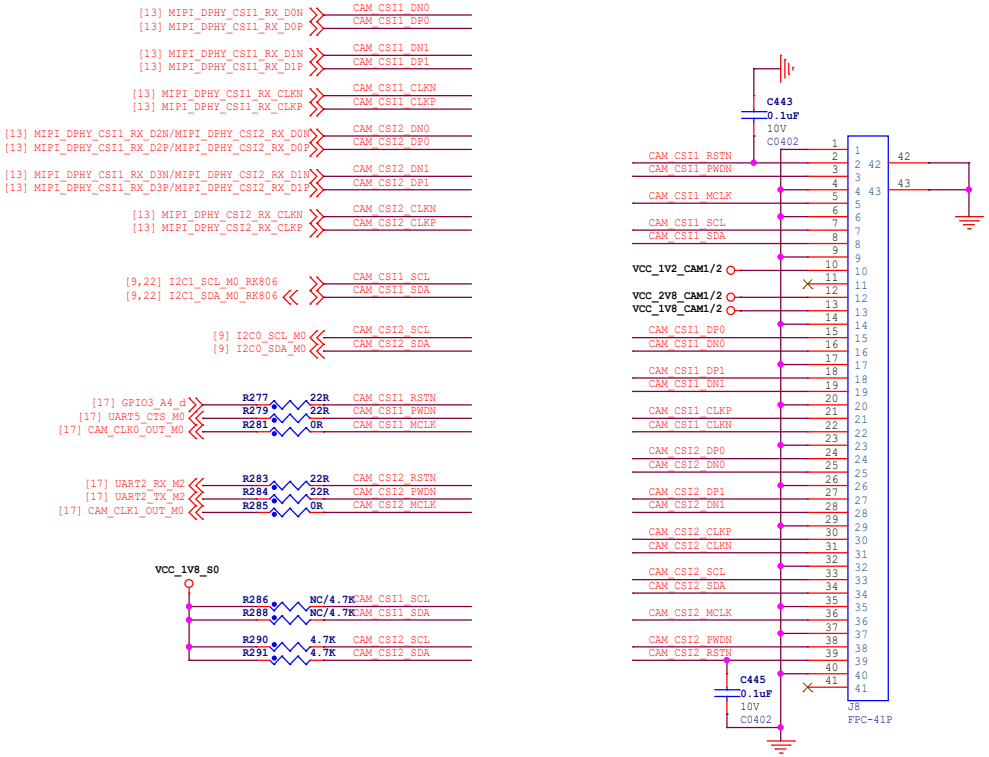
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	33.HDMI OUT				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	33 of 39

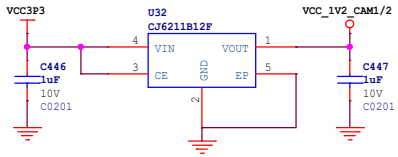
MIPI DSI

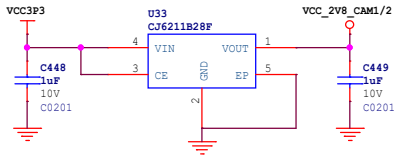


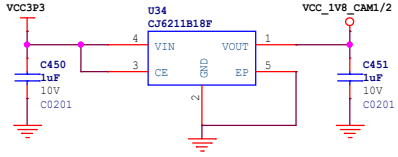
DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	34.MIPI DSI				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	34 of 39

MIPI CSI1/2

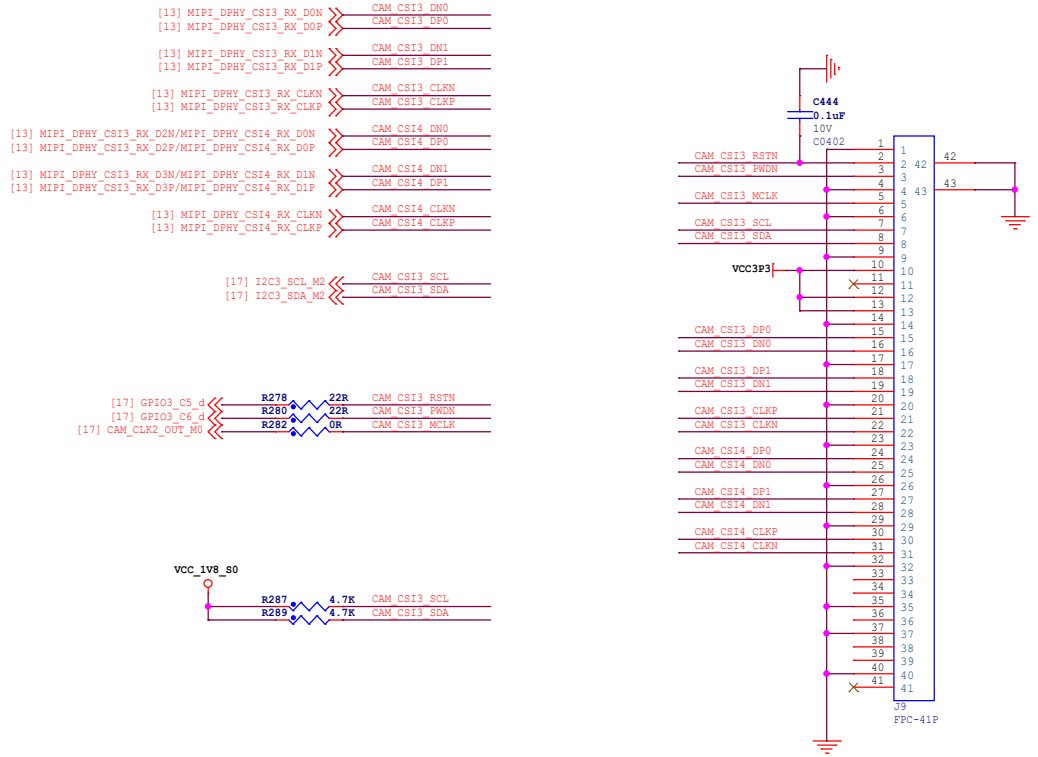






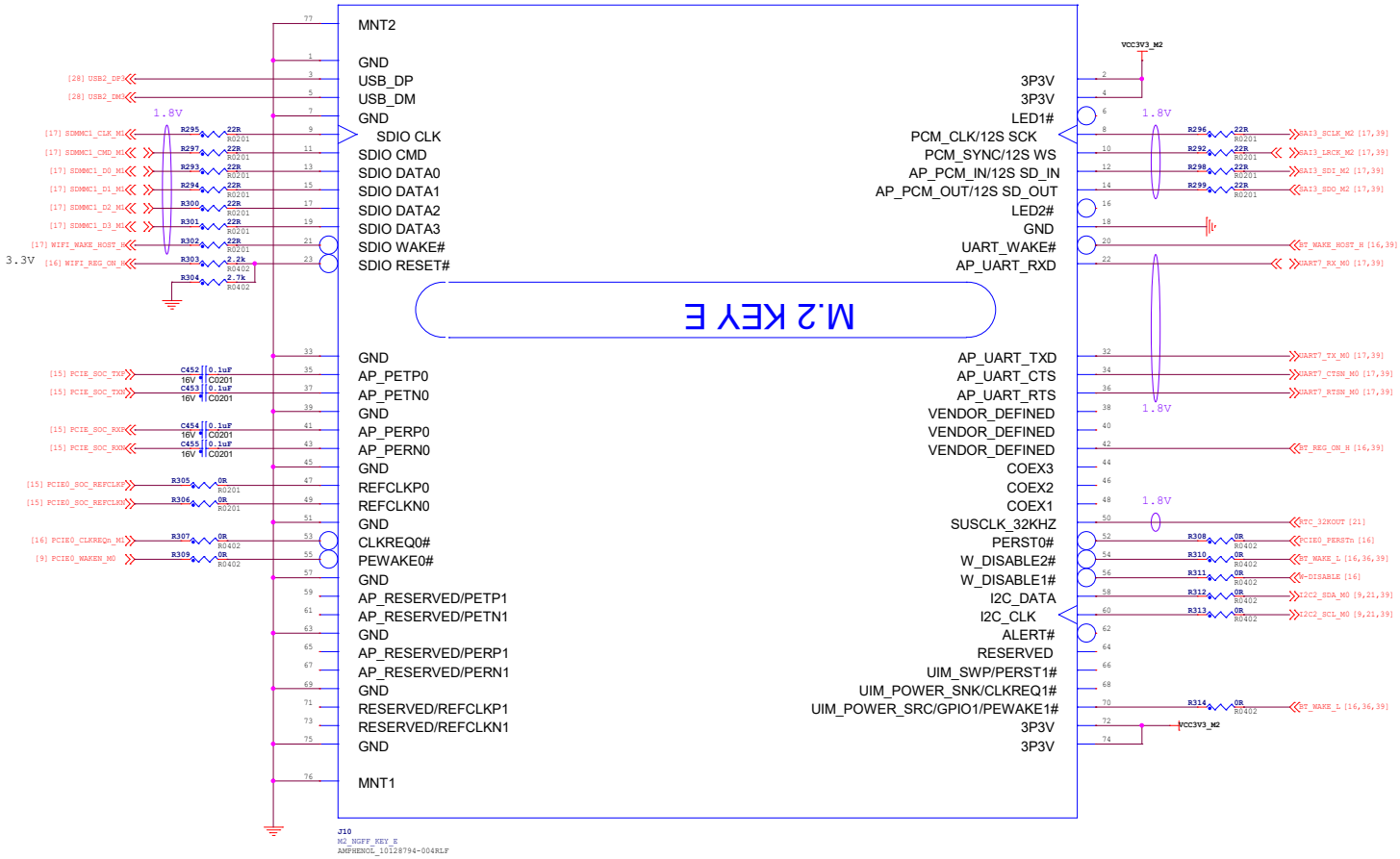


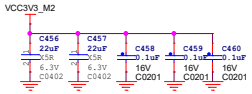
MIPI CSI3/4

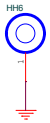


DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	35.MIPI CSI				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	35 of 39

M.2-E Key

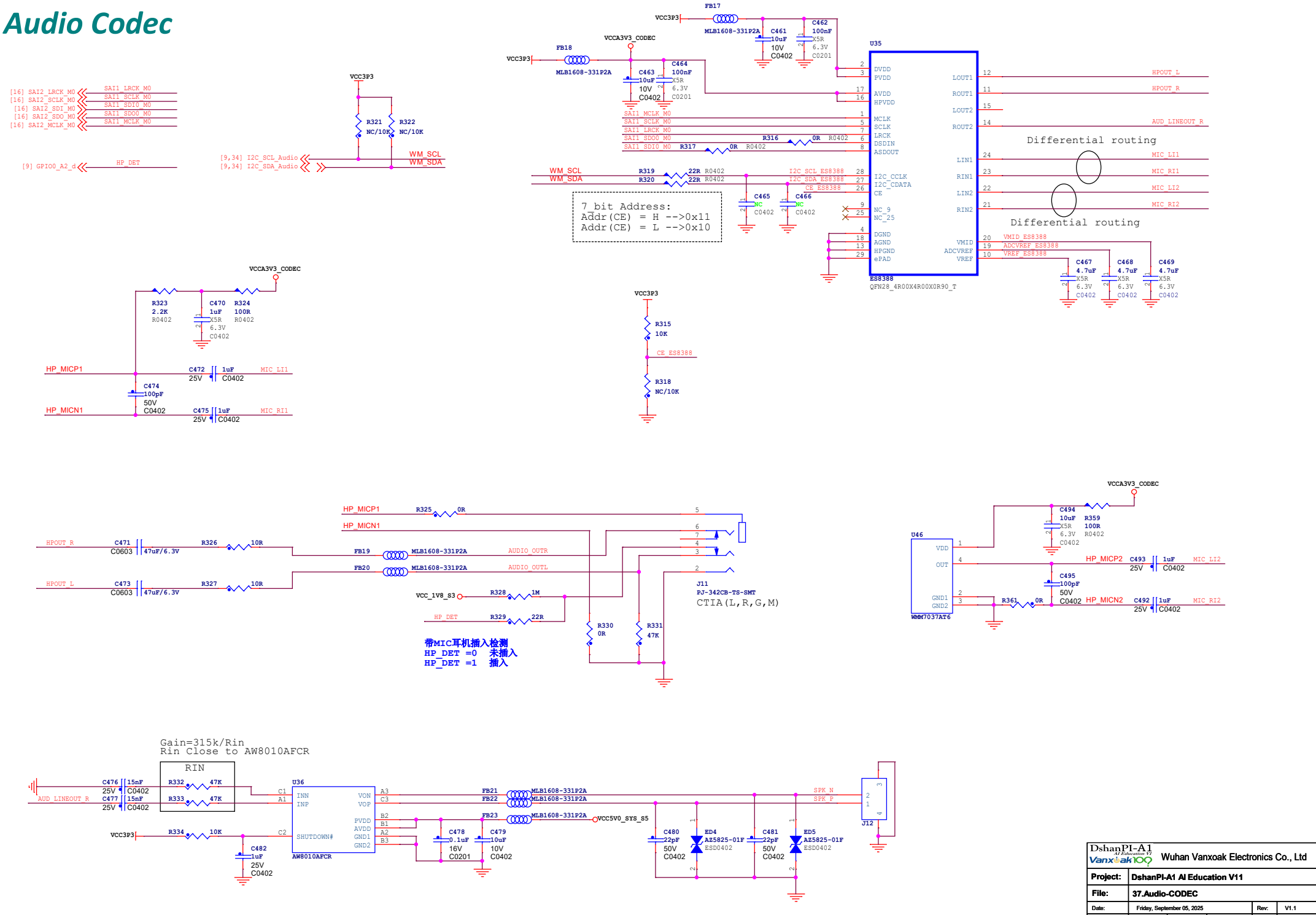






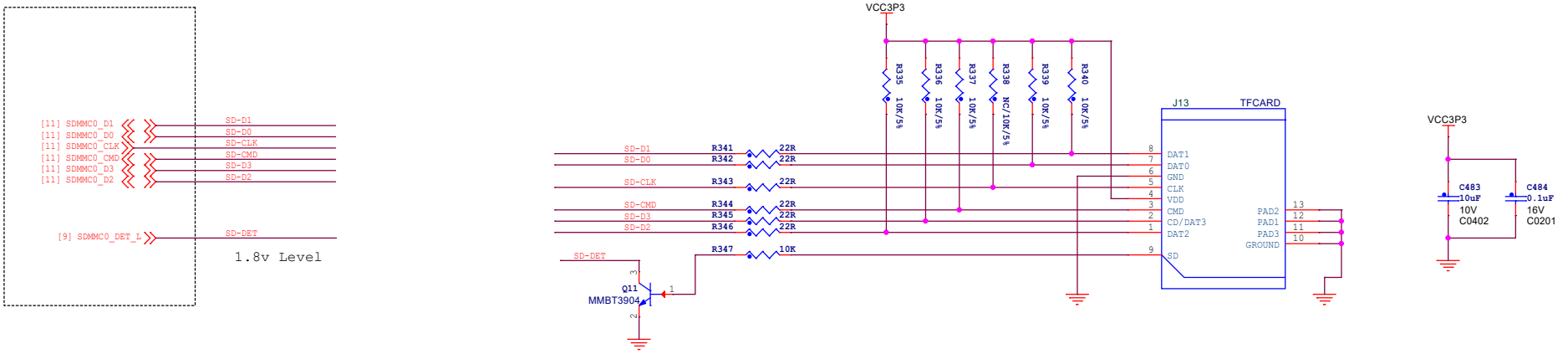
DshanPI-A1 / Varx Oak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	36.M.2-E KEY				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	36 of 39

Audio Codec

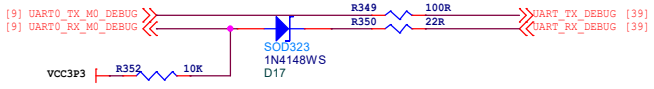


DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	37.Audio-CODEC				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	37 of 39

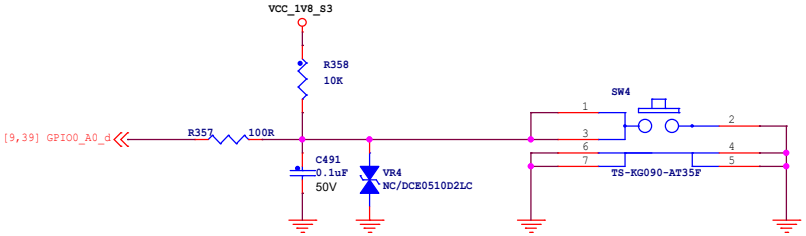
TF CARD



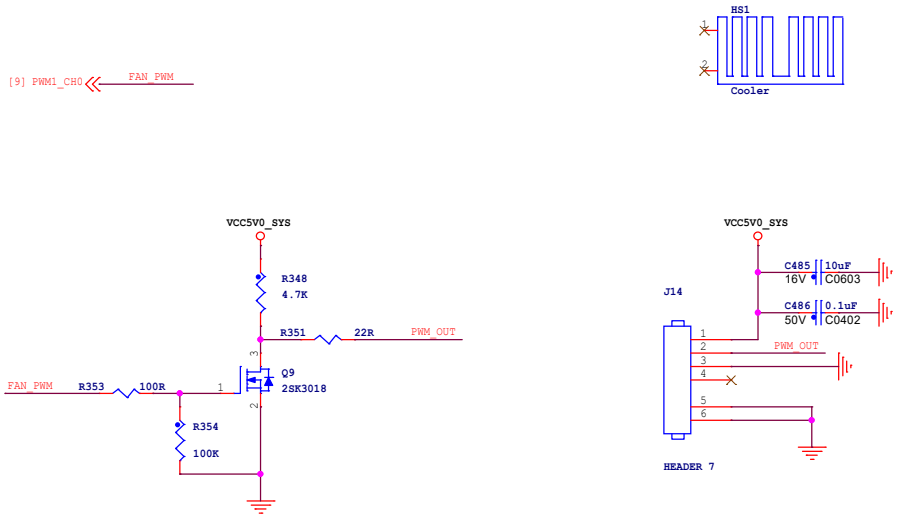
UART DEBUG



KEY

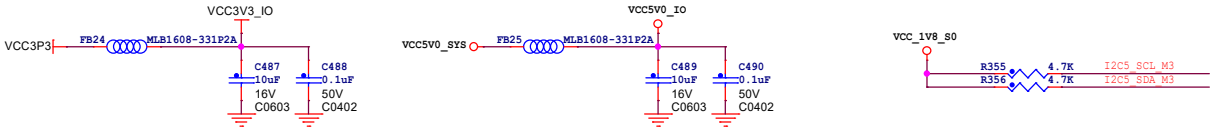


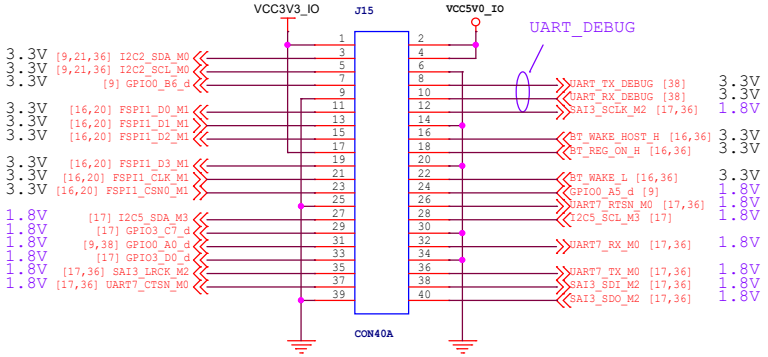
FAN



DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	38.TF Card/Debug/FAN/KEY				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	38 of 39

Expansion Interface





DshanPI-A1 AI Education V1 / Vanxoak100	Wuhan Vanxoak Electronics Co., Ltd				
Project:	DshanPI-A1 AI Education V11				
File:	39.Expansion Interface				
Date:	Friday, September 05, 2025			Rev:	V1.1
Designed by:	Cao Jun	Reviewed by:	<Checker>	Sheet:	39 of 39