A133 User Manual

Revision 1.6

Jan. 18, 2023

Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DECLARATION

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF ALLWINNER TECHNOLOGY ("ALLWINNER"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF ALLWINNER AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE PURCHASED PRODUCTS, SERVICES AND FEATURES ARE STIPULATED BY THE CONTRACT MADE BETWEEN ALLWINNER AND THE CUSTOMER. PLEASE READ THE TERMS AND CONDITIONS OF THE CONTRACT AND RELEVANT INSTRUCTIONS CAREFULLY BEFORE USING, AND FOLLOW THE INSTRUCTIONS IN THIS DOCUMENTATION STRICTLY. ALLWINNER ASSUMES NO RESPONSIBILITY FOR THE CONSEQUENCES OF IMPROPER USE(INCLUDING BUT NOT LIMITED TO OVERVOLTAGE, OVERCLOCK, OR EXCESSIVE TEMPERATURE).

THE INFORMATION FURNISHED BY ALLWINNER IS PROVIDED JUST AS A REFERENCE OR TYPICAL APPLICATIONS, ALL STATEMENTS, INFORMATION, AND RECOMMENDATIONS IN THIS DOCUMENT DO NOT CONSTITUTE A WARRANTY OF ANY KIND, EXPRESS OR IMPLIED. ALLWINNER RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE.

NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF ALLWINNER. THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. ALLWINNER SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. ALLWINNER SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Revision History

Revision	Date	Description
1.0	Jul.07, 2020	Initial release version
1.1	Jul.14, 2020	1. Modify the maximum display resolution from 1080p to 1920 x 1200 2. Delete the limit on the minimum display resolution
1.2	Jan.19, 2021	**Chapter10 Interfaces** Modify the PL voltage mode in section 10.6.6.11.
1.3	July.27, 2021	1. Modify the register description of CPUX Configuration in section 3.2.4 and 3.2.6. 2. Add the BMODE select bit in section 3.9.6.9. 3. Adjust the main frequency parameters in the section 2.2.1.
1.4	March 28, 2022	Add UART FIFO depth in section 2.2.11.3 and section 10.2.1
1.5	Jan. 15, 2023	1. Update some specifications in section 2.2.3.2, section 5.1.1, section 2.2.8.1, and section 6.1.1 2. Update some descriptions in **Table 10-36 EMAC RMII Pin List** and **Table 10-37 EMAC Clock Characteristics**. 3. Update figures in section 2.3 4. Add LPDDR2 support.
1.6	Jan. 18, 2023	1. Add R_Timer contents.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 1 About This Document 5
1.1. Purpose 5
1.2. Intended Audience 5
1.3. Symbol Conventions 5
1.4. Notes 6
1.4.1. Register Attributes 6
1.4.2. Reset Value Conventions 6
1.4.3. Numerical System 6
1.5. Acronyms and Abbreviations 7

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 1 About This Document

1.1. Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module about A133. For details about the interface timings and related parameters, the pins, pin usages, performance parameters, and package dimension, refer to the ***Allwinner A133 Datasheet***.

1.2. Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

1.3. Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1.4. Notes

1.4.1. Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear. Writing 1 has no effect
R/W1C	Read/Write 1 to Clear. Writing 0 has no effect
R/W1S	Read/Write 1 to Set. Writing 0 has no effect
W	Write Only

1.4.2. Reset Value Conventions

In the register definition tables:
If other column value in a bit or multiple bits row is "/", that this bit or these multiple bits are unused.
If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

1.4.3. Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency,data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200, 0x79	Address or data in hexadecimal
0b	0b010, 0b00 000 111	Data or sequence in binary(register description is excluded.)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

X	00X, XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

1.5. Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Pitch Ball Grid Array
FEL	Fireware Exchange Launch

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LFBGA	Low Profile Fine Pitch Ball Grid Array
LRADC	Low Rate Analog to Digital Converter
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Sychronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 2 Product Description 12
2.1. Overview 12
2.2. Features 12
2.2.1. CPU Architecture 12
2.2.2. GPU Architecture 12
2.2.3. Memory Subsystem 13
2.2.4. Video Engine 14
2.2.5. Video and Graphics 15
2.2.6. System Peripherals 15
2.2.7. Image Input 18
2.2.8. Video Output 19
2.2.9. Audio Subsystem 19
2.2.10. Security Engine 20
2.2.11. External Peripherals 21
2.2.12. Package 25
2.3. Block Diagram 26

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 2- 1. A133 System Block Diagram 26
Figure 2- 2. A133 Tablet Solution Diagram 27

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 2 Product Description

2.1. Overview

A133 is a high-performance quad-core application processor for tablets. The application processor incorporates a high efficient 64-bit quad-core Cortex™-A53 processor, advanced Imagination PowerVR GE8300 GPU, 13M camera ISP, and high-definition 4K@30fps video decoder. Rich memory interfaces (DDR4, DDR3, DDR3L, LPDDR3, LPDDR4, eMMC, Nand) provide high flexibility to support variant memory configurations.

Lots of high-performance interfaces can get very flexible solution, such as MIPI CSI, MIPI DSI, EMAC, USB, UART, SPI, PWM, TWI, LEDC, etc. A133 processor delivers high-performance computing, low-power consumption, and good multimedia experience for tablets. The Allwinner SDK features high stability and ease of use, supports rapid mass production.

2.2. Features

2.2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 processor@1.5 GHz
- Power-efficient ARM v8 architecture
- 64-bit and 32-bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD (Single Instruction Multiple Data) instruction for acceleration of media and signal processing functions
- VFPv4 Floating Point Unit
- 32 KB L1 Instruction cache and 32 KB L1 Data cache for per CPU
- 512 KB L2 cache shared

2.2.2. GPU Architecture

- Imagination GE8300
- Supports OpenGL ES 1.1/2.0/3.2, Vulkan 1.3, OpenCL 1.2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.2.3. Memory Subsystem

2.2.3.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - SD/eMMC (SMHC0, SMHC2)
  - Nand Flash
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports mandatory upgrade process through SMHC0 and USB
- Supports GPIO pin to select the kind of boot media to boot
- Supports GPADC to select the kind of boot media to boot
- Supports SID (eFUSE) to select the kind of boot media to boot
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

2.2.3.2. SDRAM

- 32-bit LPDDR2/DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 interface
- LPDDR2: clock frequency up to 528 MHz
- DDR3/DDR3L: clock frequency up to 792 MHz
- LPDDR3: clock frequency up to 672 MHz
- DDR4: clock frequency up to 792 MHz
- LPDDR4: clock frequency up to 792 MHz
- Memory capacity up to 4 GB

2.2.3.3. Nand Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals
- Supports SLC/MLC flash and EF-NAND
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0 and Toggle DDR2.0 RAW NAND FLASH

2.2.3.4. SMHC

- Three SD/MMC host controller (SMHC) interfaces
- SMHC0 controls the devices that comply with the Secure Digital (SD3.0)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

  - 4-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - DDR mode 100MHz@1.8V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output (SDIO3.0)
  - 4-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - DDR mode 100MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the Multimedia Card (eMMC 5.1)
  - 8-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - DDR mode 100MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.2.4. Video Engine

2.2.4.1. Video Decoding

- Supports multi-formats video decoder, including:
  - H.265 MP@L5.0: 4K@30fps
  - H.264 BP/MP/HP@L5.1: 4K@30fps
  - VP9: 720p@30fps
  - MPEG-4 SP/ASP: 1080p@60fps
  - MPEG-2 MP/HL: 1080p@60fps
  - MPEG-1 MP/HL: 1080p@60fps
  - VP8: 1080p@60fps
  - AVS/AVS+ JiZhun@L6.0: 1080p@60fps
  - H.263 BP: 1080p@60fps
  - MJPEG: 1080p@60fps
  - VC1 SP/MP/AP: 1080p@30fps

2.2.4.2. Video Encoding

- H.264 BP/MP/HP
- Maximum 16-megapixel (4096 x 4096) resolution for H.264 encoding
- H.264 encoding performance of 1080p@60fps
- MJPEG encoding performance of 1080p@30fps

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.2.5. Video and Graphics

2.2.5.1. Display Engine (DE)

- Output size up to 2048 x 2048
- Four alpha blending channels for main display, three channels for aux display
- Four overlay layers in each channel, and has a independent scaler
- Potter-duff compatible blending operation
- Input format: YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back only for high efficient main display and miracast

2.2.5.2. Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports input/output formats: YUV422 (semi-planar and planar format)/YUV420 (semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

2.2.6. System Peripherals

2.2.6.1. Timer

- The timer module implements the timing and counting functions, which includes Timer0, Timer1, Watchdog and AVS0, AVS1
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factor
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters (AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- 12-bit frequency divider factor
- Pause/Start function

2.2.6.2. R_Timer

- Configurable count clock: for R_Timer0/1/2/3, clock source can be LOSC or OSC. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Supports two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

2.2.6.3. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

2.2.6.4. RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency: 1 kHz
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Supports a calibration function of 32.768 kHz obtained by RC16M clock division
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing power-off information

2.2.6.5. GIC

- Supports 16 Software Generated Interrupts (SGIs), 16 Private Peripheral Interrupts (PPIs) and 160 Shared Peripheral Interrupts (SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.2.6.6. DMA

- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.2.6.7. CCU

- 12 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.2.6.8. Thermal Sensor Controller

- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Three thermal sensors: sensor0 located in the CPU, sensor1 located in the GPU, and sensor2 located in the DDR

2.2.6.9. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control, CP15 control and power on/off control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc
- Including CPU debug control and status register

2.2.6.10. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE, VE, CSI, ISP, G2D parallel address mapping
- Supports DE, VE, CSI, ISP, G2D bypass function independently
- Supports DE, VE, CSI, ISP, G2D prefetch independently
- Supports DE, VE, CSI, ISP, G2D interrupt handing mechanism independently

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.2.6.11. Spinlock

- Provides a hardware synchronization mechanism in multi-core system
- Supports 32 lock units to prevent multi processors from handling the shared data at the same time
- Two kinds of lock status: locked and unlocked
- The lock time of the processor is less than 200 cycles

2.2.6.12. Message Box

- Provides interrupt communication mechanism for on-chip processor
- The communication parties transmit information by a channel
- Interrupt alarm function

2.2.7. Image Input

2.2.7.1. CSI

- Supports 2 MIPI CSI interfaces (one for 4-lane, the other for 2-lane)
- Supports image crop function
- Supports MIPI Version 1.0
- Supports up to 1.0 Gbps/lane
- Maximum video capture resolution up to 8M@30fps (for online mode) or 13M@10fps (for offline mode) or 4*1080p@25fps (for de-interleaver conversion chip)

2.2.7.2. ISP

- Supports one sensor in online mode, or two sensors in offline mode
- Maximum frame rate of 8M@30fps (for online mode) or 13M@10fps (for offline mode)
- Adjustable 3A functions, including automatic exposure (AE), automatic white balance (AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D denoising
- Global tone mapping
- Graphics mirror and flip
- ISP tuning tools for the PC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.2.8. Video Output

2.2.8.1. TCON_LCD

- RGB interface with DE/SYNC mode, up to 1280x720@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- LVDS interface with dual link, up to 1920 x 1200@60fps
- LVDS interface with single link, up to 1366 x 768@60fps
- i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

2.2.8.2. MIPI DSI

- One 4-lane MIPI DSI
- Compliance with MIPI DSI v1.01
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Maximum 1920 x 1200@60fps performance for MIPI DSI
- Supports non-burst mode with sync pulse/sync event, burst mode and command mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports ULPS and escape modes
- Hardware checksum capabilities

2.2.9. Audio Subsystem

2.2.9.1. Audio Codec

- Two audio digital-to-analog (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95±3dB SNR
- Two audio analog-to-digital (ADC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95±3dB SNR
- Two audio output interfaces:
  - One stereo headphone output (HPOUTL and HPOUTR)
  - One differential line output (LINEOUTLP and LINEOUTLN)
- Two audio input interfaces:
  - Two differential microphone inputs (MICIN1P/N and MICIN2P/N)
- Two low-noise analog microphone bias output
- Supports Dynamic Range Controller adjusting the DAC playback and ADC capture

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- DMA and Interrupt support

2.2.9.2. I2S/PCM

- Four I2S/PCM interfaces
- Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode
- I2S mode supports 8 channels, and 32-bit/192 kHz sample rate
- I2S and TDM modes support maximum 16 channels, and 32-bit/96 kHz sample rate

2.2.9.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.2.9.4. OWA

- One OWA TX
- Compliance with S/PDIF interface
- IEC-60958 transmitter functionality
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit, 20-bit and 24-bit data formats

2.2.10. Security Engine

2.2.10.1. Crypto Engine (CE)

- Encryption and decryption algorithms implemented by using hardware, including AES, XTS-AES, DES, TDES, SM4
  - ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC, GCM mode for AES
  - 128/192/256-bit key for AES
  - 256-bit, 512-bit key for XTS-AES
  - ECB, CBC, CTR, CBC-MAC mode for DES
- Hash tamper proofing algorithms implemented by using hardware, including MD5, SHA, SM3, HMAC
  - SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - HMAC-SHA1, HMAC-SHA256 for HMAC
  - Supports hardware padding

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

  - Supports multi-package mode
- Signature and verification algorithms implemented by using hardware, including RSA, ECC
  - RSA supports 512/1024/2048/3072/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Hardware random number generator: PRNG, TRNG, HASH+DRBG
- Security strategy and system feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, which can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
  - Supports task chain mode for each request. Task or task chain are executed at request order
  - 8 scatter group (sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, they do not know the existence of each other
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other

2.2.10.2. Security ID

- Supports 2 Kbits eFUSE for chip ID and security application
- EFUSE has secure zone and non-secure zone
- Supports a SRAM to backup fuse information

2.2.10.3. Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

2.2.10.4. Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.2.11. External Peripherals

2.2.11.1. USB

- One USB 2.0 OTG (USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
- Up to 10 User-Configurable Endpoints (EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
- Supports (8 KB+64 Bytes) FIFO for all EPs (including EP0)
- Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode

• One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device

2.2.11.2. EMAC

- One EMAC interface
- Compliant with IEEE 802.3-2002 standard
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.2.11.3. UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, S_UART)
- UART0, S_UART: 2-wire; UART1, UART2, UART3, UART4: 4-wire
- Two separate FIFOs: RX FIFO and TX FIFO
  - Each of them is 64 bytes (For UART0, UART3, UART4, and S_UART)
  - Each of them is 256 bytes (For UART1 and UART2)
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.2.11.4. SPI

- Up to 3 SPI controllers (SPI0, SPI1, SPI2)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to 32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

2.2.11.5. Two Wire Interface (TWI)

- Up to 6 TWI controllers (TWI0, TWI1, TWI2, TWI3, S_TWI0, S_TWI1)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

2.2.11.6. PWM

- 5 PWM channels (PWM0~3, S_PWM)
- PWM0~3 channels divide to 2 PWM pairs: PWM01 pair, PWM23 pair
- S_PWM channel has the single channel characteristics of PWM module, and has no pair function
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveforms: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~24 MHz/100 MHz
- Various duty-cycle: 0%~100%

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input
- Supports PWM group mode(4 groups), the starting phase of each channel in same group is configurable

2.2.11.7. Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: 1.8 V, power reference voltage: 1.35 V, analog input and detected voltage range: 0 to LEVELB (the maximum value is 1.266 V)

2.2.11.8. General Purpose ADC (GPADC)

- One GPADC input channel
- 12-bit resolution and 8-bit effective SAR type A/D converter
- Power reference voltage: 1.8 V, analog input voltage range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Outbreak conversion mode

2.2.11.9. LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable input high/low level width of LED
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configurable mode
- Maximum 1024 LEDs serial connect

2.2.11.10. CIR Transmitter (CIR_TX)

- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports DMA shake and wait mode
- 128 bytes FIFO for data buffer

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.2.11.11. CIR Receiver (CIR_RX)

- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.2.12. Package

- LFBGA346 balls, 0.5 mm ball pitch, 0.3 mm ball size, 12 mm x 12 mm body

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2.3. Block Diagram

Figure 2-1 shows the system block diagram of the A133.

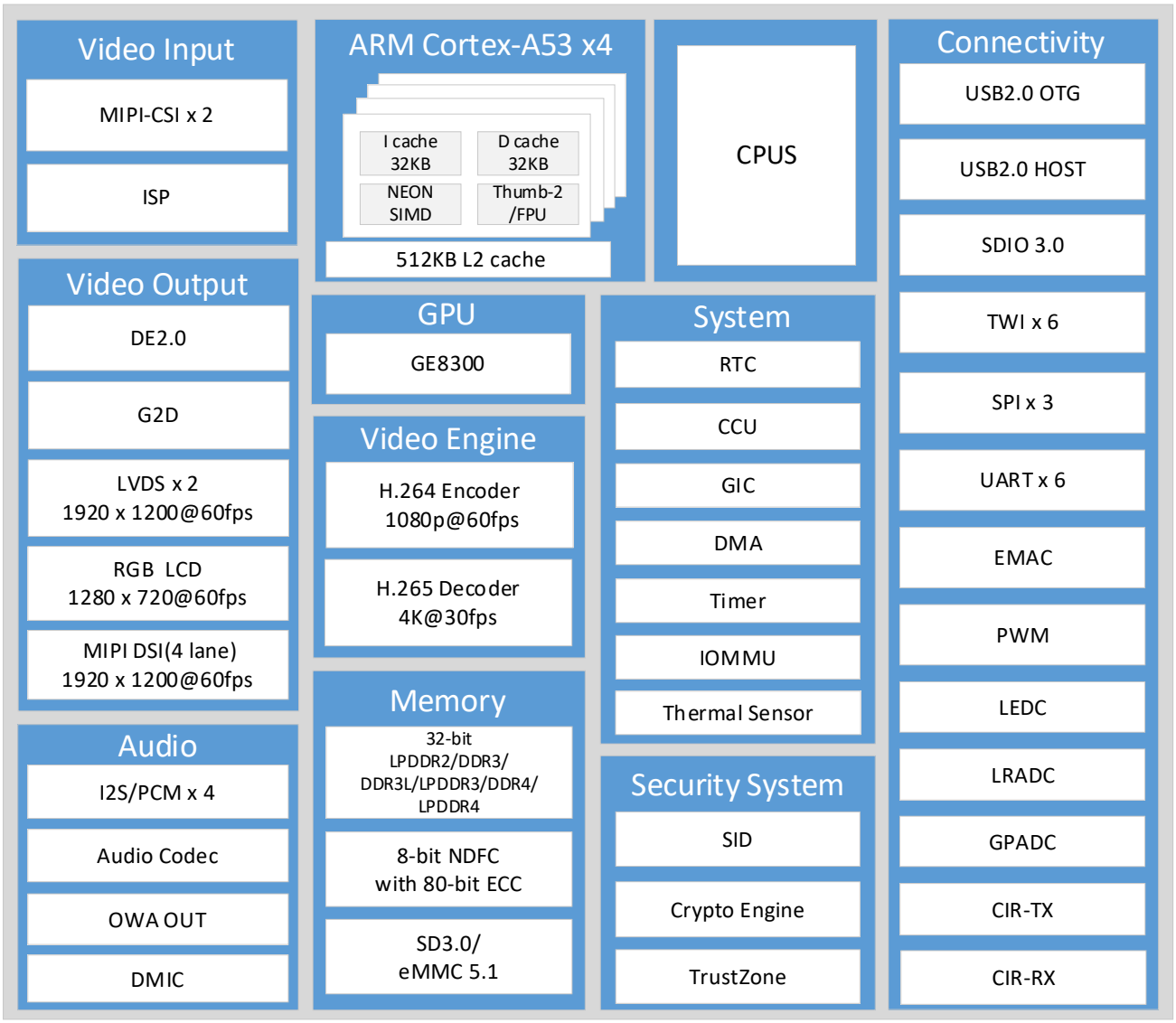


Figure 2- 1. A133 System Block Diagram

Figure 2-2 shows the tablet solution diagram of the A133.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

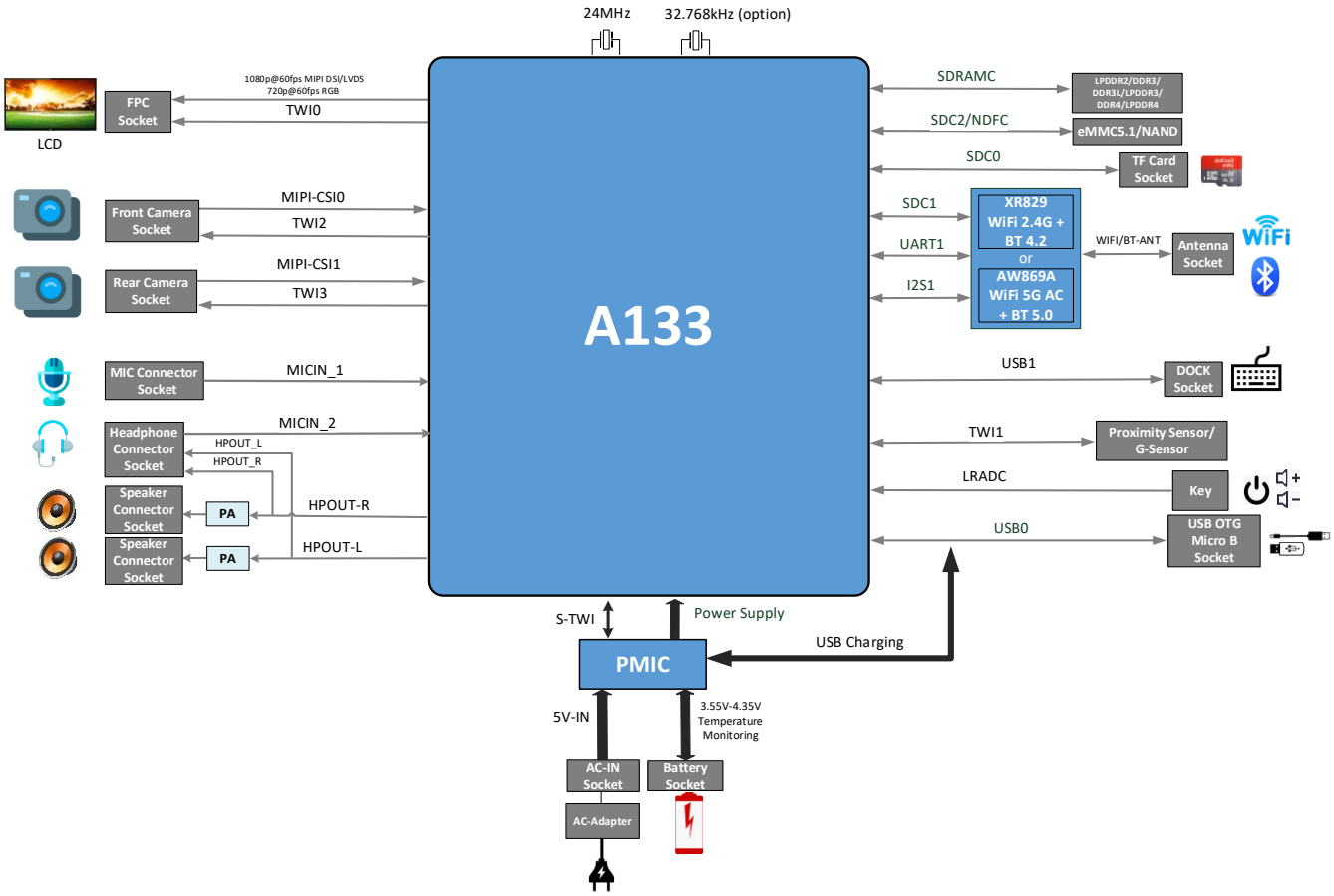


Figure 2- 2. A133 Tablet Solution Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 3 System 34
3.1. Memory Mapping 34
3.2. CPUX Configuration 38
3.2.1. Overview 38
3.2.2. Operations and Functional Descriptions 38
3.2.3. Cluster 0 Configuration Register List 40
3.2.4. Cluster 0 Configuration Register Description 40
3.2.5. CPU Subsystem Control Register List 48
3.2.6. CPU Subsystem Control Register Description 48
3.3. CCU 54
3.3.1. Overview 54
3.3.2. Operations and Functional Descriptions 54
3.3.3. Programming Guidelines 62
3.3.4. Register List 66
3.3.5. Register Description 69
3.4. BROM System 140
3.4.1. Overview 140
3.4.2. Operations and Functional Descriptions 140
3.5. System Configuration 146
3.5.1. Overview 146
3.5.2. Operations and Functional Descriptions 146
3.6. Timer 147
3.6.1. Overview 147
3.6.2. Block Diagram 148
3.6.3. Operations and Functional Descriptions 148
3.6.4. Programming Guidelines 151
3.6.5. Register List 152
3.6.6. Register Description 153
3.7. R_Timer 161
3.7.1. Overview 161
3.7.2. Block Diagram 161
3.7.3. Operations and Functional Descriptions 161
3.7.4. Programming Guidelines 163
3.7.5. Register List 163
3.7.6. Register Description 164
3.8. High Speed Timer 172
3.8.1. Overview 172
3.8.2. Block Diagram 172
3.8.3. Operations and Functional Descriptions 172

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.8.4. Programming Guidelines 174
3.8.5. Register List 175
3.8.6. Register Description 175
3.9. GIC 181
3.9.1. Interrupt Source 181
3.10. DMA 186
3.10.1. Overview 186
3.10.2. Block Diagram 186
3.10.3. Operations and Functional Descriptions 187
3.10.4. Programming Guidelines 196
3.10.5. Register List 197
3.10.6. Register Description 197
3.11. Thermal Sensor Controller 209
3.11.1. Overview 209
3.11.2. Block Diagram 209
3.11.3. Operations and Functional Descriptions 209
3.11.4. Programming Guidelines 211
3.11.5. Register List 212
3.11.6. Register Description 213
3.12. IOMMU 220
3.12.1. Overview 220
3.12.2. Block Diagram 220
3.12.3. Operations and Functional Descriptions 221
3.12.4. Programming Guidelines 229
3.12.5. Register List 230
3.12.6. Register Description 233
3.13. RTC 289
3.13.1. Overview 289
3.13.2. Clock Tree Diagram 289
3.13.3. Operations and Functional Descriptions 290
3.13.4. Programming Guidelines 297
3.13.5. Register List 297
3.13.6. Register Description 298
3.14. Message Box 309
3.14.1. Overview 309
3.14.2. Block Diagram 309
3.14.3. Operations and Functional Descriptions 310
3.14.4. Programming Guidelines 313
3.14.5. Register List 314
3.14.6. Register Description 314
3.15. Spinlock 322
3.15.1. Overview 322
3.15.2. Block Diagram 322
3.15.3. Operations and Functional Descriptions 322
3.15.4. Programming Guidelines 324

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.15.5. Register List 325
3.15.6. Register Description 326

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 3- 1. CPUX Power Domain Block Diagram 39
Figure 3- 2. System Bus Tree 55
Figure 3- 3. Bus Clock Generation 56
Figure 3- 4. Module Clock Generation 57
Figure 3- 5. PLL Distribution 60
Figure 3- 6. Boot Process Diagram 142
Figure 3- 7. Mandatory Upgrade Process 143
Figure 3- 8. USB FEL Process 144
Figure 3- 9. Timer Block Diagram 148
Figure 3- 10. Timer Application Diagram 149
Figure 3- 11. R_Timer Block Diagram 161
Figure 3- 12. R_Timer Application Diagram 162
Figure 3- 13. HSTimer Block Diagram 172
Figure 3- 14. HSTimer Application Diagram 173
Figure 3- 15. HSTimer Initialization Process 174
Figure 3- 16. DMA Block Diagram 186
Figure 3- 17. DMA Typical Application Diagram 187
Figure 3- 18. DMA Descriptor 189
Figure 3- 19. DMA Chain Transfer 191
Figure 3- 20. DMA Transfer Mode 193
Figure 3- 21. DMA Transfer Process 195
Figure 3- 22. Thermal Sensor Controller Block Diagram 209
Figure 3- 23. Thermal Sensor Time Requirement 210
Figure 3- 24. Thermal Sensor Controller Interrupt Source 210
Figure 3- 25. THS Initial Process 211
Figure 3- 26. IOMMU Block Diagram 221
Figure 3- 27. Internal Switch Process 225
Figure 3- 28. VA-PA Switch Process 226
Figure 3- 29. Invalid TLB Address Range 227
Figure 3- 30. Level1 Page Table Format 228
Figure 3- 31. Level1 Page Table Format 228
Figure 3- 32. Read/Write Permission Control 228
Figure 3- 33. RTC Clock Tree 289
Figure 3- 34. RTC Application Diagram 291
Figure 3- 35. RTC Counter 292
Figure 3- 36. RTC 1KHz Counter Step Structure 292
Figure 3- 37. Calibration Circuit 294
Figure 3- 38. RC Waveform 294
Figure 3- 39. DCXO Timed Wakeup Waveform 295
Figure 3- 40. Message Box Block Diagram 309

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 3- 41. Message Box Typical Application Chart 311
Figure 3- 42. User1 and User0 Working Process 313
Figure 3- 43. Spinlock Block Diagram 322
Figure 3- 44. Spinlock Typical Application Diagram 323
Figure 3- 45. Spinlock State Machine 323
Figure 3- 46. CPU0 and CPUS Taking/Freeing Spinlock0 Process 324

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 3- 1. Reset Signal Description 38
Table 3- 2. BOOT_MODE Setting 140
Table 3- 3. GPADC Boot Select Setting 141
Table 3- 4. GPIO Pin Boot Select Configuration 141
Table 3- 5. eFuse Boot Select Configuration 141
Table 3- 6. eFuse Boot Select Setting 142
Table 3- 7. Fast Boot Select Setting 145
Table 3- 8. DMA DRQ Table 188
Table 3- 9. Source/Destination Address Distribution 190
Table 3- 10. Correspondence Relation between Master and Module 221
Table 3- 11. Relation between ACI and Domain 229
Table 3- 12. RTC External Signals 290
Table 3- 13. RTC Counter Changing Range 292

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 3 System

3.1. Memory Mapping

Module	Address(It is for Cluster CPU)	Size(Bytes)
N_BROM	0x0000 0000---0x0000 FFFF	64K
S_BROM	0x0000 0000—0x0000 BFFF	48K
SRAM A1	0x0002 0000---0x0002 3FFF	16K(support Byte operation, clock source is AHB1)
SRAM C	0x0002 4000---0x0004 4FFF	Borrow VE 112K, DE 20K, supports Byte operation, clock source is AHB1
SRAM A2	0x0010 0000---0x0011 3FFF	16K + 64K 0x0010 0000---0x00103FFF: only store CPUS Vector Table, and only 16 addresses are valid, 0x00100100, 0x00100200...0x00100F00. See Openrisc, the real space of SRAM A2 is 0x00104000---0x0011 3FFF
Accelerator		
GPU	0x0180 0000---0x0187 FFFF	512K
GPU_SYS	0x0188 0000---0x0188 03FF	1K
CE_NS	0x0190 4000---0x0190 47FF	2K
CE_S	0x0190 4800---0x0190 4FFF	2K
CE_KEY_SRAM	0x0190 8000---0x0190 8FFF	4K
VE SRAM	0x01A0 0000---0x01BF FFFF	2M
VE	0x01C0 E000---0x01C0 FFFF	8K
Video Input		
CSIC	0x0200 0000---0x021F FFFF	2M
CSIC_CCU	0x0200 0000---0x0200 07FF	2K
CSIC_TOP	0x0200 0800---0x0200 0FFF	2K
CSIC_PARSER0	0x0200 1000---0x0200 1FFF	4K
CSIC_PARSER1	0x0200 2000---0x0200 2FFF	4K
CSIC_DMA0	0x0200 9000---0x0200 91FF	0.5K
CSIC_DMA1	0x0200 9200---0x0200 93FF	0.5K
CSIC_DMA2	0x0200 9400---0x0200 95FF	0.5K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA3	0x0200 9600---0x0200 97FF	0.5K
CSIC_COMBO	0x0200 A000---0x0200 BFFF	8K
CSIC_ISP0	0x0210 0000---0x0210 1FFF	8K
CSIC_ISP1	0x0210 2000---0x0210 3FFF	8K
CSIC_TDM	0x0210 8000---0x0210 83FF	1K
CSIC_VIPP0	0x0211 0000---0x0211 03FF	1K
CSIC_VIPP1	0x0211 0400---0x0211 07FF	1K
CSIC_VIPP2	0x0211 0800---0x0211 0BFF	1K
CSIC_VIPP3	0x0211 0C00---0x0211 0FFF	1K
CSIC_SRAM	0x0220 0000---0x028F FFFF	7M
TOP_PKT_SRAM	0x0220 0000---0x0220 01FF	0.5K
BRIDGE_SRAM	0x0221 0000---0x0221 3FFF	16K
DMA_SRAM	0x0222 0000---0x0223 FFFF	128K
MBUS_SRAM	0x0224 0000---0x0224 1FFF	8K
VIPP0_SRAM	0x0230 0000---0x0231 FFFF	128K
VIPP1_SRAM	0x0232 0000---0x0233 FFFF	128K
VIPP2_SRAM	0x0234 0000---0x0235 FFFF	128K
VIPP3_SRAM	0x0236 0000---0x0237 FFFF	128K
ISP_SRAM	0x0240 0000---0x027F FFFF	4M
TDM_SRAM	0x0280 0000---0x0281 FFFF	128K
System Resources		
SYS_CFG	0x0300 0000---0x0300 0FFF	4K
CCU	0x0300 1000---0x0300 1FFF	4K
DMA	0x0300 2000---0x0300 2FFF	4K
MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 4000---0x0300 4FFF	4K
HSTIMER	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
SPC	0x0300 8000---0x0300 83FF	1K
TIMER	0x0300 9000---0x0300 93FF	1K
PWM	0x0300 A000---0x0300 A3FF	1K
GPIO	0x0300 B000---0x0300 B3FF	1K
PSI	0x0300 C000---0x0300 C3FF	1K
GIC	0x0302 0000---0x0302 FFFF	64K
IOMMU	0x030F 0000---0x030F FFFF	64K
NSI	0x0310 0000---0x0310 FFFF	64K
Memory		
NAND0	0x0401 1000---0x0401 1FFF	4K
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
DRAM	0x0480 0000---0x048F FFFF	1M
SMC	0x0480 0000---0x0480 FFFF	64K
DRAM_TOP	0x0481 0000---0x0481 FFFF	64K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DDRCTL	0x0482 0000---0x0482 FFFF	64K
DDRPHY	0x0483 0000---0x0483 FFFF	64K
Interfaces		
UART0	0x0500 0000---0x0500 03FF	1K
UART1	0x0500 0400---0x0500 07FF	1K
UART2	0x0500 0800---0x0500 0BFF	1K
UART3	0x0500 0C00---0x0500 0FFF	1K
UART4	0x0500 1000---0x0500 13FF	1K
TWI0	0x0500 2000---0x0500 23FF	1K
TWI1	0x0500 2400---0x0500 27FF	1K
TWI2	0x0500 2800---0x0500 2BFF	1K
TWI3	0x0500 2C00---0x0500 2FFF	1K
SPI0	0x0501 0000---0x0501 0FFF	4K
SPI1	0x0501 1000---0x0501 1FFF	4K
SPI2	0x0501 2000---0x0501 2FFF	4K
LEDC	0x0501 8000---0x0501 83FF	1K
EMAC0	0x0502 0000---0x0502 FFFF	64K
GPADC	0x0507 0000---0x0507 03FF	1K
THS	0x0507 0400---0x0507 07FF	1K
LRADC	0x0507 0800---0x0507 0BFF	1K
CIR_TX	0x0507 1000---0x0507 13FF	1K
CIR_RX	0x0507 1800---0x0507 1BFF	1K
I2S0	0x0509 0000---0x0509 0FFF	4K
I2S1	0x0509 1000---0x0509 1FFF	4K
I2S2	0x0509 2000---0x0509 2FFF	4K
I2S3	0x0509 3000---0x0509 3FFF	4K
OWA	0x0509 4000---0x0509 43FF	1K
DMIC	0x0509 5000---0x0509 53FF	1K
Audio Codec	0x0509 6000---0x0509 6FFF	4K
USB0(USB2.0_OTG)	0x0510 0000---0x051F FFFF	1M
USB1(USB2.0_HOST)	0x0520 0000---0x052F FFFF	1M
Display		
DE	0x0600 0000---0x063F FFFF	4M
G2D	0x0648 0000---0x064B FFFF	256K
DSI0	0x0650 4000---0x0650 5FFF	8K
DSI_CORE	0x0650 4000---0x0650 43FF	1K
DSI_CONFIG_REG	0x0650 4400---0x0650 4FFF	3K
DPSS_TOP0	0x0651 0000---0x0651 0FFF	4K
TCON_LCD0	0x0651 1000---0x0651 1FFF	4K
CPUS Related		
RTC	0x0700 0000---0x0700 03FF	1K
R_CPUS_CFG	0x0700 0400---0x0700 0BFF	2K
R_PPU	0x0700 1000---0x0700 13FF	1K
R_PRCM	0x0701 0000---0x0701 03FF	1K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

R_TIMER	0x0702 0000---0x0702 03FF	1K
R_WDG	0x0702 0400---0x0702 07FF	1K
R_TWDG	0x0702 0800---0x0702 0BFF	1K
R_PWM	0x0702 0C00---0x0702 0FFF	1K
R_INTC	0x0702 1000---0x0702 13FF	1K
R_GPIO	0x0702 2000---0x0702 23FF	1K
R_CPUS_MBIST	0x0703 1000---0x0703 1FFF	4K
R_CIR_RX	0x0704 0000---0x0704 03FF	1K
R_UART	0x0708 0000---0x0708 03FF	1K
R_TWI0	0x0708 1400---0x0708 17FF	1K
R_TWI1	0x0708 1800---0x0708 1BFF	1K
CPUX Related		
CPU_SUBSYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STU	0x0811 0000---0x0811 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
IDC	0x0813 0000---0x0813 0FFF	3K
PLL_CPU_CFG	0x0814 0000---0x0814 03FF	1K
C0_CPUX_CFG	0x0901 0000---0x0901 03FF	1K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
DRAM		
DRAM	0x4000 0000---0x13FFF FFFF	4G

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2. CPUX Configuration

3.2.1. Overview

The C0_CPUX_CFG module is used for configuring cluster0 (quad-core Cortex-A53, 32 KB I-cache and 32 KB D-cache, 512 KB L2 cache), such as reset, control, cache, debug, CPU status.
The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as GIC-400, JTAG, etc.

The CPUX_CFG includes the following features:

- CPU reset system: core reset, debug circuit reset and other reset function
- CPU related control: interface control, CP15 control, power-on/off control
- CPU status check: idle status, SMP status, interrupt status
- CPU control and status register about debug related

3.2.2. Operations and Functional Descriptions

3.2.2.1. Signal Description

For the detail of CPUX signal, please refer to ***ARM Cortex-A53 TRM***, such as DDI0464F_cortex_A53_mpcore_r0p5_trm.pdf.

3.2.2.2. L2 Idle Mode

When the L2 cache of cluster needs to enter WFI mode, firstly make sure that the CPU[3:0] of cluster enters WFI mode, which can be checked through the bit[19:16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of cluster by writing 1 to the bit0 of **Cluster Control Register1**, and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Note that set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.2.3. CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX reset system is as follows.

Table 3- 1. Reset Signal Description

Reset Signal	Description
CORE_RST	This is the primary reset signal which can reset the corresponding core logic including NEON, VFP, Debug, ETM, breakpoint and watchpoint logic. It maps to a warm reset that covers reset of the processor logic.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. It maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/GIC-400/CPU_SUBSYS_CTRL.

3.2.2.4. CPUX Power Block Diagram

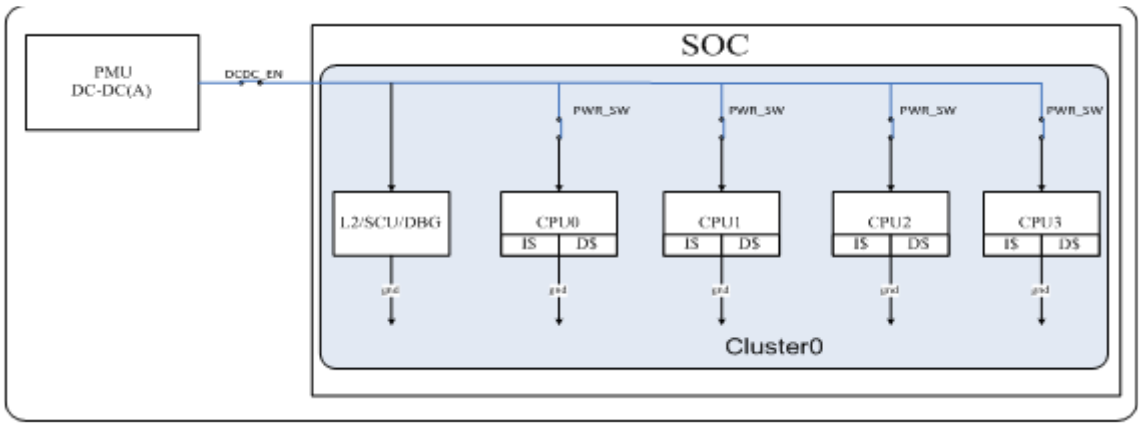


Figure 3- 1. CPUX Power Domain Block Diagram

Figure 3-1 lists the power domain of cluster in default. The power switch of all CPU core are power-on, the pwron_rst of all CPU core are de-asserted, the core reset of CPU0 is de-asserted, the core reset of CPU [3:1] is asserted.

Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

C0_CPUX_CFG and cluster0 belong to the same power domain, within opening and closing cluster0 process, when cluster0 starts to power on again from power-off state, C0_CPUX_CFG holds in default state, at this time software need initial C0_CPUX_CFG after C0_H_RST is de-asserted.

CPU_SUBSYS_CTRL belongs to system power domain. The power domains of CPU related module are as follows.

Power Domain	Modules	Description
Cluster0	Cluster0/C0_CPUX_CFG/C0_MBIST	Cluster0 circuit, C0_CPUX_CFG module and CPU

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

		reset/power/mbist
System	Timestamp/GIC/CPU_SUBSYS_CTRL/Clock	Provide system source of CPU sub-system
CPUS	CPUS_CFG	It is used for power on/off control of CORE or Cluster. Note that CPUS_CFG belongs to system power domain in SoC without CPUS.

3.2.2.5. Operation Principle

The CPU-related operations (such as open/close core, cluster switch, status query) need proper configuration of C0_CPUX_CFG module, as well as the combination of related system control resources including BUS, clock.

3.2.3. Cluster 0 Configuration Register List

Module Name	Base Address
C0_CPUX_CFG	0x09010000

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
CACHE_CFG_REG	0x0024	Cache Configuration Register
C0_CPU0_CTRL_REG	0x0060	Cluster 0 CPU0 Control Register
C0_CPU1_CTRL_REG	0x0064	Cluster 0 CPU1 Control Register
C0_CPU2_CTRL_REG	0x0068	Cluster 0 CPU2 Control Register
C0_CPU3_CTRL_REG	0x006C	Cluster 0 CPU3 Control Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 0 L2 Status Register

3.2.4. Cluster 0 Configuration Register Description

3.2.4.1. 0x0000 Cluster 0 Reset Control Register(Default Value: 0x1300_0100)

Offset: 0x0000			Register Name: C0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-assert

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal is for test 0: Assert 1: De-assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-assert
23:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-assert
7:0	/	/	/

3.2.4.2. 0x0010 Cluster 0 Control Register0(Default Value: 0x8000_0000)

Offset: 0x0010			**Register Name: C0_CTRL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus 0: Barriers are broadcasted onto system bus, this requires an AMBA4 interconnect 1: Barriers are not broadcasted onto the system bus. This is compatible with an AXI3 interconnect
30	R/W	0x0	BROADCAST_INNER Enable broadcasting of inner shareable transactions 0: Inner shareable transactions are not broadcasted externally 1: Inner shareable transactions are broadcasted externally
29	R/W	0x0	BROADCAST_OUTER Enable broadcasting of outer shareable transactions 0: Outer shareable transactions are not broadcasted externally 0: Outer shareable transactions are broadcasted externally
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches 1: Cache maintenance operations are broadcasted to downstream caches
27:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: L2 cache is reset by hardware 1: L2 cache is not reset by hardware
3:0	/	/	/

3.2.4.3. 0x0014 Cluster 0 Control Register1(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: C0_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CRM auto select slow frequency enable 0: Disable auto select 1: Enable auto select
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepts request 0: Snoop interface is active 1: Snoop interface is inactive

3.2.4.4. 0x0018 Cluster 0 Control Register2(Default Value: 0x0000_0010)

Offset: 0x0018			Register Name: C0_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain high for at least one clock cycle to be visible by the cores.
23:0	/	/	/

3.2.4.5. 0x0024 Cache Configuration Register(Default Value: 0x0018_001A)

Offset: 0x0024			Register Name: CACHE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:19	R/W	0x3	EMA_L2D L2 Cache SRAM EMA control port
18:17	R/W	0x0	EMAW_L2D L2 Cache SRAM EMAW control port
16	R/W	0x0	EMAS_L2D L2 Cache SRAM EMAS control port
15:6	/	/	/
5:3	R/W	0x3	EMA Cache SRAM EMA control port

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2:1	R/W	0x1	EMAW Cache SRAM EMAW control port
0	R/W	0x0	EMAS Cache SRAM EMAS control port

3.2.4.6. 0x0060 Cluster 0 CPU0 Control Register(Default Value: 0x0000_0107)

Offset: 0x0060			Register Name: C0_CPU0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	CPU0_DBGNOPWRDWN No power-down request. Debugger has requested that processor is not powered down. Debug no power down.
12	R	0x0	CPU0_DBGPWRUPREQ Power up request Debug power up request 0: Do not request that the core is powered up 1: Request that the core is powered up
11	/	/	/
10	R	0x0	CPU0_DBGRESTARTED Handshake for DBGRESTART
9	R/W	0x0	CPU0_DBGRESTART External restart requests
8	R/W	0x1	CPU0_DBGPWRDUP Cluster Powered up 0: Core is powered down 1: Core is powered up
7	/	/	/
6	R/W	0x0	CPU0_EXM_CLR Clear the status of interface
5	R/W	0x0	CPU0_CP15S_DISABLE Disable write access to some secure CP15 register
4	R/W	0x0	CPU0_L1_RST_DISABLE Disable automatic Cluster CPU0 L1 cache invalidate at reset 0: L1 cache is reset by hardware 1: L1 cache is not reset by hardware
3	/	/	/
2	R/W	0x1	CPU0_ETM_RST Cluster0 CPU0 ETM Reset Assert 0: Assert 1: De-assert
1	R/W	0x1	CPU0_DBG_RST

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Cluster0 CPU0 Debug Reset Assert 0: Assert 1: De-assert
0	R/W	0x1	CPU0_CORE_RESET Cluster CPU0 Reset Assert 0: Assert 1: De-assert

3.2.4.7. 0x0064 Cluster 0 CPU1 Control Register(Default Value: 0x0000_0106)

Offset: 0x0064			Register Name: C0_CPU1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	CPU1_DBGNOPWRDWN No power-down request. Debugger has requested that processor is not powered down. Debug no power down.
12	R	0x0	CPU1_DBGPWRUPREQ Power up request Debug power up request 0: Do not request that the core is powered up 1: Request that the core is powered up
11	/	/	/
10	R	0x0	CPU1_DBGRESTARTED Handshake for DBGRESTART
9	R/W	0x0	CPU1_DBGRESTART External restart requests
8	R/W	0x1	CPU1_DBGPWRDUP Cluster Powered up 0: Core is powered down 1: Core is powered up
7	/	/	/
6	R/W	0x0	CPU1_EXM_CLR Clear the status of interface
5	R/W	0x0	CPU1_CP15S_DISABLE Disable write access to some secure CP15 register
4	R/W	0x0	CPU1_L1_RST_DISABLE Disable automatic Cluster CPU1 L1 cache invalidate at reset 0: L1 cache is reset by hardware 1: L1 cache is not reset by hardware
3	/	/	/
2	R/W	0x1	CPU1_ETM_RST Cluster0 CPU1 ETM Reset Assert

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Assert 1: De-assert
1	R/W	0x1	CPU1_DBG_RST Cluster0 CPU1 Debug Reset Assert 0: Assert 1: De-assert
0	R/W	0x1	CPU1_CORE_RESET Cluster0 CPU1 Reset Assert 0: Assert 1: De-assert

3.2.4.8. 0x0068 Cluster 0 CPU2 Control Register(Default Value: 0x0000_0106)

Offset: 0x0068			Register Name: C0_CPU2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	CPU2_DBGNOPWRDWN No power-down request. Debugger has requested that processor is not powered down. Debug no power down.
12	R	0x0	CPU2_DBGPWRUPREQ Power up request Debug power up request 0: Do not request that the core is powered up 1: Request that the core is powered up
11	/	/	/
10	R	0x0	CPU2_DBGRESTARTED Handshake for DBGRESTART
9	R/W	0x0	CPU2_DBGRESTART External restart requests
8	R/W	0x1	CPU2_DBGPWRDUP Cluster Powered up 0: Core is powered down 1: Core is powered up
7	/	/	/
6	R/W	0x0	CPU2_EXM_CLR Clear the status of interface
5	R/W	0x0	CPU2_CP15S_DISABLE Disable write access to some secure CP15 register
4	R/W	0x0	CPU2_L1_RST_DISABLE Disable automatic Cluster CPU2 L1 cache invalidate at reset 0: L1 cache is reset by hardware 1: L1 cache is not reset by hardware

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	/	/	/
2	R/W	0x1	CPU2_ETM_RST Cluster0 CPU2 ETM Reset Assert 0: Assert 1: De-assert
1	R/W	0x1	CPU2_DBG_RST Cluster0 CPU2 Debug Reset Assert 0: Assert 1: De-assert
0	R/W	0x1	CPU2_CORE_RESET Cluster0 CPU2 Reset Assert 0: Assert 1: De-assert

3.2.4.9. 0x006C Cluster 0 CPU3 Control Register(Default Value: 0x0000_0106)

Offset: 0x006C			**Register Name: C0_CPU3_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	CPU3_DBGNOPWRDWN No power-down request. Debugger has requested that processor is not powered down. Debug no power down.
12	R	0x0	CPU3_DBGPWRUPREQ Power up request Debug power up request 0: Do not request that the core is powered up 1: Request that the core is powered up
11	/	/	/
10	R	0x0	CPU3_DBGRESTARTED Handshake for DBGRESTART
9	R/W	0x0	CPU3_DBGRESTART External restart requests
8	R/W	0x1	CPU3_DBGPWRDUP Cluster Powered up 0: Core is powered down 1: Core is powered up
7	/	/	/
6	R/W	0x0	CPU3_EXM_CLR Clear the status of interface
5	R/W	0x0	CPU3_CP15S_DISABLE Disable write access to some secure CP15 register
4	R/W	0x0	CPU3_L1_RST_DISABLE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Disable automatic Cluster CPU3 L1 cache invalidate at reset 0: L1 cache is reset by hardware 1: L1 cache is not reset by hardware
3	/	/	/
2	R/W	0x1	CPU3_ETM_RST Cluster0 CPU3 ETM Reset Assert 0: Assert 1: De-assert
1	R/W	0x1	CPU3_DBG_RST Cluster0 CPU3 Debug Reset Assert 0: Assert 1: De-assert
0	R/W	0x1	CPU3_CORE_RESET Cluster0 CPU3 Reset Assert 0: Assert 1: De-assert

3.2.4.10. 0x0080 Cluster0 CPU Status Register(Default Value: 0x000E_0000)

Offset: 0x0080			**Register Name: C0_CPU_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R	0x0	SMP_AMP CPU[3:0] is in Symmetric Multiprocessing mode or Asymmetric Multiprocessing mode. 0: AMP mode 1: SMP mode
23:20	/	/	/
19:16	R	0xE	STANDBYWFI Indicates if Cluster CPU[3:0] is in WFI standby mode 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:12	/	/	/
11:8	R	0x0	STANDBYWFE Indicates if Cluster CPU[3:0] is in the WFE standby mode 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2 Indicates if the Cluster L2 memory system is in WFI standby mode 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.4.11. 0x0084 L2 Status Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R	0x0	EVENTO Event output. This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8:0	/	/	/

3.2.5. CPU Subsystem Control Register List

Module Name	Base Address
CPU_SUBSYS_CTRL	0x08100000

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and JTAG Reset Control Register
C0_INT_EN	0x0010	Cluster0 Interrupt Enable Control Register
IRQ_FIQ_STATUS	0x0014	IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2
DBG_STATE	0x001C	Debug State Register
CPU0_CTRL_REG	0x0020	CPU0 Control Register
CPU1_CTRL_REG	0x0024	CPU1 Control Register
CPU2_CTRL_REG	0x0028	CPU2 Control Register
CPU3_CTRL_REG	0x002C	CPU3 Control Register
RVBARADDR0_L	0x0040	Reset Vector Base Address Register0_L
RVBARADDR0_H	0x0044	Reset Vector Base Address Register0_H
RVBARADDR1_L	0x0048	Reset Vector Base Address Register1_L
RVBARADDR1_H	0x004C	Reset Vector Base Address Register1_H
RVBARADDR2_L	0x0050	Reset Vector Base Address Register2_L
RVBARADDR2_H	0x0054	Reset Vector Base Address Register2_H
RVBARADDR3_L	0x0058	Reset Vector Base Address Register3_L
RVBARADDR3_H	0x005C	Reset Vector Base Address Register3_H

3.2.6. CPU Subsystem Control Register Description

3.2.6.1. 0x0000 General Control Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:3	/	/	/
2	R/W	0x0	Cluster 0 corepll select 0: CCU clock 1: disp pll clock
1	R/W	0x0	IDC clock enable 0: Disable IDC clock 1: Enable IDC clock
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

3.2.6.2. 0x000C GIC and Jtag Reset Control Register(Default Value: 0x0000_0F07)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EXM_CLR[3:0] Clear the status of interface, for debug
15:12	/	/	/
11	R/W	0x1	CS_RST CoreSight Reset 0: assert 1: de-assert
10	R/W	0x1	DAP_RST DAP Reset 0: assert 1: de-assert
9	R/W	0x1	PORTRST Jtag portrst 0: assert 1: de-assert
8	R/W	0x1	TRST Jtag trst 0: assert 1: de-assert
7:2	/	/	/
1	R/W	0x1	IDC_RST Interrupt delay controller reset 0: assert 1: de-assert
0	R/W	0x1	GIC_RST GIC_reset_cpu_reg 0: assert 1: de-assert

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.6.3. 0x0010 Cluster 0 Interrupt Enable Register(Default Value: 0x0000_FFFF)

Offset: 0x0010			Register Name: C0_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt enable control register. Mask irq_out/firq_out to system domain.

3.2.6.4. 0x0014 GIC IRQ/FIQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: IRQ_FIQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0000	FIQ_OUT[15:0]
15:0	R/W	0x0000	IRQ_OUT[15:0]

3.2.6.5. 0x0018 General Control Register2(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GENER_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CDBGRSTACK Debug Reset ACK
15:1	/	/	/
0	R/W	0x0	C0_TSCLKCHANGE Cluster 0 Time Stamp change bit

3.2.6.6. 0x001C Debug State Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DBG_STATE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	CLU_PWRSW_STA
23:1	/	/	/
0	R	0x0	C0_DBG_STATE Cluster 0 is in debug mode or normal mode

3.2.6.7. 0x0020 CPU0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CPU0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU0 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

3.2.6.8. 0x0024 CPU1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CPU1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU1 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

3.2.6.9. 0x0028 CPU2 Control Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CPU2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU2 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

3.2.6.10. 0x002C CPU3 Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CPU3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU3 AA64NAA32 Register width state 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.6.11. 0x0040 Reset Vector Base Address Register0_L(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: RVBARADDR0_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[31:2] for executing in 64-bit state (AArch64) of CPU0.
1:0	/	/	/

3.2.6.12. 0x0044 Reset Vector Base Address Register0_H(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: RVBARADDR0_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:32] for executing in 64-bit state (AArch64) of CPU0.

3.2.6.13. 0x0048 Reset Vector Base Address Register1_L(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: RVBARADDR1_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[31:2] for executing in 64-bit state (AArch64) of CPU1.
1:0	/	/	/

3.2.6.14. 0x004C Reset Vector Base Address Register1_H(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: RVBARADDR1_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:32] for executing in 64-bit state (AArch64) of CPU1.

3.2.6.15. 0x0050 Reset Vector Base Address Register2_L(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: RVBARADDR2_L
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[31:2] for executing in 64-bit state (AArch64) of CPU2.
1:0	/	/	/

3.2.6.16. 0x0054 Reset Vector Base Address Register2_H(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: RVBARADDR2_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:32] for executing in 64-bit state (AArch64) of CPU2.

3.2.6.17. 0x0058 Reset Vector Base Address Register3_L(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: RVBARADDR3_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARADDR[31:2] Reset Vector Base Address[31:2] for executing in 64-bit state (AArch64) of CPU3.
1:0	/	/	/

3.2.6.18. 0x005C Reset Vector Base Address Register3_H(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: RVBARADDR3_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR[39:32] Reset Vector Base Address[39:32] for executing in 64-bit state (AArch64) of CPU3.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3. CCU

3.3.1. Overview

The clock controller unit (CCU) controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. The CCU input signals include the external clock for the reference frequency (24 MHz). The outputs from CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 12 PLLs
- Bus source and divisions
- Clock output control
- PLL bias control
- PLL tuning control
- PLL pattern control
- Configuring modules clock
- Bus clock gating
- Bus software reset
- PLL lock control

3.3.2. Operations and Functional Descriptions

3.3.2.1. System Bus Tree

Figure 3-2 shows a block diagram of the system bus tree.
The system bus tree is used to introduce bus interface of every module. These modules can divide into two types: the master and slave of bus. For example, DMA, BIST_MST(Built-in Self Test Master), CE, SMHC0/1/2, CPUS, CPUX and DS(Debug System) are as bus master that can access corresponding register of every slave through bus. Every slave hangs in corresponding bus.

For example, CPU accesses to RTC module, the process is as follows: CPU instruction firstly passes AXI bus, then goes to PSI bus through AXI2PSI bridge, then goes to AHBS bus through PSI2AHB bridge, and goes to APBS2 through AHB2APB, finally RTC is operated based on relevant bus protocol. The access time from CPU to RTC, is relevant with the CPU clock, AXI bus clock, PSI bus clock, AHBS bus clock and APBS2 bus clock. Any lower bus clock will lead to access time very long.

In above module, the clocks of these modules(such as TWI and UART) to be hung on APB2/APBS2 are from their respective bus clock, however the clocks of most other modules are from related CLK register, such as DE_CLK_REG. Each module clock requirement can refer to their module.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

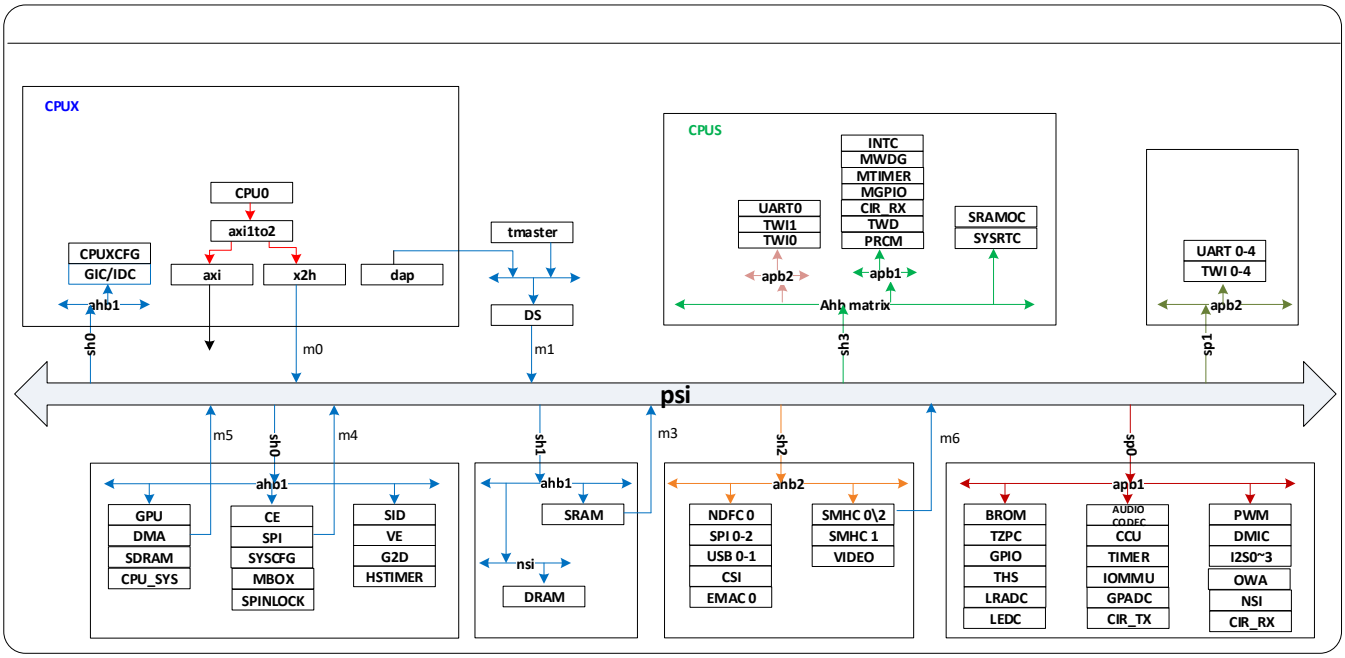


Figure 3- 2. System Bus Tree

3.3.2.2. Bus Clock Generation

Figure 3-3 describes bus clock generation.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

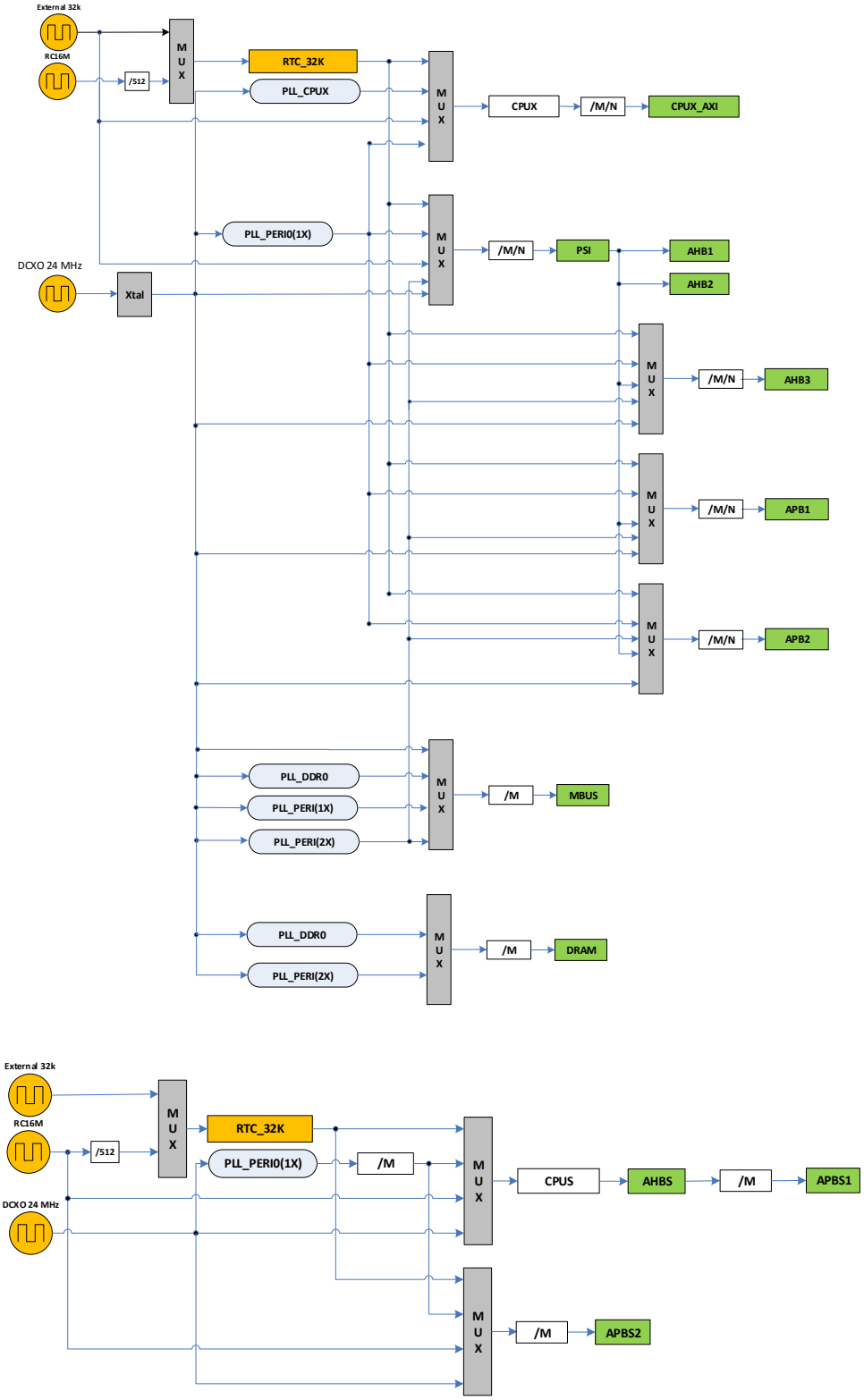


Figure 3- 3. Bus Clock Generation

3.3.2.3. Module Clock Generation

Figure 3-4 describes module clock generation.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

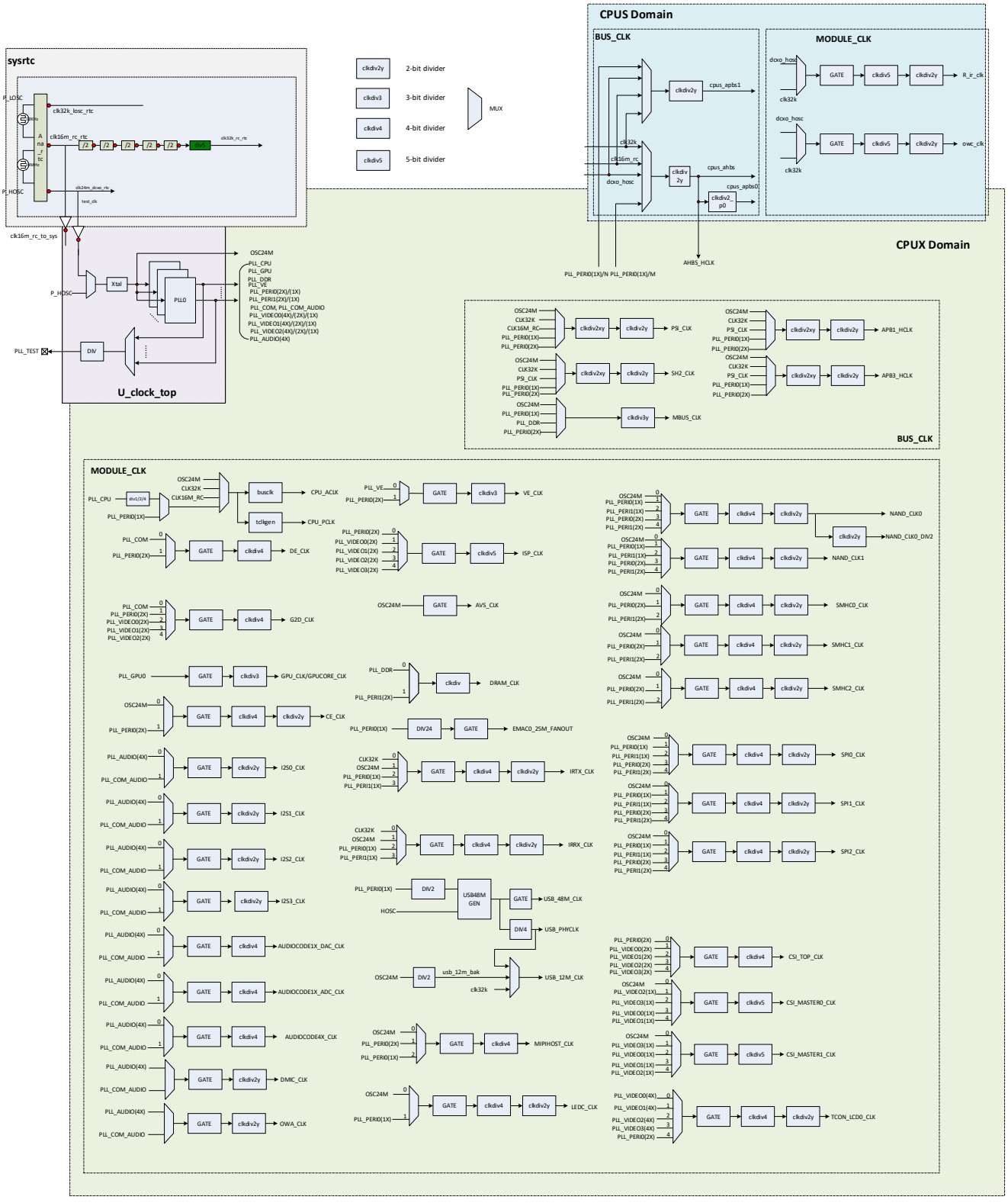


Figure 3- 4. Module Clock Generation

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Module	Clock Name	DIV1	DIV2	Source0	Source1	Source2	Source3	Source4
CPU	CPU_CLK	1~4	1~4	OSC24M	CLK32K	CLK16M_RC	CPU_PLL	PLL_PERI0(1X)
PSI/AHB1/AHB2	PSI_CLK,AHB1_CLK,AHB2_CLK	1~4	1/2/4/8	OSC24M	CLK32K	CLK16M_RC	PLL_PERI0(1X)	PLL_PERI0(2X)
AHB3/AHB_MSTG	AHB3_CLK	1~4	1/2/4/8	OSC24M	CLK32K	PSI_CLK	PLL_PERI0(1X)	PLL_PERI0(2X)
APB1	APB1_CLK	1~4	1/2/4/8	OSC24M	CLK32K	PSI_CLK	PLL_PERI0(1X)	PLL_PERI0(2X)
APB2	APB2_CLK	1~4	1/2/4/8	OSC24M	CLK32K	PSI_CLK	PLL_PERI0(1X)	PLL_PERI0(2X)
MBUS/NSI	MBUS_CLK	1~8	/	OSC24M	PLL_DDR	PLL_PERI0(1X)	PLL_PERI0(2X)	/
DE	DE_CLK	1~16	/	PLL_COM	PLL_PERI0(2X)	/	/	/
G2D	G2D_CLK	1~16	/	PLL_COM	PLL_PERI0(2X)	PLL_VIDEO0(2X)	PLL_VIDEO1(2X)	PLL_VIDEO2(2X)
GPU	GPUCORE_CLK	1~8	/	PLL_GPU	/	/	/	/
CE	CE_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(2X)	/	/	/
VE	VE_CLK	1~8	/	PLL_VE	PLL_PERI0(2X)	/	/	/
AVS	AVS_CLK	/	/	OSC24M	/	/	/	/
DRAM	DRAM_CLK	1~32	/	PLL_DDR	PLL_PERI1(2X)	/	/	/
NAND0_0	NAND0_CLK0	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	PLL_PERI0(2X)	PLL_PERI1(2X)
NAND0_1	NAND0_CLK1	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	PLL_PERI0(2X)	PLL_PERI1(2X)
SMHC0	SMHC0_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(2X)	PLL_PERI1(2X)	/	/
SMHC1	SMHC1_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(2X)	PLL_PERI1(2X)	/	/
SMHC2	SMHC2_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(2X)	PLL_PERI1(2X)	/	/
SPI0	SPI0_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	PLL_PERI0(2X)	PLL_PERI1(2X)
SPI1	SPI1_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	PLL_PERI0(2X)	PLL_PERI1(2X)
SPI2	SPI2_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	PLL_PERI0(2X)	PLL_PERI1(2X)
EMAC0_25M	EMAC0_CLK25M_FANOUT	/	/	EMAC_25M_CLK	/	/	/	/
CIR_RX	IRRX_CLK	1~16	1/2/4/8	CLK32K	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	/
CIR_TX	IRTX_CLK	1~16	1/2/4/8	CLK32K	OSC24M	PLL_PERI0(1X)	PLL_PERI1(1X)	/
I2S/PCM0	I2SPCM0_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
I2S/PCM1	I2SPCM1_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
I2S/PCM2	I2SPCM2_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
I2S/PCM3	I2SPCM3_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
OWA	OWA_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
DMIC	DMIC_CLK	/	1/2/4/8	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
AUDIOCODEC1X_DAC	AUDIOCODEC1X_DAC_CLK	1~16	/	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
AUDIOCODEC1X_ADC	AUDIOCODEC1X_ADC_CLK	1~16	/	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
AUDIOCODEC4X	AUDIOCODEC4X_CLK	1~16	/	PLL_AUDIO(4X)	PLL_COM_AUDIO	/	/	/
MIPIHOST0	MIPIHOST0_CLK	1~16	/	OSC24M	PLL_PERI0(2X)	PLL_PERI0(1X)	/	/
TCONLCD0	TCONLCD0_CLK	1~16	1/2/4/8	PLL_VIDEO0(4X)	PLL_VIDEO1(4X)	PLL_VIDEO2(4X)	PLL_VIDEO3(4X)	PLL_PERI0(2X)
LEDC	LEDC_CLK	1~16	1/2/4/8	OSC24M	PLL_PERI0(1X)	/	/	/
CSITOP	CSITOP_CLK	1~16	/	PLL_PERI0(2X)	PLL_VIDEO0(2X)	PLL_VIDEO1(2X)	PLL_VIDEO2(2X)	PLL_VIDEO3(2X)
CSIMASTER	CSIMASTER_CLK	1~32	/	OSC24M	PLL_VIDEO2(1X)	PLL_VIDEO3(1X)	PLL_VIDEO0(1X)	PLL_VIDEO1(1X)
CSIMASTER1	CSIMASTER1_CLK	1~32	/	OSC24M	PLL_VIDEO3(1X)	PLL_VIDEO0(1X)	PLL_VIDEO1(1X)	PLL_VIDEO2(1X)
ISP	ISP_CLK	1~16	/	PLL_PERI0(2X)	PLL_VIDEO0(2X)	PLL_VIDEO1(2X)	PLL_VIDEO2(2X)	PLL_VIDEO3(2X)

Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.2.4. PLL Distribution

Figure 3-5 shows the block diagram of the PLL distribution.

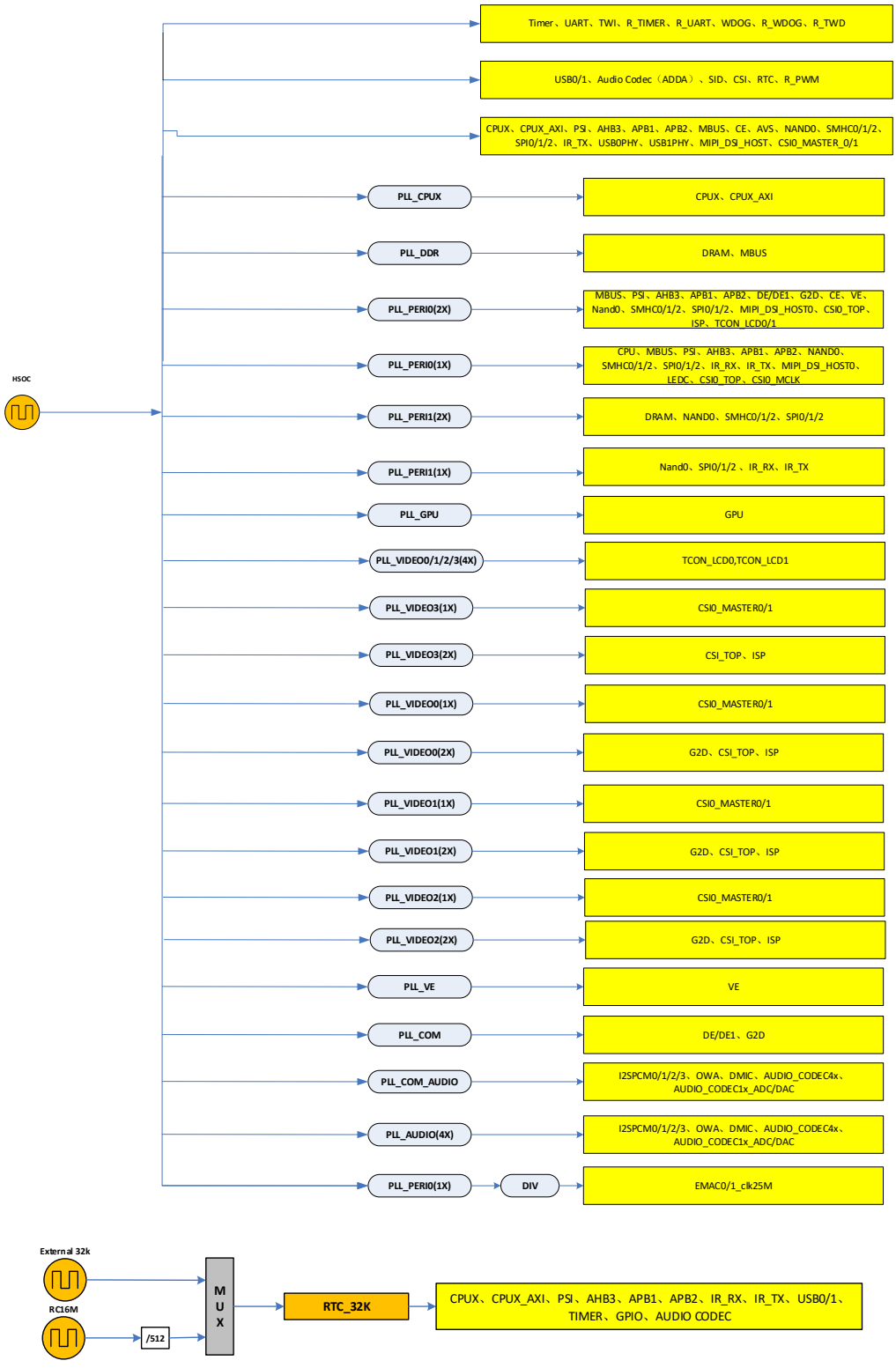


Figure 3- 5. PLL Distribution

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PLL Type	Application Module	Note
PLL_CPUX	CPUX, CPUX_AXI	The PLL_CPUX supports dynamic modification of frequency factors to achieve DVFS.
PLL_DDR	MBUS, DRAM	The PLL_DDR supports spread spectrum, and does not support linear frequency modulation.
PLL_PERI0(2X)	MBUS, PSI, AHB1, AHB2, AHB3, APB1, APB2, DE, G2D, CE, VE, NAND, SMHC0/1/2, SPI0/1/2, ISP, CSI0_TOP, MIPI_DSI_HOST0, TCON_LCD0	The PLL_PERI0(2X) does not support dynamic frequency modulation.
PLL_PERI0(1X)	MBUS, PSI, AHB1, AHB2, AHB3, APB1, APB2, NAND, SPI0/1/2, LEDC, CIR_RX, CIR_TX, MIPI_DSI_HOST0, CPUX, CPUX_AXI	The PLL_PERI0(1X) does not support dynamic frequency modulation.
PLL_PERI1(2X)	DRAM, NAND, SMHC0/1/2, SPI0/1/2	The output clock of PLL_PERI1(2X) is 1.2 GHz. The PLL_PERI1(2X) does not support dynamic frequency modulation.
PLL_PERI1(1X)	NAND, SPI0/1/2, CIR_RX, CIR_TX	The output clock of PLL_PERI1(1X) is 600 MHz. The PLL_PERI1(1X) does not support dynamic frequency modulation.
PLL_VE	VE	The PLL_VE does not support dynamic frequency modulation.
PLL_COM	DE/1, G2D	The PLL_COM does not support dynamic frequency modulation.
PLL_COM_AUDIO	I2S/PCM0/1/2/3, DMIC, OWA, AUDIO_CODEC_ADC/DAC_1X, AUDIO_CODEC_4X	
PLL_AUDIO(4X)	I2S/PCM0/1/2/3, DMIC, OWA, AUDIO_CODEC_ADC/DAC_1X, AUDIO_CODEC_4X	The PLL_AUDIO(4X) does not support DVFS.
PLL_VIDEO0(1X)/ PLL_VIDEO1(1X)/ PLL_VIDEO2(1X)	CSI_MASTER0/1	The PLL_VIDEO0(1X)/PLL_VIDEO1(1X)/PLL_VIDEO2(1X) does not support dynamic frequency modulation.
PLL_VIDEO0(2X)/ PLL_VIDEO1(2X)/ PLL_VIDEO2(2X)	G2D, CSI_TOP, ISP	The PLL_VIDEO0(2X)/PLL_VIDEO1(2X)/PLL_VIDEO2(2X) does not support dynamic frequency modulation.
PLL_VIDEO0(4X)/ PLL_VIDEO1(4X)/ PLL_VIDEO2(4X)	TCON_LCD0	The PLL_VIDEO0(4X)/PLL_VIDEO1(4X)/PLL_VIDEO2(4X) does not support dynamic frequency modulation.
PLL_VIDEO3(1X)	CSI_MASTER0/1	The PLL_VIDEO3(1X) does not support dynamic frequency modulation.
PLL_VIDEO3(2X)	CSI_TOP, ISP	The PLL_VIDEO3(2X) does not support dynamic frequency modulation.
PLL_VIDEO3(4X)	TCON_LCD0	The PLL_VIDEO3(4X) does not support dynamic frequency

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

		modulation.

3.3.3. Programming Guidelines

3.3.3.1. Frequency Adjustment of PLL_CPUX

The frequency configuration formula of PLL_CPUX: PLL_CPUX = 24MHz*N/P, where, the N parameter is frequency-doubling factor of PLL, the next parameter configuration can proceed after PLL relock; the P parameter is digital post-frequency division, which can be dynamically switched in real time, and it does not affect the normal work of PLL.

The CPU PLL supports dynamic frequency configuration (modify the value of N). The CPU should first switch to a lower intermediate frequency and then adjust to the target frequency when switching the frequency. The process is as follows.

(1) Before you configure PLL_CPU, switch the clock source of CPU to PLL_PERI0(1X).
(2) Modify the N, P parameter of PLL_CPU.
(3) Write the PLL Lock Enable bit to 0 and then write it to 1.
(4) Wait the Lock bit (bit28) of PLL_CPUX_CTRL to 1.
(5) Switch the clock source of CPU to PLL_CPU.

3.3.3.2. Frequency Adjustment of PLL_AUDIO

The frequency configuration formula of PLL_AUDIO: PLL_AUDIO = 24MHz*N/M0/M1/P. Changing any parameter of N, M0, M1 and P will affect the normal work of PLL, which needs to be relocked. Therefore, dynamic adjustment is not supported.

For PLL_AUDIO, two frequency points usually are needed: 24.576*4MHz and 22.5792*4MHz. There are generally specific recommended configuration factors for the two frequencies. To implement the desired frequency point of PLL_AUDIO, you need to use the decimal frequency division function. The process is as follows.

(1) Configure the N, M1, M0, P factor.
(2) Configure the PLL_SDM_ENABLE bit of PLL_AUDIO_CTRL to 1.
(3) Configure PLL_AUDIO_PAT0_CTRL to enable digital spread spectrum.
(4) Write the PLL Lock Enable bit of PLL_AUDIO_CTRL to 0 and then write it to 1.
(5) Wait the Lock bit (bit28) of PLL_AUDIO_CTRL to 1.

NOTE

The P factor of PLL_AUDIO is odd number, the clock output is non-equal duty.

3.3.3.3. Frequency Adjustment of PLL_DDR

For the clock of DDR, the switch of the clock source and the frequency division coefficient is burrless, but the

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

frequency adjustment of the module should follow the following rules.

- From high frequency to low frequency: switch the clock source first, and then set the frequency division coefficient;
- From low frequency to high frequency: switch the frequency division coefficient first, and then modify clock source.

3.3.3.4. Frequency Adjustment of General PLL

(1) At present, the PLL should be enabled. If the PLL is not enabled, refer to the PLL process from disable to enable in section 3.3.3.5. For PLL, it is not suggested to switch during PLL using. When clock is not needed, it is suggested to configure the PLL_OUTPUT_EN bit of PLL_CTRL to 0 to disable the output gate of PLL.
(2) General PLL cannot be used in the process of frequency modulation. It is suggested to configure the PLL_OUTPUT_EN bit of PLL_CTRL to 0 in the process of PLL adjustment.
(3) Configure the N, M1, M0 factor. (It is not suggested to configure M1 factor, configure according to <<PLL recommended configuration table>>)
(4) Write the PLL Lock Enable bit (bit29) of PLL_CTRL to 0 and then write it to 1.
(5) Wait the Lock bit (bit28) of PLL_CTRL to 1.
(6) Configure PLL_OUTPUT_EN to 1.

3.3.3.5. PLL Disable to PLL Enable

(1) Configure the N, M1, M0 factor of PLL_CTRL_REG.
(2) Write the Enable bit of PLL_CTRL_REG to 1.
(3) Write the Lock Enable bit of PLL_CTRL_REG to 1.
(4) Wait the status of Lock to 1.
(5) Delay 20us, the PLL can be used.

3.3.3.6. PLL Enable to PLL Disable

(1) Write the Enable bit of PLL to 0.
(2) Write the Lock Enable bit (bit29) of PLL_CTRL_REG to 0.

CAUTION

In the normal using of PLL, it is not recommended to switch PLL frequently, because the switch of PLL will cause mutual interference between PLL, which will affect the stability of the system. Therefore, it is recommended to turn off PLL by configuring the PLL_OUTPUT_EN bit of PLL_CTRL to 0, instead of writing 0 to the enable bit.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.3.7. Bus Configuration

The Bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From high frequency to low frequency: switch the clock source first, and then set the frequency division factor;
- From low frequency to high frequency: switch the frequency division factor first, and then switch clock source.

3.3.3.8. Module Clock Configuration

For the bus gating and reset register of modules, the reset is de-asserted first, and then the CLK gating is enabled, to ensure that no problem will occur due to the module not being reset synchronously released.

For module clock, except DDR clock, the other clocks first configure the clock source and frequency division factor, then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, perform as the following rules:

- With the increasing of the clock source frequency, first configure frequency division factor, then configure the clock source;
- With the decreasing of the clock source frequency, first configure the clock source, then configure the frequency division factor.

3.3.3.9. Spread Spectrum Function

3.3.3.9.1. Configuration Process

The configuration of spread spectrum follows the following steps.

Step1: Configure PLL_CTRL Register

- According to PLL frequency and PLL frequency formula, calculate factor N and decimal value X, and write M0、M1、N and PLL frequency to the PLL_CTRL register.
- Configure the SDM_Enable bit(bit24) of the PLL_CTRL register to 1 to enable spread spectrum function.

Step 2: Configure PLL_PAT Register

- According to decimal value X and spread spectrum frequency(the bit[18:17] of the PLL_PAT register), calculate SDM_BOT and WAVE_STEP of PLL_PAT register.
- Configure spread spectrum mode(SPR_FREQ_MODE) to 2 or 3.
- Configure the spread spectrum clock source select bit(SDM_CLK_SEL) to 0 by default. But if the PLL_INPUT_DIV_M1 bit of the PLL_CTRL register is 1, the bit should set to 1.
- Write SDM_BOT、WAVE_STEP、PREQ、SPR_FREQ_MODE and SDM_CLK_SEL to the PLL_PAT register, and configure the SIG_DELT_PAT_EN bit(bit31) of this register to 1.

Step 3: Delay 20us

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.3.9.2. Configuration Instruction

(1).The spread spectrum is an additional low frequency periodic frequency at the desired frequency point, which is not related with the configuration parameters(N, P, M1, M0) of the frequency point.
(2).The parameter M0, P is not related with the configuration of spread spectrum, only used for frequency division configuration.

3.3.3.9.3. Frequency Calculation Formula

$$f = \frac{N+1+X}{P\cdot(M0+1)\cdot(M1+1)}\cdot 24\text{MHz}, 0 < X < 1$$

Where,
P is the frequency division factor of module or PLL;
M0 is the post-frequency division factor of PLL;
M1 is the pre-frequency division factor of PLL;
N is the frequency doubling factor of PLL;
X is the amplitude coefficient of spread spectrum.

NOTE

Having different PLL calculate formula for different PLL, please refer to each PLL_CTRL register.

If selecting M1 = 0, M0 = 0, P = 1(no frequency division)
Then the above formula can be simplified:

$$f = (N+1+X)\cdot 24\text{MHz}, 0 < X < 1$$

- $f_1 \sim f_2 = [N+1+(X_1 \sim X_2)]\cdot 24\text{MHz}$
- $\text{SDM_BOT} = 2^{17}\cdot X1$
- $\text{WAVE_STEP} = 2^{17}\cdot(X2-X1)/(24\text{M/PREQ})*2, 0 < X < 1$

PREQ is the frequency of spread spectrum.

NOTE

For decimal frequency division, the formula can be referenced by it, at this time X1 is equal to X2.

3.3.3.9.4. Configuration Example

Configure 605.3 MHz ~ 609.7 MHz
M0 = 1,
N + 1+ (X1 ~ X2) = (605.3 ~ 609.7) / 24 = [600 + (5.3 ~ 9.7)] / 24 = 24 + 1 + (5.3/24 ~ 9.7/24)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Calculate to get the following values:
N = 24, X1 = 5.3/24, X2 = 9.7/24
SDM_BOT = 2^{17} * X1 = 0x7111
WAVE_STEP = 2^{17} * (X2 – X1) /(24M/PREQ)*2 = 0x3f; PREQ = 31.5 kHz

If M0 = 1, P = 1, then total frequency division factor is (M0 + 1) *1 = 2,
So the actual output frequency of PLL is 1212.1 MHz ~ 1219.4 MHz.
Calculate to get the following values:
N = 49, X1 = 12.1/24, X2 = 19.4/24
Then calculate based on SDM_BOT and WAVE_STEP formula.

3.3.4. Register List

Module Name	Base Address
CCU	0x03001000

Register Name	Offset	Description
PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_DDR_CTRL_REG	0x0010	PLL_DDR Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_GPU_CTRL_REG	0x0030	PLL_GPU Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VIDEO1_CTRL_REG	0x0048	PLL_VIDEO1 Control Register
PLL_VIDEO2_CTRL_REG	0x0050	PLL_VIDEO2 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_COM_CTRL_REG	0x0060	PLL_COM Control Register
PLL_VIDEO3_CTRL_REG	0x0068	PLL_VIDEO3 Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_DDR_PAT0_CTRL_REG	0x0110	PLL_DDR Pattern0 Control Register
PLL_DDR_PAT1_CTRL_REG	0x0114	PLL_DDR Pattern1 Control Register
PLL_PERI0_PAT0_CTRL_REG	0x0120	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x0124	PLL_PERI0 Pattern1 Control Register
PLL_PERI1_PAT0_CTRL_REG	0x0128	PLL_PERI1 Pattern0 Control Register
PLL_PERI1_PAT1_CTRL_REG	0x012C	PLL_PERI1 Pattern1 Control Register
PLL_GPU0_PAT0_CTRL_REG	0x0130	PLL_GPU0 Pattern0 Control Register
PLL_GPU0_PAT1_CTRL_REG	0x0134	PLL_GPU0 Pattern1 Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0140	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x0144	PLL_VIDEO0 Pattern1 Control Register
PLL_VIDEO1_PAT0_CTRL_REG	0x0148	PLL_VIDEO1 Pattern0 Control Register
PLL_VIDEO1_PAT1_CTRL_REG	0x014C	PLL_VIDEO1 Pattern1 Control Register
PLL_VIDEO2_PAT0_CTRL_REG	0x0150	PLL_VIDEO2 Pattern0 Control Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PLL_VIDEO2_PAT1_CTRL_REG	0x0154	PLL_VIDEO2 Pattern1 Control Register
PLL_VE_PAT0_CTRL_REG	0x0158	PLL_VE Pattern0 Control Register
PLL_VE_PAT1_CTRL_REG	0x015C	PLL_VE Pattern1 Control Register
PLL_COM_PAT0_CTRL_REG	0x0160	PLL_COM Pattern0 Control Register
PLL_COM_PAT1_CTRL_REG	0x0164	PLL_COM Pattern1 Control Register
PLL_VIDEO3_PAT0_CTRL_REG	0x0168	PLL_VIDEO3 Pattern0 Control Register
PLL_VIDEO3_PAT1_CTRL_REG	0x016C	PLL_VIDEO3 Pattern1 Control Register
PLL_AUDIO_PAT0_CTRL_REG	0x0178	PLL_AUDIO Pattern0 Control Register
PLL_AUDIO_PAT1_CTRL_REG	0x017C	PLL_AUDIO Pattern1 Control Register
PLL_CPUX_BIAS_REG	0x0300	PLL_CPUX Bias Register
PLL_DDR_BIAS_REG	0x0310	PLL_DDR Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_GPU0_BIAS_REG	0x0330	PLL_GPU0 Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0348	PLL_VIDEO1 Bias Register
PLL_VIDEO2_BIAS_REG	0x0348	PLL_VIDEO2 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register
PLL_COM_BIAS_REG	0x0360	PLL_COM Bias Register
PLL_VIDEO3_BIAS_REG	0x0368	PLL_VIDEO3 Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_CPUX_TUN_REG	0x0400	PLL_CPUX Tuning Register
C0_CPUX_AXI_CFG_REG	0x0500	CPUX_AXI Configuration Register
PSI_AHB1_AHB2_CFG_REG	0x0510	PSI_AHB1_AHB2 Configuration Register
AHB3_CFG_REG	0x051C	AHB3 Configuration Register
APB1_CFG_REG	0x0520	APB1 Configuration Register
APB2_CFG_REG	0x0524	APB2 Configuration Register
MBUS_CFG_REG	0x0540	MBUS Configuration Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
GPU_CORE_CLK_REG	0x0670	GPU Clock Register
GPU_BGR_REG	0x067C	GPU Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	MSGBOX Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	SPINLOCK Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HSTIMER Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PSI_BGR_REG	0x079C	PSI Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NAND0_0_CLK_REG	0x0810	NAND0_0 Clock Register
NAND0_1_CLK_REG	0x0814	NAND0_1 Clock Register
NAND_BGR_REG	0x082C	NAND Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EMAC0_25M_CLK_REG	0x0970	EMAC0_25M Clock Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
IRRX_CLK_REG	0x0990	IRRX Clock Register
IRRX_BGR_REG	0x099C	IRRX Bus Gating Reset Register
IRTX_CLK_REG	0x09C0	IRTX Clock Register
IRTX_BGR_REG	0x09CC	IRTX Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
I2SPCM0_CLK_REG	0x0A10	I2S/PCM0 Clock Register
I2SPCM1_CLK_REG	0x0A14	I2S/PCM1 Clock Register
I2SPCM2_CLK_REG	0x0A18	I2S/PCM2 Clock Register
I2SPCM3_CLK_REG	0x0A1C	I2S/PCM3 Clock Register
I2SPCM_BGR_REG	0x0A20	I2S/PCM Bus Gating Reset Register
OWA_CLK_REG	0x0A24	OWA Clock Register
OWA_BGR_REG	0x0A2C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_CODEC_DAC_1X_CLK_REG	0x0A50	AUDIO CODEC DAC 1X Clock Register
AUDIO_CODEC_ADC_1X_CLK_REG	0x0A54	AUDIO CODEC ADC 1X Clock Register
AUDIO_CODEC_4X_CLK_REG	0x0A58	AUDIO CODEC 4X Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	AUDIO CODEC Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB1_CLK_REG	0x0A74	USB1 Clock Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
LRADC_BGR_REG	0x0A9C	LRADC Bus Gating Reset Register
DPSS_TOP0_BGR_REG	0x0ABC	DPSS_TOP0 Bus Gating Reset Register
DPSS_TOP1_BGR_REG	0x0ACC	DPSS_TOP1 Bus Gating Reset Register
MIPI_DSI_HOST0_CLK_REG	0x0B24	MIPI DSI Host0 Clock Register
MIPI_BGR_REG	0x0B4C	MIPI DSI Bus Gating Reset Register
DISPLAY_IF_TOP_BGR_REG	0x0B5C	DISPLAY_IF_TOP Bus Gating Reset Register
TCON_LCD0_CLK_REG	0x0B60	TCON LCD0 Clock Register
TCON_LCD_BGR_REG	0x0B7C	TCON LCD Bus Gating Reset Register
LVDS_BGR_REG	0x0BAC	LVDS Bus Gating Reset Register
LEDC_CLK_REG	0x0BF0	LEDC Clock Register
LEDC_BGR_REG	0x0BFC	LEDC Bus Gating Reset Register
CSI0_TOP_CLK_REG	0x0C04	CSI0 TOP Clock Register
CSI0_0_MST_CLK_REG	0x0C08	CSI0_0 Master Clock Register
CSI0_1_MST_CLK_REG	0x0C0C	CSI0_1 Master Clock Register
CSI_BGR_REG	0x0C1C	CSI Bus Gating Reset Register
CSI_ISP_CLK_REG	0x0C20	CSI ISP Clock Register
CSI_ISP_BGR_REG	0x0C2C	CSI ISP Bus Gating Reset Register
CCU_SEC_SWITCH_REG	0x0F00	CCU Security Switch Register
PLL_LOCK_DBG_CTRL_REG	0x0F04	PLL Lock Debug Control Register
PLL_CPUX_HW_FM_REG	0x0F20	PLL_CPUX Hardware FM Register

3.3.5. Register Description

3.3.5.1. 0x0000 PLL_CPUX Control Register (Default Value: 0x0A00_1000)

Offset: 0x0000			**Register Name: PLL_CPUX_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_CPUX= InputFreq *N/P **Note: The PLL_CPUX output frequency must be in the range from 200 MHz to 3 GHz. And the default value of PLL_CPUX is 408 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:24	R/W	0x0	PLL_LOCK_TIME. PLL lock time The bit indicates the step amplitude from one frequency to another.
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIVP PLL Output External Divider P 00: 1 01: 2 10: 4 11: / When output clock is less than 288MHz, clock frequency is outputted by dividing P.
15:8	R/W	0x10	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3. PLL_TestFreq=InputFreq*N/P/M. **Note: The bit is only for testing.**

3.3.5.2. 0x0010 PLL_DDR Control Register (Default Value: 0x0800_2301)

Offset: 0x0010			**Register Name: PLL_DDR_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR= InputFreq *N/M0/M1 **Note: When the crystal is 24MHz, the default value of PLL_DDR is 432 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0:Disable 1:Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.3. 0x0020 PLL_PERI0 Control Register (Default Value: 0x0800_3100)

Offset: 0x0020			**Register Name: PLL_PERI0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI0(2X) = 24MHz*N/M0/M1 PLL_PERI0(1X) = 24MHz*N/M0/M1/2 **Note: When the crystal is 24 MHz, the default value of PLL_PERI0(2X) is 1.2 GHz. It is not recommended to modify the value.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:16	/	/	/
15:8	R/W	0x1	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.4. 0x0028 PLL_PERI1 Control Register (Default Value: 0x0800_3100)

Offset: 0x0028			**Register Name: PLL_PERI1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI1(2X) = InputFreq *N/M0/M1. PLL_PERI1(1X) = InputFreq *N/M0/M1/2. **Note: When the crystal is 24 MHz, the default value of PLL_PERI1(2X) is 1.2 GHz. It is not recommended to modify the value.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x31	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.5. 0x0030 PLL_GPU Control Register (Default Value: 0x0800_2301)

Offset: 0x0030			**Register Name: PLL_GPU_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_GPU0 = InputFreq *N/M0/M1. **Note: When the crystal is 24 MHz, the default value of PLL_GPU is 432 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.6. 0x0040 PLL_VIDEO0 Control Register (Default Value: 0x0800_6203)

Offset: 0x0040			**Register Name: PLL_VIDEO0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO0(4X)=InputFreq *N/M PLL_VIDEO0(2X)= InputFreq *N/M/2 PLL_VIDEO0(1X)= InputFreq *N/M/4 **Note: When the crystal is 24 MHz, the default value of PLL_VIDEO0(4X) is 1188 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. The bit is only for testing. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.7. 0x0048 PLL_VIDEO1 Control Register (Default Value: 0x0800_6203)

Offset: 0x0048			**Register Name: PLL_VIDEO1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO1(4X)=InputFreq*N/M. PLL_VIDEO1(2X)=InputFreq*N/M/2. PLL_VIDEO1(1X)= InputFreq*N/M/4. **Note: When the crystal is 24 MHz, the default value of PLL_VIDEO1(4X) is 1188 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. The bit is only for testing. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.8. 0x0050 PLL_VIDEO2 Control Register (Default Value: 0x0800_6203)

Offset: 0x0050			**Register Name: PLL_VIDEO2_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO2(4X)=InputFreq*N/M. PLL_VIDEO2(2X)=InputFreq*N/M/2 PLL_VIDEO2(1X)= InputFreq*N/M/4. **Note: When the crystal is 24 MHz, the default value of PLL_VIDEO2(4X) is 1188 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. The bit is only for testing. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.9. 0x0058 PLL_VE Control Register (Default Value: 0x0800_2301)

Offset: 0x0058			**Register Name: PLL_VE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable The PLL_VE = InputFreq *N/M0/M1. **Note: When the crystal is 24 MHz, the default value of PLL_VE is 432 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.10. 0x0060 PLL_COM Control Register (Default Value: 0x0800_2301)

Offset: 0x0060			**Register Name: PLL_COM_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_COM = InputFreq *N/M0/M1. **Note: When the crystal is 24 MHz, the default value of PLL_COM is 432 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.11. 0x0068 PLL_VIDEO3 Control Register (Default Value: 0x0800_6203)

Offset: 0x0068			**Register Name: PLL_VIDEO3_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO3(4X)=InputFreq*N/M PLL_VIDEO3(2X)=InputFreq*N/M/2 PLL_VIDEO3(1X)= InputFreq*N/M/4 **Note: When the crystal is 24 MHz, the default value of PLL_VIDEO3(4X) is 1188 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. The bit is only for testing. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.12. 0x0078 PLL_AUDIO Control Register (Default Value: 0x0814_5500)

Offset: 0x0078			**Register Name: PLL_AUDIO_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable This PLL is for Audio. PLL_AUDIO(4X) = 24MHz*N/M0/M1/P **7.5≤N/M0/M1≤125 and 12≤N** **The range of 24MHz*N/M0/M1 is from 180 MHz to 3 GHz.** **The default value of PLL_AUDIO(4X) is 98 MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.) **Note: The bit is only valid when the bit29 is set to 1.**
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE Spread Spectrum and Decimal Frequency Division 0: Disable 1: Enable
23:22	/	/	/
21:16	R/W	0x14	PLL_POST_DIV_P PLL Post-div P P= PLL_POST_DIV_P +1 PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x55	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.13. 0x0110 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			**Register Name: PLL_DDR_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.14. 0x0114 PLL_DDR Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.15. 0x0120 PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1bit)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.16. 0x0124 PLL_PERI0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			**Register Name: PLL_PERI0_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.17. 0x0128 PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			**Register Name: PLL_PERI1_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.18. 0x012C PLL_PERI1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x012C			**Register Name: PLL_PERI1_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.19. 0x0130 PLL_GPU0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0130			**Register Name: PLL_GPU0_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.20. 0x0134 PLL_GPU0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0134			**Register Name: PLL_GPU0_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.21. 0x0140 PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			**Register Name: PLL_VIDEO0_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.22. 0x0144 PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.23. 0x0148 PLL_VIDEO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.24. 0x014C PLL_VIDEO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PLL_VIDEO1_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.25. 0x0150 PLL_VIDEO2 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Wave Bottom

3.3.5.26. 0x0154 PLL_VIDEO2 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PLL_VIDEO2_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.27. 0x0158 PLL_VE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.28. 0x015C PLL_VE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PLL_VE_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.29. 0x0160 PLL_COM Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_COM_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.30. 0x0164 PLL_COM Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0164	Register Name: PLL_COM_PAT1_CTRL_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.31. 0x0168 PLL_VIDEO3 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_VIDEO3_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.32. 0x016C PLL_VIDEO3 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PLL_VIDEO3_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.33. 0x0178 PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.34. 0x017C PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16:0	R/W	0x0	FRAC_IN

3.3.5.35. 0x300 PLL_CPUX Bias Register (Default Value: 0x8010_0000)

Offset: 0x0300			Register Name: PLL_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST VCO reset in
30:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CURRENT PLL current bias control [4:0], CPU_CP.
15:0	/	/	/

3.3.5.36. 0x0310 PLL_DDR0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.37. 0x0320 PLL_PERI0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.38. 0x0328 PLL_PERI1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.39. 0x0330 PLL_GPU0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0330			Register Name: PLL_GPU0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.40. 0x0340 PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.41. 0x0348 PLL_VIDEO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_VIDEO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.42. 0x0350 PLL_VIDEO2 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0350			Register Name: PLL_VIDEO2_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.43. 0x0358 PLL_VE Bias Register (Default Value: 0x0003_0000)

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	Read/Write	Default/Hex	Description

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.44. 0x0360 PLL_COM Bias Register (Default Value: 0x0003_0000)

Offset: 0x0360			Register Name: PLL_COM_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.45. 0x0368 PLL_VIDEO3 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0368			Register Name: PLL_VIDEO3_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.46. 0x0378 PLL_AUDIO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.47. 0x0400 PLL_CPUX Tuning Register (Default Value: 0x4440_4000)

Offset: 0x0400			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x4	VCO_RNG_CTRL VCO range control [2:0]
27	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

26:24	R/W	0x4	KVCO_GAIN_CTRL KVCO gain control [2:0]
23	/	/	/
22:16	R/W	0x40	CNT_INIT_CTRL Counter initial control [6:0]
15	R/W	0x0	C_OD0 C-REG-OD0 for verify
14:8	R/W	0x40	C_B_IN C-B-IN [6:0] for verify
7	R/W	0x0	C_OD1 C-REG-OD1 for verify
6:0	RO	0x0	C_B_OUT C-B-OUT [6:0] for verify

3.3.5.48. 0x0500 CPUX_AXI Configuration Register (Default Value: 0x0000_0301)

Offset: 0x0500			**Register Name: CPUX_AXI_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K 010: RC16M 011: PLL_CPUX 100: PLL_PERI0(1X) 101: reserved 110: reserved 111: reserved CPUX Clock = Clock Source CPUX_AXI Clock = Clock Source/M CPUX_APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x3	CPUX_APB_FACTOR_N Factor N.(N = FACTOR_N +1) FACTOR_N is from 0 to 3.
7:2	/	/	/
1:0	R/W	0x1	FACTOR_ M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.49. 0x0510 PSI_AHB1_AHB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PSI_AHB1_AHB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K 010: RC16M 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) PSI_AHB1_AHB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.50. 0x051C AHB3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x051C			Register Name: AHB3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K 010: PSI 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) 0ther: / AHB3 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.51. 0x0520 APB1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K 010: PSI 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) Other: / APB1 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.52. 0x0524 APB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010: PSI 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) Other: / APB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.53. 0x0540 MBUS Configuration Register (Default Value: 0xC000_0000)

Offset: 0x0540			Register Name: MBUS_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M.
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_DDR 10: PLL_PERI0(1X) 11: PLL_PERI0(2X)
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 7.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.54. 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_COM 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.55. 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock For DE 0: Mask 1: Pass

3.3.5.56. 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_COM 001: PLL_PERI0(2X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_VIDEO2(2X) Other: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.57. 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock For G2D 0: Mask 1: Pass

3.3.5.58. 0x0670 GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: GPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Clock Source Select 0: PLL_GPU0 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 7.

3.3.5.59. 0x067C GPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x067C			Register Name: GPU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPU_RST GPU Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPU_GATING Gating Clock for GPU 0: Mask 1: Pass

3.3.5.60. 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.61. 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CE_RST CE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CE_GATING Gating Clock for CE 0: Mask 1: Pass

3.3.5.62. 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_VE 1: PLL_PERI0(2X)
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 7.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.63. 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING Gating Clock for VE 0: Mask 1: Pass

3.3.5.64. 0x070C DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMA_RST DMA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING Gating Clock for DMA 0: Mask 1: Pass

3.3.5.65. 0x071C MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MSGBOX_RST MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MSGBOX_GATING Gating Clock for MSGBOX

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Mask 1: Pass

3.3.5.66. 0x072C SPINLOCK Bus Gating Reset Register (Default: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING Gating Clock for SPINLOCK 0: Mask 1: Pass

3.3.5.67. 0x073C HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST HSTIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING Gating Clock for HSTIMER 0: Mask 1: Pass

3.3.5.68. 0x0740 AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			SCLK = OSC24M.
30:0	/	/	/

3.3.5.69. 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING Gating Clock for DBGSYS 0: Mask 1: Pass

3.3.5.70. 0x079C PSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x079C			Register Name: PSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PSI_RST PSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PSI_GATING Gating Clock for PSI 0: Mask 1: Pass

3.3.5.71. 0x07AC PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST PWM Reset 0: Assert

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING Gating Clock for PWM 0: Mask 1: Pass

3.3.5.72. 0x07BC IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	IOMMU_GATING Gating Clock for IOMMU 0: Mask 1: Pass

3.3.5.73. 0x0800 DRAM Clock Register (Default Value: 0x8000_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30	R/W	0x0	MODULE_RST Module Reset 0: Assert 1: De-assert
29:28	/	/	/
27	R/WAC	0x0	SDRCLK_UPD SDRCLK Configuration 0 update. 0:Invalid 1:Valid Setting this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid.
26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_DDR 01: PLL_PERI1(2X)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Other: /
23:5	/	/	/
4:0	R/W	0x3	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.74. 0x0804 MBUS Master Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	G2D_MCLK_GATING Gating MBUS Clock for G2D 0: Mask 1: Pass
9	R/W	0x0	ISP_MCLK_GATING Gating MBUS Clock for ISP 0: Mask 1: Pass
8	R/W	0x0	CSI0_MCLK_GATING Gating MBUS Clock for CSI0 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	NAND0_MCLK_GATING Gating MBUS Clock for NAND0 0: Mask 1: Pass
4:3	/	/	/
2	R/W	0x0	CE_MCLK_GATING Gating MBUS Clock for CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_GATING Gating MBUS Clock for VE 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_GATING Gating MBUS Clock for DMA 0: Mask 1: Pass

NOTE

DE MCLK is put in DE module to control.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.75. 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DRAM_GATING Gating Clock for DRAM 0: Mask 1: Pass

3.3.5.76. 0x0810 NAND0_0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: NAND0_0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.77. 0x0814 NAND0_1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: NAND0_1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.78. 0x082C NAND Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: NAND_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NAND0_RST NAND0 Reset 0: Assert

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: De-assert
15:1	/	/	/
0	R/W	0x0	NAND0_GATING Gating Clock for NAND0 0: Mask 1: Pass

3.3.5.79. 0x0830 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_PERI1(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.80. 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_PERI1(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.81. 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			**Register Name: SMHC2_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_PERI1(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.82. 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING Gating Clock For SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock For SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock For SMHC0 0: Mask 1: Pass

3.3.5.83. 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R/W	0x0	UART4_RST

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			UART4 Reset 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	UART4_GATING Gating Clock for UART4 0: Mask 1: Pass
3	R/W	0x0	UART3_GATING Gating Clock for UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock for UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock for UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock for UART0 0: Mask 1: Pass

3.3.5.84. 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C	Register Name: TWI_BGR_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	TWI3_GATING Gating Clock for TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock for TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock for TWI1 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING Gating Clock for TWI0 0: Mask 1: Pass

3.3.5.85. 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.86. 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			**Register Name: SPI1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.87. 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.88. 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:19	/	/	/
18	R/W	0x0	SPI2_RST SPI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SPI2_GATING Gating Clock for SPI2 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING Gating Clock for SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING Gating Clock for SPI0 0: Mask 1: Pass

3.3.5.89. 0x0970 EMAC0_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			**Register Name: EMAC0_25M_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EMAC0_25M_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON CLK =PLL_PERI0(1X)/24=25
30	R/W	0x0	EMAC0_25M_CLK_SRC_GATING Gating the Source Clock of Special Clock 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.90. 0x097C EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMAC0_RST EMAC0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC0_GATING Gating Clock for EMAC0 0: Mask 1: Pass

3.3.5.91. 0x0990 IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0990			Register Name: IRRX_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IRRT CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: clk32k 001: OSC24M 010: PLL_PERI0(1X) 011: PLL_PERI1(1X) Other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.92. 0x099C IRRX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x099C			Register Name: IRRX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	IRRX_RST IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRRX_GATING Gating Clock for IRRX 0: Mask 1: Pass

3.3.5.93. 0x09C0 IRTX Clock Register (Default Value: 0x0000_0000)

Offset: 0x09C0			Register Name: IRTX_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IRTX CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: clk32k 001: OSC24M 010: PLL_PERI0(1X) 011: PLL_PERI1(1X) Other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.94. 0x09CC IRTX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09CC			Register Name: IRTX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	IRTX_RST IRTX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRTX_GATING Gating Clock for IRTX 0: Mask 1: Pass

3.3.5.95. 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPADC_RST GPADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING Gating Clock for GPADC 0: Mask 1: Pass

3.3.5.96. 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	THS_RST THS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING Gating Clock for THS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Mask 1: Pass

3.3.5.97. 0x0A10 I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A10			Register Name: I2SPCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO(divided 5 by PLL_COM) other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.98. 0x0A14 I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2SPCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.99. 0x0A18 I2S/PCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A18			Register Name: I2SPCM2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.100. 0x0A1C I2S/PCM3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A1C			Register Name: I2SPCM3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.101. 0x0A20 I2S/PCM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: I2SPCM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	I2S/PCM3_RST I2S/PCM3 Reset 0: Assert 1: De-assert
18	R/W	0x0	I2S/PCM2_RST I2S/PCM2 Reset 0: Assert 1: De-assert
17	R/W	0x0	I2S/PCM1_RST I2S/PCM1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S/PCM0_RST I2S/PCM0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	I2S/PCM3_GATING Gating Clock for I2S/PCM3 0: Mask 1: Pass
2	R/W	0x0	I2S/PCM2_GATING Gating Clock for I2S/PCM2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Mask 1: Pass
1	R/W	0x0	I2S/PCM1_GATING Gating Clock for I2S/PCM1 0: Mask 1: Pass
0	R/W	0x0	I2S/PCM0_GATING Gating Clock for I2S/PCM0 0: Mask 1: Pass

3.3.5.102. 0x0A24 OWA Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A24			Register Name: OWA_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.103. 0x0A2C OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A2C			Register Name: OWA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	OWA_RST OWA Reset

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING Gating Clock for OWA 0: Mask 1: Pass

3.3.5.104. 0x0A40 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: DMIC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.105. 0x0A4C DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert
15:1	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x0	DMIC_GATING Gating Clock for DMIC 0: Mask 1: Pass

3.3.5.106. 0x0A50 AUDIO CODEC DAC 1X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_DAC_1X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.107. 0x0A54 AUDIO CODEC ADC 1X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A54			Register Name: AUDIO_CODEC_ADC_1X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.108. 0x0A58 AUDIO CODEC 4X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A58			Register Name: AUDIO_CODEC_4X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO(4X) 01: PLL_COM_AUDIO other: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.109. 0x0A5C AUDIO CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A5C			Register Name: AUDIO_CODEC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST AUDIO_CODEC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING Gating Clock for AUDIO_CODEC 0: Mask 1: Pass

3.3.5.110. 0x0A70 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70	Register Name: USB0_CLK_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING_OHCI0 Gating Special Clock for OHCI0 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY0_RST USB PHY0 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY0 Gating Special Clock for USBPHY0 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M.
28:26	/	/	/
25:24	R/W	0x0	OHCI0_12M_SRC_SEL OHCI0 12M Source Select 00: 12M divided from OHCI_48M 01: 12M divided from OSC24M 10: LOSC 11: RC16M
23:0	/	/	/

3.3.5.111. 0x0A74 USB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A74			Register Name: USB1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_OHCI1 Gating Special Clock for OHCI1 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY1_RST USB PHY1 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY1 Gating Special Clock for USBPHY1 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M.
28:26	/	/	/
25:24	R/W	0x0	OHCI1_12M_SRC_SEL OHCI1 12M Source Select 00: 12M divided from OHCI_48M

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: 12M divided from OSC24M 10: LOSC 11: RC16M
23:0	/	/	/

3.3.5.112. 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USBOTG_RST USBOTG Reset 0: Assert 1: De-assert
23:22	/	/	/
21	R/W	0x0	USBEHCI1_RST USBEHCI1 Reset 0: Assert 1: De-assert
20	R/W	0x0	USBEHCI0_RST USBEHCI0 Reset 0: Assert 1: De-assert
19:18	/	/	/
17	R/W	0x0	USBOHCI1_RST USBOHCI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	USBOHCI0_RST USBOHCI0 Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBOTG_GATING Gating Clock for USBOTG 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	USBEHCI1_GATING Gating Clock for USBEHCI1 0: Mask 1: Pass
4	R/W	0x0	USBEHCI0_GATING

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Gating Clock for USBEHCI0 0: Mask 1: Pass
3:2	/	/	/
1	R/W	0x0	USBOHCI1_GATING Gating Clock for USBOHCI1 0: Mask 1: Pass
0	R/W	0x0	USBOHCI0_GATING Gating Clock for USBOHCI0 0: Mask 1: Pass

3.3.5.113. 0xA9C LRADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A9C			Register Name: LRADC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LRADC_RST LRADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LRADC_GATING Gating Clock for LRADC 0: Mask 1: Pass

3.3.5.114. 0x0ABC DPSS_TOP0 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: DPSS_TOP0_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DPSS_TOP0_RST DPSS_TOP0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DPSS_TOP0_GATING Gating Clock for DPSS_TOP0 0: Mask 1: Pass

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.115. 0x0ACC DPSS_TOP1 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ACC			Register Name: DPSS_TOP1_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DPSS_TOP1_RST DPSS_TOP1 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DPSS_TOP1_GATING Gating Clock for DPSS_TOP1 0: Mask 1: Pass

3.3.5.116. 0x0B24 MIPI DSI Host0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: MIPI_DSI_HOST0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_PERI0(1X) 11:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.117. 0x0B4C MIPI DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: MIPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:17	/	/	/
16	R/W	0x0	MIPI_DSI0_RST MIPI_DSI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MIPI_DSI0_GATING Gating Clock for MIPI_DSI0 0: Mask 1: Pass

3.3.5.118. 0x0B60 TCON LCD0 Clock Register(Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCON_LCD0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(4X) 001: PLL_VIDEO1(4X) 010: PLL_VIDEO2(4X) 011: PLL_VIDEO3(4X) 100: PLL_PERI0(2X) other: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.119. 0x0B7C TCON LCD Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCON_LCD_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_LCD0_RST TCON_LCD0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_LCD0_GATING Gating Clock for TCON_LCD0 0: Mask 1: Pass

3.3.5.120. 0x0BAC LVDS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BAC			Register Name: LVDS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LVDS0_RST LVDS0 Reset 0: Assert 1: De-assert
15:0	/	/	/

3.3.5.121. 0x0BF0 LEDC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BF0			Register Name: LEDC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) Other: /
23:10	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.122. 0x0BFC LEDC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BFC			Register Name: LEDC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LEDC_RST LEDC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LEDC_GATING Gating Clock for LEDC 0: Mask 1: Pass

3.3.5.123. 0x0C04 CSI TOP Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_TOP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000:PLL_PERI0(2X) 001:PLL_VIDEO0(2X) 010:PLL_VIDEO1(2X) 011:PLL_VIDEO2(2X)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100:PLL_VIDEO3(2X) Others:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.124. 0x0C08 CSI0_0 Master Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI0_0_MST_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK0_GATING Gating CSI Master Clock0, this clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO2(1X) 010: PLL_VIDEO3(1X) 011: PLL_VIDEO0(1X) 100: PLL_VIDEO1(1X) Others: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.125. 0x0C0C CSI0_1 Master Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI0_1_MST_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK1_GATING Gating CSI0 Master Clock1, this clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			000: OSC24M 001: PLL_VIDEO3(1X) 010: PLL_VIDEO0(1X) 011: PLL_VIDEO1(1X) 100: PLL_VIDEO2(1X) Others: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.126. 0x0C1C CSI Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0C1C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI0_RST CSI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI0_GATING Gating Clock for CSI0 0: Mask 1: Pass

3.3.5.127. 0x0C20 CSI0 ISP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C20			Register Name: CSI0_ISP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MISP_GATING Gating CSI0 ISP Clock, this clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000:PLL_PERI0(2X) 001:PLL_VIDEO0(2X) 010:PLL_VIDEO1(2X) 011:PLL_VIDEO2(2X)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100:PLL_VIDEO3(2X) Others: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.128. 0x0C2C CSI ISP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_ISP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_ISP_RST CSI_ISP Reset 0: Assert 1: De-assert
15:0	/	/	/

3.3.5.129. 0x0F00 CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCU_SEC_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MBUS_SEC MBUS clock registers' security 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC Bus relevant registers' security 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC PLL relevant registers' security 0: Secure 1: Non-secure

NOTE

If the secure bit in SID module has not been programed, the register is invalid.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.5.130. 0x0F04 PLL Lock Debug Control Register(Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: PLL_LOCK_DBG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBG_EN Debug Enable 0: Disable 1: Enable
30:25	/	/	/
24:20	R/W	0x0	DBG_SEL Debug Select 00000: PLL_CPUX 00001: / 00010: PLL_DDR 00011:/ 00100: PLL_PERI0(2X) 00101: PLL_PERI1(2X) 00110:PLL_GPU0 00111:/ 01000: PLL_VIDEO0(4X) 01001: PLL_VIDEO1(4X) 01010: PLL_VIDEO2(4X) 01011: PLL_VE 01100: PLL_COM 01101: PLL_VIDEO3(4X) 01110: / 01111: PLL_AUDIO 10000: / 10001: / 10010: / 10011: / 10100: / 10101: / 10110: / 10111: / 11000: / 11001: / 11010: / Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
15:0	/	/	/

3.3.5.131. 0x0F20 PLL_CPUX Hardware FM Register (Default Value: 0x0000_0000)

Offset: 0x0F20			**Register Name: PLL_CPUX_HW_FM_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_CPUX_MODE 0:Normal Mode 1:Hardware FM Mode In normal mode, the frequency of PLL_CPUX depends on the configuration of PLL_CPUX_CTRL_REG. In hardware FM mode, PLL_CPUX uses hardware frequency modulation mode.
30	R	0x0	PMU_FLAG 0:Unlock 1:Lock
29:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIV P PLL Output external divider P 00:1 01:2 10:4 11:/
15:8	R/W	0x0	PLL_FACTOR_N PLL Factor N N=PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M=PLL_FACTOR_M+1 PLL_FACTOR_M is from 0 to 3. **Note: M has no effect on the frequency of CPU.**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4. BROM System

3.4.1. Overview

The BROM system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) which could be considered the primary program-loader. On startup process, the SoC starts to fetch the first instruction from address 0x0, where is the BROM located.

The BROM system divides into two parts: FEL and Media Boot. The task of FEL is to write the external data to the local NVM, the task of the Media Boot is to load an effective and legitimate BOOT0 from NVM and running.

The BROM system includes the following features:

- CPU0 boot process
- Mandatory upgrade process through SMHC0, USB
- Supports GPIO pin to select the kind of boot media to boot
- Supports GPADC to select the kind of boot media to boot
- Supports efuse to select the kind of boot media to boot
- Supports normal boot and secure boot
- Supports loading only-certified firmware
- Ensure that Secure Boot is a trusted environment

3.4.2. Operations and Functional Descriptions

3.4.2.1. Boot Media Select

The BROM system supports the following boot media:

- SD/eMMC
- Nand Flash
- SPI NOR Flash
- SPI NAND Flash

There are three ways of Boot Select: **GPIO Pin Select, GPADC Select** and **eFuse Select**. On startup, the BROM will read the state of BOOT_MODE, according to the state of BOOT_MODE to decide which way to select the kind of boot media to boot. The BOOT_MODE is actually the BROM_CONFIG at efuse mapping (the lowest 2 bits of the REG[0x03006210] at the SID). Table 3-2 shows BOOT_MODE Setting.

Table 3- 2. BOOT_MODE Setting

BOOT_MODE[0:1]	Boot Select Type
00	GPADC Select
01	GPIO Pin Select
10	eFuse Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	reserved

3.4.2.1.1. GPADC Boot Select

If the state of the BOOT_MODE is 00, that is to choose the GPADC SELECT. Table 3-3 show GPADC Boot Select Setting.

Table 3- 3. GPADC Boot Select Setting

KEY_VALUE	Boot Select type
0x00~0xb6	SMHC0->MLC NAND->SLC NAND
0xb7~0x22b	SMHC0->SLC NAND->MLC NAND
0x22c~0x3af	SMHC0->EMMC_BOOT->EMMC_USER
0x3b0~0x57b	SMHC0->EMMC_USER->EMMC_BOOT
0x57c~0x73c	SMHC0->SPI NOR
0x73d~0x8cc	SMHC0->SPI NAND
0x8cd~0xfff	reserved

3.4.2.1.2. GPIO Boot Select

If the state of the BOOT_MODE is 01, that is to choose GPIO pin. And in GPIO pin mode, there is one pin (The status of the boot select pin is the bit9 of the REG[0x03000024] at the system configuration module) to select which boot media to boot. Table 3-4 shows boot media devices in GPIO pin mode.

Table 3- 4. GPIO Pin Boot Select Configuration

Pin_Boot_Select[13]	Boot Media
0	SMHC0->NAND FLASH->EMMC2->SPI NOR->SPI NAND
1	SMHC0->EMMC2->NAND FLASH->SPI NOR->SPI NAND

3.4.2.1.3. Efuse Boot Select

If the state of the BOOT_MODE is 10, that is to choose the eFuse type. The eFuse type has one 12 bits configuration (The status of the efuse boot select pin is the bit16 to bit27 of the REG[0x03006210] at SID module), every 3 bits is divided into a group of the Boot Select, so it has four groups of boot_select. Table 3-5 shows eFuse Boot Select Configuration.

Table 3- 5. eFuse Boot Select Configuration

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 3-6 describes each group of the eFuse Boot Select Setting. The first group to the third group are the same settings, but the fourth group need to be careful. If eFuse_Boot_Select_7 is set to 111, that means the way of the *Try*. The way of *Try* is followed by SMHC0, SMHC2, Nand Flash, SPI NOR Flash, SPI NAND Flash.

Table 3- 6. eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot Media
000	Try
001	SLC NAND Flash
010	SMHC2
011	SPI NOR Flash
100	SPI NAND Flash
101	MLC NAND Flash
110	Reserved
111	The next a group of the eFuse_Boot_Select, but when the n is equal to 7, it will be a way of Try.

3.4.2.2. BROM Process

In Normal boot mode, the system boot will start from CPU0. Then BROM will read the state of the FEL Pin, if the FEL Pin signal is detected pulling to high level, then the system will jump to the Fast Boot process, or jump to the mandatory upgrade process. Figure 3-6 shows the BROM Process.

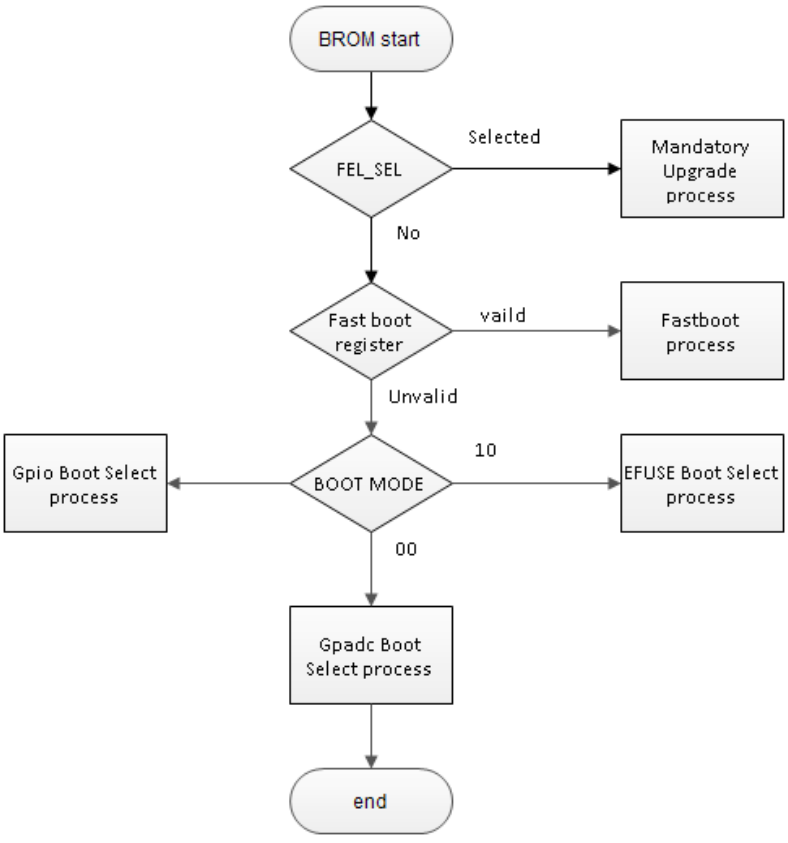


Figure 3- 6. Boot Process Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4.2.3. Secure BROM Process

The Secure BROM supports the following features:

- Supports X509 certificate
- Supports cryptographic algorithms: AES-128, SHA-256, RSA-2048, DES
- Supports OTP/eFuse

Before runing Security Boot, software must check whether it has been modified or replaced, so the system will check and verify the integrity of the certificate, because the certificate has been using the RSA algorithm signature. The system also uses the Crypto Engine (CE) hardware module to accelerate the speed of encryption and decryption. Using standard cryptography ensure that the firmware images can be trusted, so the Secure BROM ensure the system security state is as expected.

3.4.2.4. BROM Process Description

3.4.2.4.1. Mandatory Upgrade Process

When the system chooses to whether enter Mandatory Upgrade Processor, if the FEL signal is detected pulling to low level, then the system will jump to the Mandatory Upgrade Process. Figure 3-7 shows the mandatory upgrade process.

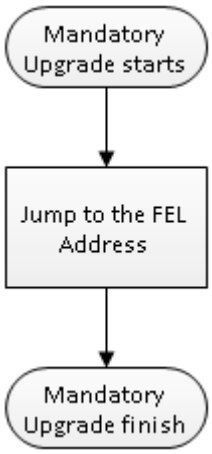


Figure 3- 7. Mandatory Upgrade Process

NOTE

The FEL address of the Normal BROM is 0x20.

The FEL Address of the Secure BROM is 0x64.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4.2.4.2. FEL Process

When the system chooses to enter Mandatory Upgrade Process, then the system will jump to the FEL process. Figure 3-8 shows the FEL upgrade process.

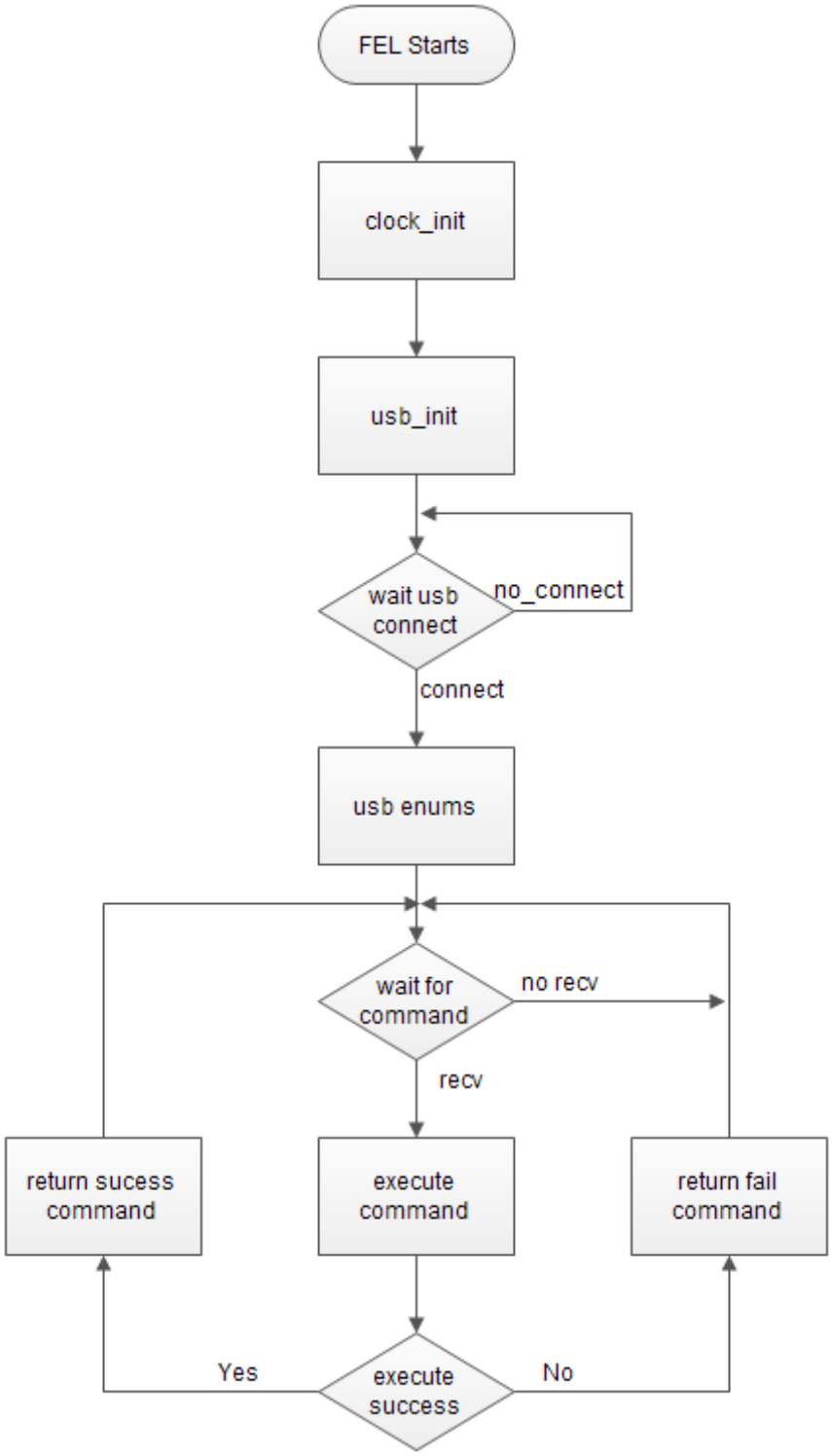


Figure 3- 8. USB FEL Process

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4.2.4.3. Fast Boot Process

If the value of the Fast Boot register is not zero, the system chooses to enter the Fast Boot Process. Table 3-7 shows Fast Boot Select Setting.

Table 3- 7. Fast Boot Select Setting

Reg_bit[31:28]	Boot Select Type
1	SMHC0->MLC NAND->SLC NAND
2	SMHC0->EMMC_USER->EMMC_BOOT
3	SMHC0->SPI NOR
4	SMHC0->SPI NAND
5	SMHC0->EMMC_BOOT->EMMC_USER
6	SMHC0->SLC NAND-> MLC NAND
7	reserved

NOTE

The address of Fast Boot is 0x07000120.

The bit[28:0] of Fast Boot register is used to record the media information.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.5. System Configuration

3.5.1. Overview

The system configuration module is used to configure parameter for system domain, such as SRAM, CPU, PLL, BROM, and so on.

The address range of SRAM is as follows.

Area	Address	Size
SRAM A1	0x0002 0000---0x0002 3FFF	16 KB(Supports Byte operation, the clock source is AHB1)
SRAM C	0x0002 4000---0x0004 4FFF	Borrow VE 112 KB, DE 20KB, supports Byte operation, clock source can be switched to AHB1.
SRAM A2	0x0010 0000---0x0011 3FFF	16 KB + 64 KB 0x0010 0000---0x00103FFF: only store CPUS Vector Table, and only 16 addresses are valid,0x00100100,0x00100200...0x00100F00. See Openrisc, the real space of SRAM A2 is 0x00104000---0x0011 3FFF.

3.5.2. Operations and Functional Descriptions

3.5.2.1. SRAM

The system SRAM includes SRAM A1 and SRAM C. The address between SRAM A1 and SRAM C is continuous.

The SRAM A1 is used in System area, the SRAM C is a memory which system borrows from specific module(such as DE, VE), only in special scene(such as BOOT, STANDBY, etc), the SRAM C will switch to system to use.

When the SRAM of the module switchs to SRAM C, then the clock of the SRAM switchs to AHB1, if using SRAM C, the switch needs be opened, and the bus gating of the module needs be opened, the SRAM can be accessed.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6. Timer

3.6.1. Overview

The timer module implements the timing and counting functions. The timer module includes timer0, timer1, watchdog and AVS0, AVS1.

The timer 0 and timer 1 are completely consistent. The timer 0 and timer 1 have the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transmit a reset signal to reset the entire system after an exception occurs in the system. The watchdog has the following features:

- Single clock source: OSC24M/750
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent. The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Pause/Start function

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.2. Block Diagram

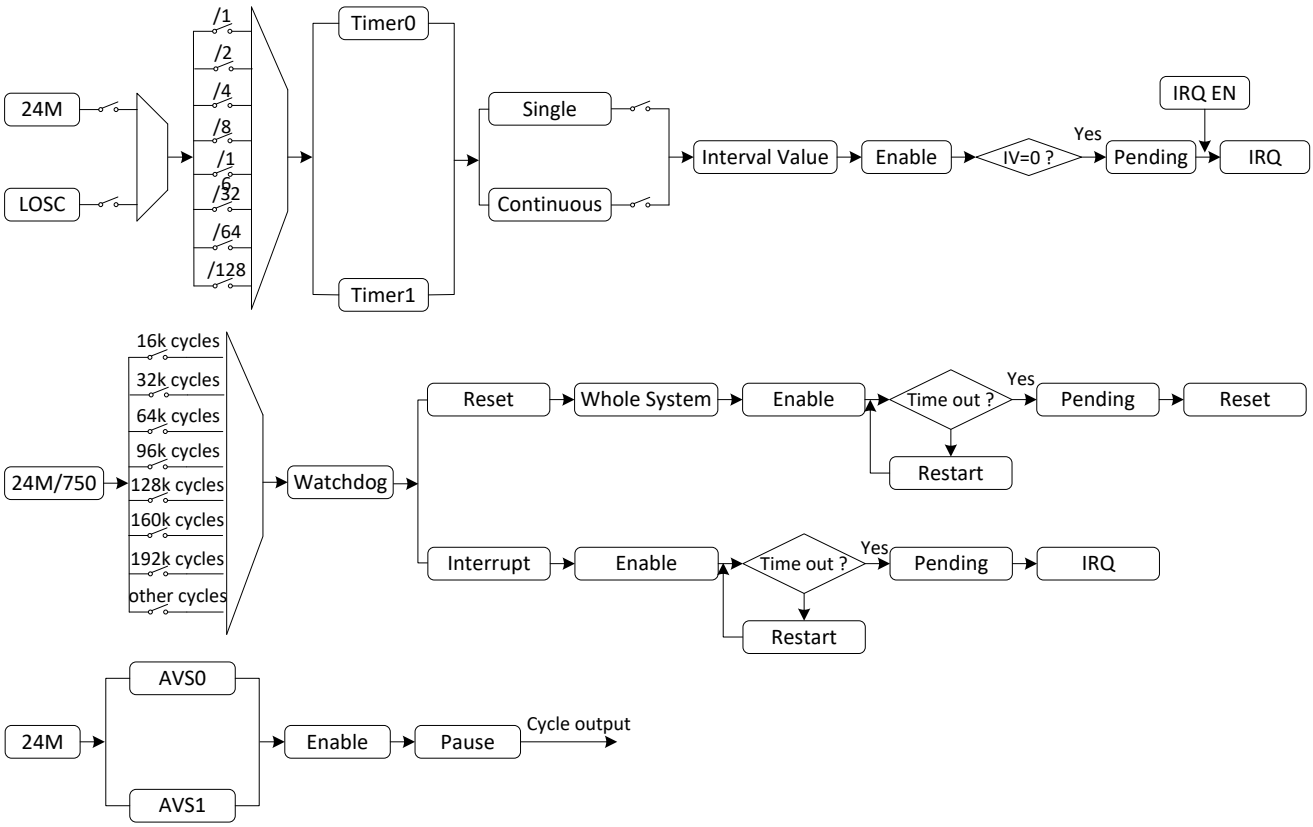


Figure 3- 9. Timer Block Diagram

3.6.3. Operations and Functional Descriptions

3.6.3.1. Timer Formula

Using Timer0 as an example.

$$T_{timer0} = \frac{TMR0_INTV_VALUE_REG - TMR0_CUR_VALUE_REG}{TMR0_CLK_SRC} \times TMR0_CLK_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;
TMR0_CUR_VALUE_REG: timer current counter;
TMR0_CLK_SRC: timer clock source;
TMR0_CLK_PRES: timer clock prescale ratio.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.3.2. Typical Application

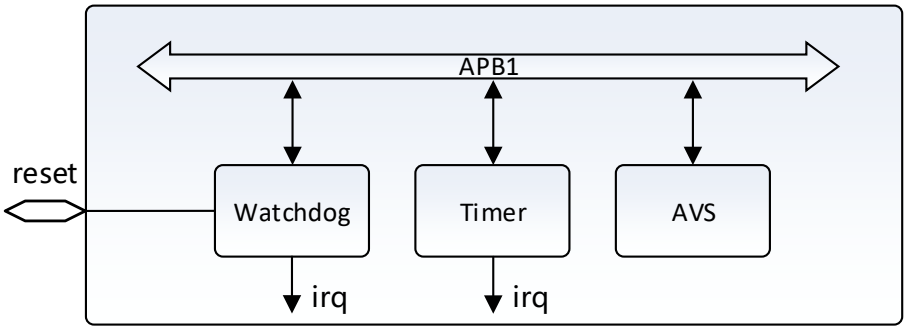


Figure 3- 10. Timer Application Diagram

Timer, watchdog and AVS configure register by APB1 bus.
Timer and watchdog have interrupt mode.
The system configures the time of watchdog, if the system has no timing for restart watchdog(such as bus hang dead), then watchdog sends out watchdog reset external signal to reset system; meanwhile watchdog outputs signal to RESET pad to reset PMIC.

3.6.3.3. Function Implemention

3.6.3.3.1. Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- **Continuous mode**

The bit7 of the TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- **Single mode**

The bit7 of the TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

3.6.3.3.2. Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The watchdog has two operating modes.

- **Interrupt mode**

The WDOG0_CFG_REG is set to 0x2, when the counter value reaches 0 and WDOG0_IRQ_EN_REG is enabled, the watchdog generates an interrupt, the watchdog enters into interrupt mode.

- **Reset mode**

The WDOG0_CFG_REG is set to 0x1, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

The clock source of the watchdog is OSC24M/750. There are 12 configurable initial count values.
The watchdog can restart to count by setting the WDOG0_CTRL_REG: write 0xA57 to bit[12:1], then write 1 to bit[0].

3.6.3.3.3. AVS

The AVS is a 33-bit up counter. The counter value is increased by 1 on each rising edge of the count clock.
The AVS can be operated after its clock gating in CCU module is opened.
The AVS has an OSC24M clock source and a 12-bit division factor(N1 or N2). When the timer increases to N1 or N2 from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit, the AVS will start to count from initial value again.
In counter working process, the division factor and initial counter of the AVS can be changed anytime. And the AVS can stop or start to operate counter anytime.

3.6.3.4. Operating Mode

3.6.3.4.1. Timer Initial

(1) Configure the timer parameters: clock source, prescale factor, working mode. The configuration of these parameters have no sequence, and can be implemented by writing **TMRn_CTRL_REG**.
(2) Write the initial value: write **TMRn_INTV_VALUE_REG** to provide an initial value for the timer; write the bit[1] of **TMRn_CTRL_REG** to load the initial value to the timer, if the bit[1] is 1, writing operation cannot perform; if is 0, this indicates successful loading.
(3) Enable timer: write the bit[0] of **TMRn_CTRL_REG** to enable timer count; read **TMRn_CUR_VALUE_REG** to get the current count value.

3.6.3.4.2. Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of **TMR_IRQ_EN_REG**, when timer counter time reaches, the corresponding interrupt generates.
(2) After enter interrupt process, write **TMR_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.3.4.3. Watchdog Initial

(1) Write **WDOG0_CFG_REG** to configure the generation of the interrupts and the output of reset signal.
(2) Write **WDOG0_MODE_REG** to configure the initial count value.
(3) Write **WDOG0_MODE_REG** to enable the watchdog.

3.6.3.4.4. Watchdog Interrupt

Watchdog interrupt is only used for the counter.
(1) Write **WDOG0_IRQ_EN_REG** to enable the interrupt.
(2) After enter the interrupt process, write **WDOG0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.5. AVS Start/Pause

(1) Write **AVS_CNT_DIV_REG** to configure the division factor.
(2) Write **AVS_CNT_REG** to configure the initial count value.
(3) Write **AVS_CNT_CTL_REG** to enable AVS counter. AVS counter can be paused at any time.

3.6.4. Programming Guidelines

3.6.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                  //Set interval value
writel(0x94, TMR_0_CTRL);                   //Select Single mode, 24 MHz clock source, 2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);            //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```

3.6.4.2. Watchdog Reset

In the following instance making configurations for Watchdog: configure clock source as 24M/750, configure Interval Value as 1s and configure Watchdog Configuration as To whole system. This instance indicates that reset system after 1s.

```
writel(0x1, WDOG_CONFIG);                   //To whole system
writel(0x10, WDOG_MODE);                    //Interval Value set 1s
```

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

```
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);     //Enable Watchdog
```

3.6.4.3. Watchdog Restart

In the following instance making configurations for Watchdog: configure clock source as 24M/750, configure Interval Value as 1s and configure Watchdog Configuration as To whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG_CONFIG);                       //To whole system
writel(0x10, WDOG_MODE);                        //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);     //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL); //Write 0xA57 at Key Field and Restart Watchdog
```

3.6.5. Register List

Module Name	Base Address
Timer	0x03009000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_SOFT_RST_REG	0x00A8	Watchdog Software Reset Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
WDOG_OUTPUT_CFG_REG	0x00BC	Watchdog Output Configuration Register
AVS_CNT_CTL_REG	0x00C0	AVS Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Divisor Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.6. Register Description

3.6.6.1. 0x0000 Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	TMR1_IRQ_EN Timer 1 Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	TMR0_IRQ_EN Timer 0 Interrupt Enable 0: Disable 1: Enable

3.6.6.2. 0x0004 Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

3.6.6.3. 0x0010 Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE Timer 0 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD Timer 0 Reload 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN Timer 0 Enable 0: Stop/Pause 1: Start If the timer starts, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer starts again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.4. 0x0014 Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE Timer 0 Interval Value

NOTE

The value setting should consider the system clock and the timer clock source.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.6.5. 0x0018 Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE Timer 0 Current Value Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.6. 0x0020 Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE Timer 1 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES Select the pre-scale of timer 1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC 00: LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD Timer 1 Reload 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR1_EN Timer 1 Enable 0: Stop/Pause 1: Start If the timer starts, it will reload the interval value to internal register, and the

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer starts again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.7. 0x0024 Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE Timer 1 Interval Value

NOTE

The value should consider the system clock and the timer clock source.

3.6.6.8. 0x0028 Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE Timer 1 Current Value Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.9. 0x00A0 Watchdog IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name:WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG_IRQ_EN Watchdog Interrupt Enable 0: Disable 1: Enable

3.6.6.10. 0x00A4 Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4	Register Name:WDOG_IRQ_STA_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ _PEND Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending. Watchdog interval value is reached.

3.6.6.11. Watchdog Software Reset Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name:WDOG_SOFT_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15:1	/	/	/
0	R/W1C	0x0	Soft Reset Enable 0: De-assert 1: Reset System If the system is reset by the bit, the watchdog function need be disabled.

3.6.6.12. 0x00B0 Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name:WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the Watchdog

3.6.6.13. 0x00B4 Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name:WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG 00: /

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: To whole system 10: Only interrupt 11: /

3.6.6.14. 0x00B8 Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name:WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE Watchdog Interval Value Watchdog clock source is OSC24M/750. If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) Others: Reserved
3:1	/	/	/
0	R/W	0x0	WDOG_EN Watchdog Enable 0: Disable 1: Enable

3.6.6.15. Watchdog Output Config Register (Default Value: 0x0000_001F)

Offset: 0x00BC			Register Name:WDOG_OUTPUT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x1F	Wdog output config Wdog rst valid time config T=1/32ms*(N+1) Default 1ms

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.6.16. 0x00C0 AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/Disable The counter source is OSC24M. 0: Disable 1: Enable

3.6.6.17. 0x00C4 AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter will not increase.

3.6.6.18. 0x00C8 AVS Counter 1 Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name:AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter will not increase.

3.6.6.19. 0x00CC AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			**Register Name: AVS_CNT_DIV_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7. R_Timer

3.7.1. Overview

The R_Timer0, R_Timer1, R_Timer2, and R_Timer3 have the following features:

- Configurable count clock: LOSC and OSC. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

3.7.2. Block Diagram

Figure 3-11 shows a block diagram of the R_Timer.

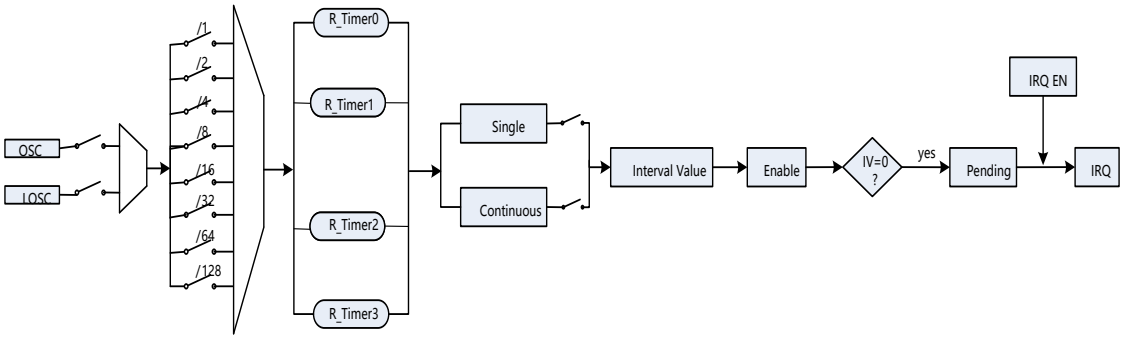


Figure 3- 11. R_Timer Block Diagram

3.7.3. Operations and Functional Descriptions

3.7.3.1. R_Timer Formula

Using R_Timer0 as an example.

$$T_{R_timer0} = \frac{RTMR0_INTV_VALUE_REG - RTMR0_CUR_VALUE_REG}{RTMR0_CLK_SRC} \times RTMR0_CLK_PRES$$

RTMR0_INTV_VALUE_REG: R_Timer initial value;
RTMR0_CUR_VALUE_REG: R_Timer current counter;
RTMR0_CLK_SRC: R_Timer clock source;
RTMR0_CLK_PRES: R_Timer clock prescale ratio.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.2. Typical Application

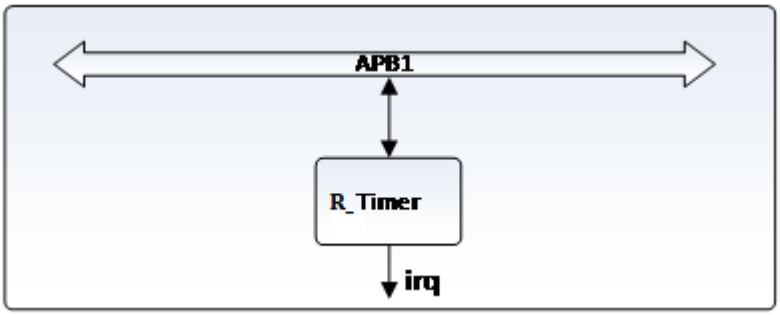


Figure 3- 12. R_Timer Application Diagram

R_Timer configure register by APB1 bus.
R_Timer has interrupt mode.

3.7.3.3. Function Implemention

3.7.3.3.1. R_Timer

The R_Timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each R_Timer has independent interrupt.

The R_Timer has two operating modes.

- **Continuous mode**

The bit7 of the RTMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the R_Timer module reloads data from RTMRn_INTV_VALUE_REG then continues to count.

- **Single mode**

The bit7 of the RTMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the R_Timer stops counting. The R_Timer starts to count again only when a new initial value is loaded.

Each R_Timer has a prescaler that divides the working clock frequency of each R_Timer by 1,2,4,8,16,32,64,128.

3.7.3.4. Operating Mode

3.7.3.4.1. R_Timer Initial

(1) Configure the R_Timer parameters: clock source, prescale factor, working mode. The configuration of these parameters have no sequence, and can be implemented by writing **RTMRn_CTRL_REG**.
(2) Write the initial value: write **RTMRn_INTV_VALUE_REG** to provide an initial value for the R_Timer; write the bit[1] of **RTMRn_CTRL_REG** to load the initial value to the R_Timer, if the bit[1] is 1, writing operation cannot perform; if

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

is 0, this indicates successful loading.

(3) Enable R_Timer: write the bit[0] of **RTMRn_CTRL_REG** to enable R_Timer count; read **RTMRn_CUR_VALUE_REG** to get the current count value.

3.7.3.4.2. R_Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of **RTMR_IRQ_EN_REG**, when R_Timer counter time reaches, the corresponding interrupt generates.

(2) After enter interrupt process, write **RTMR_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

3.7.4. Programming Guidelines

3.7.4.1. R_Timer

Take making a 1ms delay for an example, OSC clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0, RTMR0_INTV_VALUE_REG);                    //Set interval value
writel(0x94, RTMR0_CTRL_REG);                    //Select Single mode, OSC clock source, 2 pre-scale
writel(readl(RTMR0_CTRL_REG)|(1<<1), RTMR0_CTRL_REG);    //Set Reload bit
while((readl(RTMR0_CTRL_REG)>>1)&1);                    //Waiting Reload bit turns to 0
writel(readl(RTMR0_CTRL_REG)|(1<<0), RTMR0_CTRL_REG);    //Enable R_Timer0
While(!(readl(RTMR_IRQ_STA_REG)&1));                    //Wait for R_Timer0 counter to count down to 0
Writel(1, RTMR_IRQ_STA_REG);
```

3.7.5. Register List

Module Name	Base Address
R_Timer	0x0702 0000

Register Name	Offset	Description
RTMR_IRQ_EN_REG	0x0000	R_Timer IRQ Enable Register
RTMR_IRQ_STA_REG	0x0004	R_Timer Status Register
RTMR0_CTRL_REG	0x0010	R_Timer 0 Control Register
RTMR0_INTV_VALUE_REG	0x0014	R_Timer 0 Interval Value Register
RTMR0_CUR_VALUE_REG	0x0018	R_Timer 0 Current Value Register
RTMR1_CTRL_REG	0x0020	R_Timer 1 Control Register
RTMR1_INTV_VALUE_REG	0x0024	R_Timer 1 Interval Value Register
RTMR1_CUR_VALUE_REG	0x0028	R_Timer 1 Current Value Register
RTMR2_CTRL_REG	0x0030	R_Timer 2 Control Register
RTMR2_INTV_VALUE_REG	0x0034	R_Timer 2 Interval Value Register
RTMR2_CUR_VALUE_REG	0x0038	R_Timer 2 Current Value Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

RTMR3_CTRL_REG	0x0040	R_Timer 3 Control Register
RTMR3_INTV_VALUE_REG	0x0044	R_Timer 3 Interval Value Register
RTMR3_CUR_VALUE_REG	0x0048	R_Timer 3 Current Value Register
RTMR_VER_REG	0x0090	R_Timer Version Register

3.7.6. Register Description

3.7.6.1. 0x0000 R_Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: RTMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	RTMR3_IRQ_EN. R_Timer 3 Interrupt Enable. 0: disable 1: R_Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	RTMR2_IRQ_EN. R_Timer 2 Interrupt Enable. 0: disable 1: R_Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	RTMR1_IRQ_EN. R_Timer 1 Interrupt Enable. 0: disable 1: R_Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	RTMR0_IRQ_EN. R_Timer 0 Interrupt Enable. 0: disable 1: R_Timer 0 Interval Value reached interrupt enable.

3.7.6.2. 0x0004 R_Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: RTMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
3	R/W	0x0	RTMR3_IRQ_PEND. R_Timer3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, R_Timer 3 interval value is reached
2	R/W	0x0	RTMR2_IRQ_PEND. R_Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, R_Timer 2 interval value is reached
1	R/W	0x0	RTMR1_IRQ_PEND. R_Timer 1 IRQ Pending. Set 1 to the bit will clear it.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: No effect 1: Pending, R_Timer 1 interval value is reached
0	R/W	0x0	RTMR0_IRQ_PEND. R_Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, R_Timer 0 interval value is reached

3.7.6.3. 0x0x0010 R_Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: RTMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RTMR0_MODE. R_Timer 0 mode. 0: Continuous mode. When interval value reached, the R_Timer will not disable automatically. 1: Single mode. When interval value reached, the R_Timer will disable automatically.
6:4	R/W	0x0	RTMR0_CLK_PRES. Select the pre-scale of R_Timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	RTMR0_CLK_SRC. 00:LOSC 01: OSC 10: / 11: /
1	R/W	0x0	RTMR0_RELOAD. R_Timer 0 Reload. 0: No effect 1: Reload R_Timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	RTMR0_EN. R_Timer 0 Enable. 0: Stop/Pause 1: Start If the R_Timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the R_Timer enable bit is set to "0",

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In R_Timer pause state, the interval value register can be modified. If the R_Timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.4. 0x0014 R_Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: RTMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RTMR0_INTV_VALUE. R_Timer 0 Interval Value.

NOTE

When setting value, the system clock and the R_Timer clock source should be taken into consideration.

3.7.6.5. 0x0018 R_Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: RTMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RTMR0_CUR_VALUE. R_Timer 0 Current Value.

NOTE

R_Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.6. 0x0020 R_Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: RTMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RTMR1_MODE. R_Timer 1 mode. 0: Continuous mode. When interval value reached, the R_Timer will not disable automatically. 1: Single mode. When interval value reached, the R_Timer will disable automatically.
6:4	R/W	0x0	RTMR1_CLK_PRES. Select the pre-scale of R_Timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			101: /32 110: /64 111: /128
3:2	R/W	0x1	RTMR1_CLK_SRC. 00:LOSC 01: OSC 10: / 11: /
1	R/W	0x0	RTMR1_RELOAD. R_Timer 1 Reload. 0: No effect 1: Reload R_Timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	RTMR1_EN. R_Timer 1 Enable. 0: Stop/Pause 1: Start If the R_Timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the R_Timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In R_Timer pause state, the interval value register can be modified. If the R_Timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.7. 0x0024 R_Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: RTMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	RTMR1_INTV_VALUE. R_Timer 1 Interval Value.

NOTE

When setting value, the system clock and the R_Timer clock source should be taken into consideration.

3.7.6.8. 0x0028 R_Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: RTMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RTMR1_CUR_VALUE. R_Timer 1 Current Value.

NOTE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

R_Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.9. 0x0030 R_Timer 2 Control Register(Default Value: 0x0000_0004)

Offset: 0x0030			Register Name: RTMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RTMR2_MODE. R_Timer 2 mode. 0: Continuous mode. When interval value reached, the R_Timer will not disable automatically. 1: Single mode. When interval value reached, the R_Timer will disable automatically.
6:4	R/W	0x0	RTMR2_CLK_PRES. Select the pre-scale of R_Timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	RTMR2_CLK_SRC. 00:LOSC 01: OSC 10: / 11: /
1	R/W	0x0	RTMR2_RELOAD. R_Timer 2 Reload. 0: No effect 1: Reload R_Timer 2 Interval value After the bit is set, it can not be written again before it's cleared automatically.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x0	RTMR2_EN. R_Timer 2 Enable. 0: Stop/Pause 1: Start If the R_Timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the R_Timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In R_Timer pause state, the interval value register can be modified. If the R_Timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.10. 0x0034 R_Timer 2 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: RTMR2_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	RTMR2_INTV_VALUE. R_Timer 2 Interval Value.

NOTE

When setting value, the system clock and the R_Timer clock source should be taken into consideration.

3.7.6.11. 0x0038 R_Timer 2 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: RTMR2_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RTMR2_CUR_VALUE. R_Timer 2 Current Value.

NOTE

R_Timer 2 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.12. 0x0040 R_Timer 3 Control Register(Default Value: 0x0000_0004)

Offset: 0x0040			Register Name: RTMR3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RTMR3_MODE. R_Timer 3 mode. 0: Continuous mode. When interval value reached, the R_Timer will not disable automatically. 1: Single mode. When interval value reached, the R_Timer will disable automatically.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6:4	R/W	0x0	RTMR3_CLK_PRES. Select the pre-scale of R_Timer 3 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	RTMR3_CLK_SRC. 00:LOSC 01: OSC 10: / 11: /
1	R/W	0x0	RTMR3_RELOAD. R_Timer 3 Reload. 0: No effect 1: Reload R_Timer 3 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	RTMR3_EN. R_Timer 3 Enable. 0: Stop/Pause 1: Start If the R_Timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the R_Timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In R_Timer pause state, the interval value register can be modified. If the R_Timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.13. 0x0044 R_Timer 3 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: RTMR3_INTV_VALUE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	RTMR3_INTV_VALUE. R_Timer 3 Interval Value.

NOTE

When setting value, the system clock and the R_Timer clock source should be taken into consideration.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.6.14. 0x0048 R_Timer 3 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: RTMR3_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RTMR3_CUR_VALUE. R_Timer 3 Current Value.

NOTE

R_Timer 3 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.15. 0x0090 R_Timer Version Register(Default Value: 0x0001_0000)

Offset: 0x0090			Register Name: RTMR_VER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R	0x1	Large Version.
15:15	/	/	/
4:0	R	0x0	Small Version.

NOTE

The entire version is V1.0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.8. High Speed Timer

3.8.1. Overview

The high speed timer(HSTimer) module implements more precise timing and counting functions.

The HSTimer has the following features:

- Timing clock is AHB1 that can provides more precise timing clock
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.8.2. Block Diagram

Figure 3-13 shows a block diagram of the HSTimer.

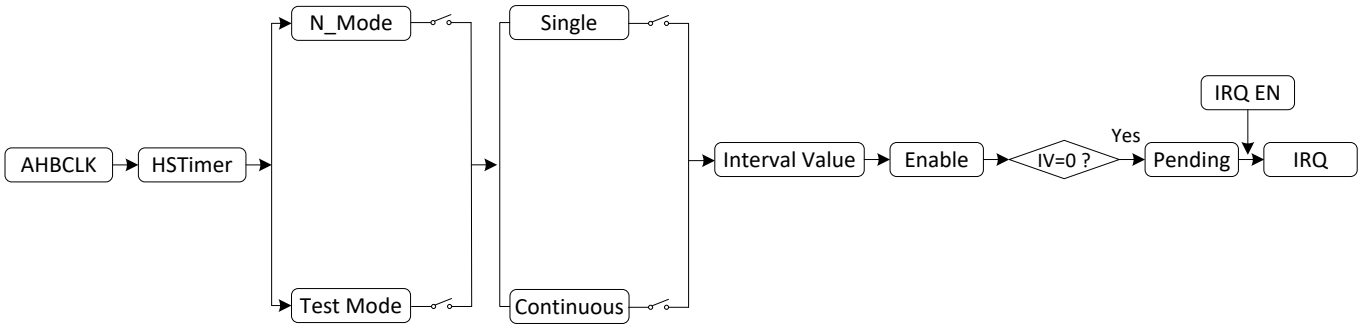


Figure 3- 13. HSTimer Block Diagram

3.8.3. Operations and Functional Descriptions

3.8.3.1. HSTimer Formula

$$\frac{(HS_TMR_INTV_HI_REG<<32 + HS_TMR_INTV_LO_REG) - (HS_TMR_CURNT_HI_REG<<32 + HS_TMR_CURNT_LO_REG)}{AHB1CLK} \times HS_TMR_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit

HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit

HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

HS_TMR_CURNT_LO_REG: Current Value of Counter Lower Bit
AHB1CLK: AHB1 Clock Frequency
HS_TMR_CLK: Time Prescale Ratio of Counter

3.8.3.2. Typical Application

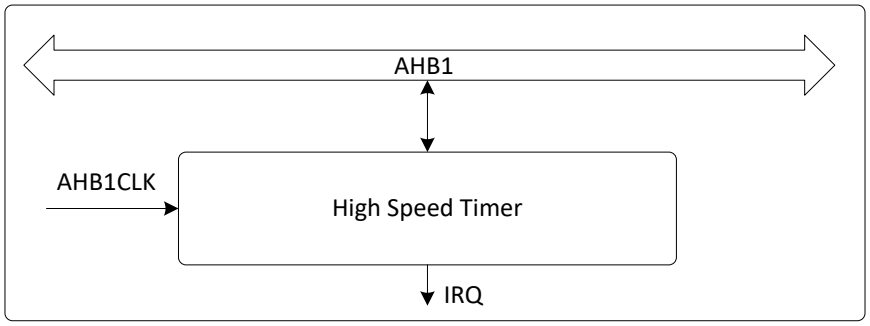


Figure 3- 14. HSTimer Application Diagram

The high speed timer is on AHB1, and the high speed timer controls registers by AHB1.
The high speed timer has single clock source: AHB1. The high speed timer can generate interrupt.

3.8.3.3. Function Implemention

The high speed timer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The high speed timer has two timing modes.

- **Continuous mode** : The bit7 of **HS_TMR0_CTRL_REG** is set to the continuous mode, when the count value is decreased to 0, the high speed timer module reloads data from **HS_TMR_INTV_LO_REG** and **HS_TMR_INTV_HI_REG,** then continues to count.
- **Single mode** : The bit7 of **HS_TMR0_CTRL_REG** is set to the single mode, when the count value is decreased to 0, the high speed timer stops counting. The high speed timer starts to count again only when a new initial value is loaded.

The high speed timer has two operating modes.

- **Normal mode**: When the bit31 of **HS_TMR0_CTRL_REG** is set to the normal mode, the high speed timer is used as 56-bit down counter, which can finish continuous timing and single timing.
- **Test mode**: When the bit31 of **HS_TMR0_CTRL_REG** is set to the test mode, then **HS_TMR_INTV_LO_REG** must be set to 0x1, the high speed timer is used as 24-bit down counter, and **HS_TMR_INTV_HI_REG** is the initial value of the high speed timer.

Each high speed timer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8,16.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.8.3.4. Operating Mode

3.8.3.4.1. HSTimer Initial

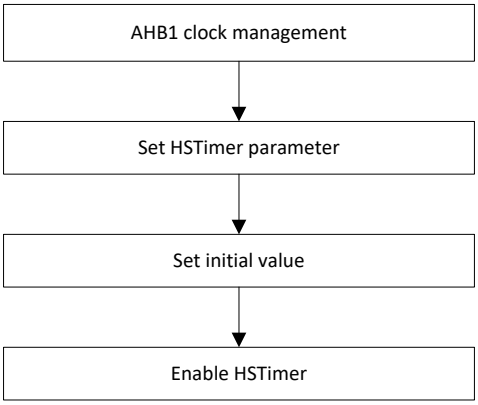


Figure 3- 15. HSTimer Initialization Process

(1) AHB1 clock management: Open the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the high speed timer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to **HS_TMR0_CTRL_REG** have no sequences.
(3) Write the initial value: Firstly write the low-bit register **(HS_TMR_INTV_LO_REG)**, then write the high-bit register **(HS_TMR_INTV_HI_REG)**. Write the bit1 of **HS_TMR0_CTRL_REG** to load the initial value. If in timing stop stage of high speed timer, write the bit1 and bit0 of **HS_TMR0_CTRL_REG** to reload the initial value.
(4) Enable high speed timer: Write the bit[0] of **HS_TMR0_CTRL_REG** to enable high speed timer to count.
(5) Reading **HS_TMR_CURNT_LO_REG** and **HS_TMR_CURNT_HI_REG** can get current counting value.

3.8.3.4.2. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of **HS_TMR_IRQ_EN_REG**, when the counting time of high speed timer reaches, the corresponding interrupt generates.
(2) After enter the interrupt process, write **HS_TMR_IRQ_STAS_REG** to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.8.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follows, AHB1CLK will be configured as 100MHz and n_mode,single mode and 2 pre-scale will be selected in this instance.

```
writel(0x32, HS_TMR0_INTV_LO);                  //Set interval value Lo 0x32
writel(0x0, HS_TMR0_INTV_HI);                   //Set interval value Hi 0x0
writel(0x90, HS_TMR0_CTRL);                     //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);  //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);  //Enable HSTimer0
```

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

```
while(!(readl(HS_TMR_IRQ_STAS)&1));          //Wait for HSTimer0 to generate pending
writel(1,HS_TMR_IRQ_STAS);                    //Clear HSTimer0 pending
```

3.8.5. Register List

Module Name	Base Address
High Speed Timer	0x03005000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.8.6. Register Description

3.8.6.1. 0x0000 HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	HS_TMR1_INT_EN High Speed Timer 1 Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	HS_TMR0_INT_EN High Speed Timer 0 Interrupt Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.8.6.2. 0x0004 HS Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND High Speed Timer 1 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 1 interval value is reached.
0	R/W1C	0x0	HS_TMR0_IRQ_PEND High Speed Timer 0 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached.

3.8.6.3. 0x0020 HS Timer 0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST High Speed Timer 0 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE High Speed Timer 0 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W1S	0x0	HS_TMR0_RELOAD High Speed Timer 0 Reload 0: No effect 1: Reload High Speed Timer 0 Interval Value
0	R/W	0x0	HS_TMR0_EN High Speed Timer 0 Enable 0: Stop/Pause 1: Start If the timer starts, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer starts again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.4. 0x0024 HS Timer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO High Speed Timer 0 Interval Value [31:0]

3.8.6.5. 0x0028 HS Timer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI High Speed Timer 0 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.8.6.6. 0x002C HS Timer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			High Speed Timer 0 Current Value [31:0]

3.8.6.7. 0x0030 HS Timer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI High Speed Timer 0 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.8.6.8. 0x0040 HS Timer 1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST High Speed Timer 1 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE High Speed Timer 1 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W1S	0x0	HS_TMR1_RELOAD High Speed Timer 1 Reload 0: No effect 1: Reload High Speed Timer 1 Interval Value
0	R/W	0x0	HS_TMR1_EN High Speed Timer 1 Enable 0: Stop/Pause 1: Start If the timer starts, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer starts again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.9. 0x0044 HS Timer 1 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO High Speed Timer 1 Interval Value [31:0]

3.8.6.10. 0x0048 HS Timer 1 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI High Speed Timer 1 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.8.6.11. 0x004C HS Timer 1 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			High Speed Timer 1 Current Value [31:0]

3.8.6.12. 0x0050 HS Timer 1 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI High Speed Timer 1 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.9. GIC

3.9.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x00	SGI 0 interrupt
1	SGI 1	0x04	SGI 1 interrupt
2	SGI 2	0x08	SGI 2 interrupt
3	SGI 3	0x0C	SGI 3 interrupt
4	SGI 4	0x10	SGI 4 interrupt
5	SGI 5	0x14	SGI 5 interrupt
6	SGI 6	0x18	SGI 6 interrupt
7	SGI 7	0x1C	SGI 7 interrupt
8	SGI 8	0x20	SGI 8 interrupt
9	SGI 9	0x24	SGI 9 interrupt
10	SGI 10	0x28	SGI 10 interrupt
11	SGI 11	0x2C	SGI 11 interrupt
12	SGI 12	0x30	SGI 12 interrupt
13	SGI 13	0x34	SGI 13 interrupt
14	SGI 14	0x38	SGI 14 interrupt
15	SGI 15	0x3C	SGI 15 interrupt
16	PPI 0	0x40	PPI 0 interrupt
17	PPI 1	0x44	PPI 1 interrupt
18	PPI 2	0x48	PPI 2 interrupt
19	PPI 3	0x4C	PPI 3 interrupt
20	PPI 4	0x50	PPI 4 interrupt
21	PPI 5	0x54	PPI 5 interrupt
22	PPI 6	0x58	PPI 6 interrupt
23	PPI 7	0x5C	PPI 7 interrupt
24	PPI 8	0x60	PPI 8 interrupt
25	PPI 9	0x64	PPI 9 interrupt
26	PPI 10	0x68	PPI 10 interrupt
27	PPI 11	0x6C	PPI 11 interrupt
28	PPI 12	0x70	PPI 12 interrupt
29	PPI 13	0x74	PPI 13 interrupt
30	PPI 14	0x78	PPI 14 interrupt
31	PPI 15	0x7C	PPI 15 interrupt
Normal Interfaces			
32	UART0	0x80	UART0 interrupt
33	UART1	0x84	UART1 interrupt
34	UART2	0x88	UART2 interrupt

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
35	UART3	0x8C	UART3 interrupt
36	UART4	0x90	UART4 interrupt
37	/	0x94	/
38	/	0x98	/
39	TWI0	0x9C	TWI0 interrupt
40	TWI1	0xA0	TWI1 interrupt
41	TWI2	0xA4	TWI2 interrupt
42	TWI3	0xA8	TWI3 interrupt
43	/	0xAC	/
44	/	0xB0	/
45	SPI0	0xB4	SPI0 interrupt
46	SPI1	0xB8	SPI1 interrupt
47	SPI2	0xBC	SPI2 interrupt
48	EMAC0	0xC0	EMAC0 interrupt
49	/	0xC4	/
50	PWM	0xC8	PWM interrupt
51	IR_TX	0xCC	CIR transimiter interrupt
52	GPADC	0xD0	GPADC interrupt
53	THS	0xD4	Thermal sensor interrupt
54	LRADC	0xD8	LRADC interrupt
55	OWA	0xDC	OWA interrupt
56	DMIC	0xE0	DMIC interrupt
57	Audio Codec	0xE4	Audio codec interrupt
58	I2S0	0xE8	I2S0 interrupt
59	I2S1	0xEC	I2S1 interrupt
60	I2S2	0xF0	I2S2 interrupt
61	I2S3	0xF4	I2S3 interrupt
62	USB0_EHCI	0xF8	USB0 EHCI interrupt
63	USB0_OHCI	0xFC	USB0 OHCI interrupt
64	USB0_OTG	0x100	USB0 OTG interrupt
65	USB1_EHCI	0x104	USB1 EHCI interrupt
66	USB1_OHCI	0x108	USB1 OHCI interrupt
67	LEDC	0x10C	LEDC interrupt
68	CIR_RX	0x110	CIR receiver interrupt
69	/	0x114	/
Memory			
70	NAND0	0x118	NAND0 interrupt
71	SMHC0	0x11C	SMHC0 interrupt
72	SMHC1	0x120	SMHC1 interrupt
73	SMHC2	0x124	SMHC2 interrupt
74	/	0x128	/
75	/	0x12C	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
System			
76	CLK_DET	0x130	Clock detect interrupt
77	DMA_NS	0x134	DMA interrupt in non-secure domain
78	MSGBOX	0x138	Message box interrupt
79	SPINLOCK	0x13C	Spinlock interrupt
80	HSTIMER0	0x140	High speed timer0 interrupt
81	HSTIMER1	0x144	High speed timer1 interrupt
82	SMC	0x148	Secure memory control interrupt
83	TIMER0	0x14C	Timer0 interrupt
84	TIMER1	0x150	Timer1 interrupt
85	WDOG	0x154	Watchdog interrupt
86	GPIOB	0x158	GPIOB interrupt
87	GPIOC	0x15C	GPIOC interrupt
88	GPIOD	0x160	GPIOD interrupt
89	GPIOE	0x164	GPIOE interrupt
90	GPIOF	0x168	GPIOF interrupt
91	GPIOG	0x16C	GPIOG interrupt
92	GPIOH	0x170	GPIOH interrupt
93	/	0x174	/
94	/	0x178	/
95	NSI	0x17C	NSI interrupt
96	PSI	0x180	PSI interrupt
97	BUS_TIMEOUT	0x184	Bus timeout interrupt
98	IOMMU	0x188	IOMMU interrupt
99	DMA_S	0x18C	DMA interrupt in secure domain
Display&Image Interfaces			
100	DSI0	0x190	DSI0 interrupt
101	TCON_LCD0	0x194	TCON_LCD0 interrupt
102	/	0x198	/
103	CSI_DMA0	0x19C	CSI_DMA0 interrupt
104	CSI_DMA1	0x1A0	CSI_DMA1 interrupt
105	CSI_DMA2	0x1A4	CSI_DMA2 interrupt
106	CSI_DMA3	0x1A8	CSI_DMA3 interrupt
107	CSI_PARSER0	0x1AC	CSI_PARSER0 interrupt
108	CSI_PARSER1	0x1B0	CSI_PARSER1 interrupt
109	CSI_ISP0	0x1B4	CSI_ISP0 interrupt
110	CSI_ISP1	0x1B8	CSI_ISP1 interrupt
111	CSI_TDM	0x1BC	CSI_TDM interrupt
112	CSI_CMB	0x1C0	CSI_CMB interrupt
113	CSI_TOP	0x1C4	CSI_TOP interrupt
114	/	0x1C8	/
115	/	0x1CC	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
116	/	0x1D0	/
117	/	0x1D4	/
118	/	0x1D8	/
119	/	0x1DC	/
Accelerator			
120	DE	0x1E0	DE interrupt
121	/	0x1E4	/
122	/	0x1E8	/
123	G2D	0x1EC	G2D interrupt
124	CE_NS	0x1F0	CE interrupt in non-secure domain
125	CE	0x1F4	CE interrupt in secure domain
126	VE	0x1F8	VE interrupt
127	/	0x1FC	/
128	/	0x200	/
129	GPU	0x204	GPU interrupt
130	/	0x208	/
131	/	0x20C	/
132	/	0x210	/
133	/	0x214	/
134	/	0x218	/
CPUS domain			
135	NMI	0x21C	NMI interrupt
136	R_TIMER0	0x220	Timer0 interrupt in CPUS
137	R_TIMER1	0x224	Timer1 interrupt in CPUS
138	R_TIMER2	0x228	Timer2 interrupt in CPUS
139	R_TIMER3	0x22C	Timer3 interrupt in CPUS
140	R_Alarm	0x230	Alarm interrupt in CPUS
141	R_WDOG	0x234	Watchdog interrupt in CPUS
142	R_TWD	0x238	Trust watchdog interrupt in CPUS
143	R_GPIOL	0x23C	GPIOL interrupt in CPUS
144	R_UART	0x240	UART interrupt in CPUS
145	R_TWI0	0x244	TWI0 interrupt in CPUS
146	R_TWI1	0x248	TWI1 interrupt in CPUS
147	R_IR	0x24C	IR interrupt in CPUS
148	R_PWM	0x250	PWM interrupt in CPUS
149	/	0x254	/
150	/	0x258	/
151	R_PPU	0x25C	PPU interrupt in CPUS
CPUX related			
160	C0_CTI0	0x280	C0_CTI0 interrupt
161	C0_CTI1	0x284	C0_CTI1 interrupt
162	C0_CTI2	0x288	C0_CTI2 interrupt

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Interrupt Number	Interrupt Source	Interrupt Vector	Description
163	C0_CTI3	0x28C	C0_CTI3 interrupt
164	C0_COMMTX0	0x290	C0_COMMTX0 interrupt
165	C0_COMMTX1	0x294	C0_COMMTX1 interrupt
166	C0_COMMTX2	0x298	C0_COMMTX2 interrupt
167	C0_COMMTX3	0x29C	C0_COMMTX3 interrupt
168	C0_COMMRX0	0x2A0	C0_COMMRX0 interrupt
169	C0_COMMRX1	0x2A4	C0_COMMRX1 interrupt
170	C0_COMMRX2	0x2A8	C0_COMMRX2 interrupt
171	C0_COMMRX3	0x2AC	C0_COMMRX3 interrupt
172	C0_PMU0	0x2B0	C0_PMU0 interrupt
173	C0_PMU1	0x2B4	C0_PMU1 interrupt
174	C0_PMU2	0x2B8	C0_PMU2 interrupt
175	C0_PMU3	0x2BC	C0_PMU3 interrupt
176	C0_AXI_ERROR	0x2C0	C0_AXI_ERROR interrupt
177	AXI_WR_IRQ	0x2C4	
178	AXI_RD_IRQ	0x2C8	
179	DBGRSTREQ0	0x2CC	
180	DBGRSTREQ1	0x2D0	
181	DBGRSTREQ2	0x2D4	
182	DBGRSTREQ3	0x2D8	
183	nVCPUMNTIRQ0	0x2DC	
184	nVCPUMNTIRQ1	0x2E0	
185	nVCPUMNTIRQ2	0x2E4	
186	nVCPUMNTIRQ3	0x2E8	
187	nCOMMIRQ0	0x2EC	
188	nCOMMIRQ1	0x2F0	
189	nCOMMIRQ2	0x2F4	
190	nCOMMIRQ3	0x2F8	
191	DBGPWRUPREQ_out	0x2FC	

For complete GIC information, refer to the ***GIC PL400 technical reference manual*** and ***ARM GIC Architecture Specification V2.0***.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10. DMA

3.10.1. Overview

The direction memory access (DMA) is used to transfer data between a peripheral and a memory, between peripherals, or between memories. DMA is a high-speed data transfer operation that reduces the CPU resources.

The DMA has the following features:

- 8 channels DMA
- Provides 32 peripheral DMA requests for data read and 32 peripheral DMA requests for data write
- Transfer with linked list
- Programmable 8-,16-,32-,64-bit data width
- Programmable DMA burst length
- DRQ response includes wait mode and handshake mode
- Memory devices support non-aligned transform
- DMA channel supports pause function

3.10.2. Block Diagram

The following figure shows a block diagram of DMA.

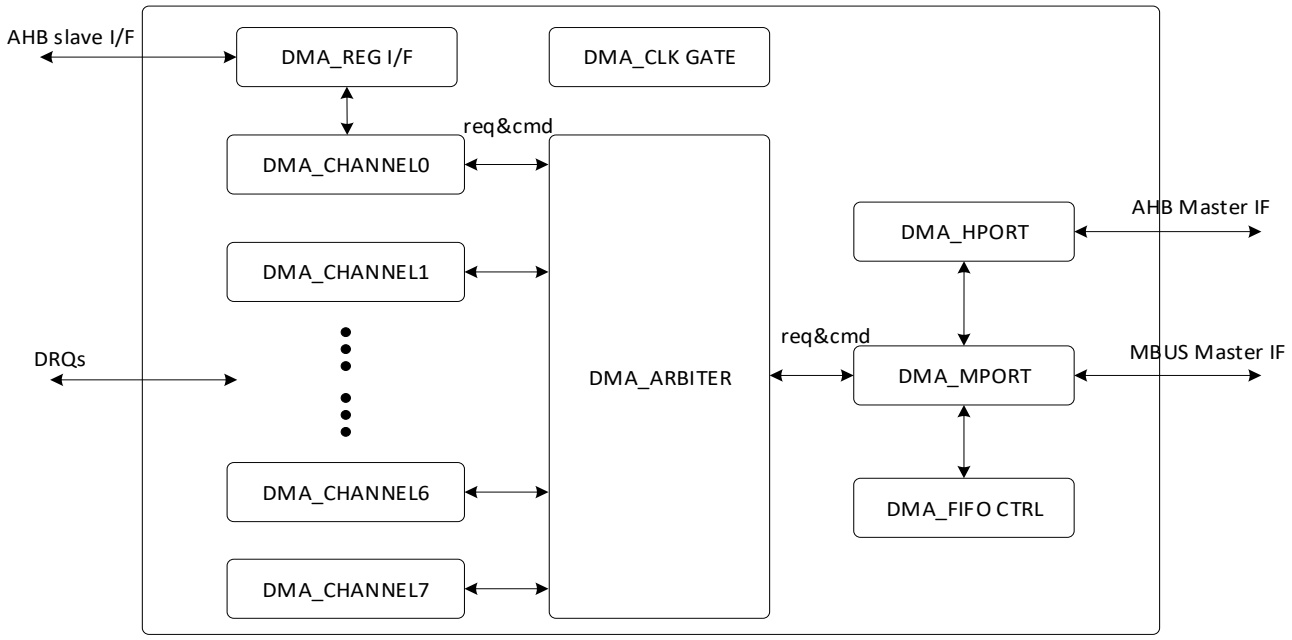


Figure 3- 16. DMA Block Diagram

- **DMA_ARBITER**: Arbitrate DMA read/write requirement of each channel, and convert to read/write requirement of each port.
- **DMA_CHANNEL**: DMA transform engine. Each channel is independent. The priorities of DMA channels uses

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

polling mechanism. When the DMA requests from two peripherals are valid simultaneously, if DMA_ARBITER is non-idle, the next channel of the current channel has the higher priority; if DMA_ARBITER is idle, the smaller the number of the channel is, the higher the priority is, such as the channel0 has the highest priority, whereas the channel 7 has the lowest priority.

- **DMA_MPORT**: Receive read/write requirement of DMA_ARBITER, and convert to the corresponding MBUS access. It is mainly used to access DRAM.
- **DMA_HPORT**: AHB master access interface, it is mainly used to access SRAM and IO device.
- **DMA_FIFOCTL**: Internal FIFO cell control module.
- **DMA_REGIF**: Common register module, mainly used to resolve AHB1 demand.
- **DMA_CLKGATE**: Hardware auto clock gating control module.

DMA integrates 8 independent DMA channels. When DMA channel starts, DMA gets DMA descriptor by DMA_DESC_ADDR_REG to use for the configuration information of the current DMA package transfer, and DMA can transfer data between the specified peripherals through the configuration information. When a package transfer finished, DMA judges whether the current channel transfer finished or continues to obtain/transfer the descriptor of the next package through the linked information in descriptor. When the chained address information of the descriptor indicates the current channel transfer is completed, DMA will close chain-transfer and the channel.

3.10.3. Operations and Functional Descriptions

3.10.3.1. Clock and Reset

DMA is on AHB1. The clock of AHB1 influences the transfer efficiency of DMA.

3.10.3.2. Typical Application

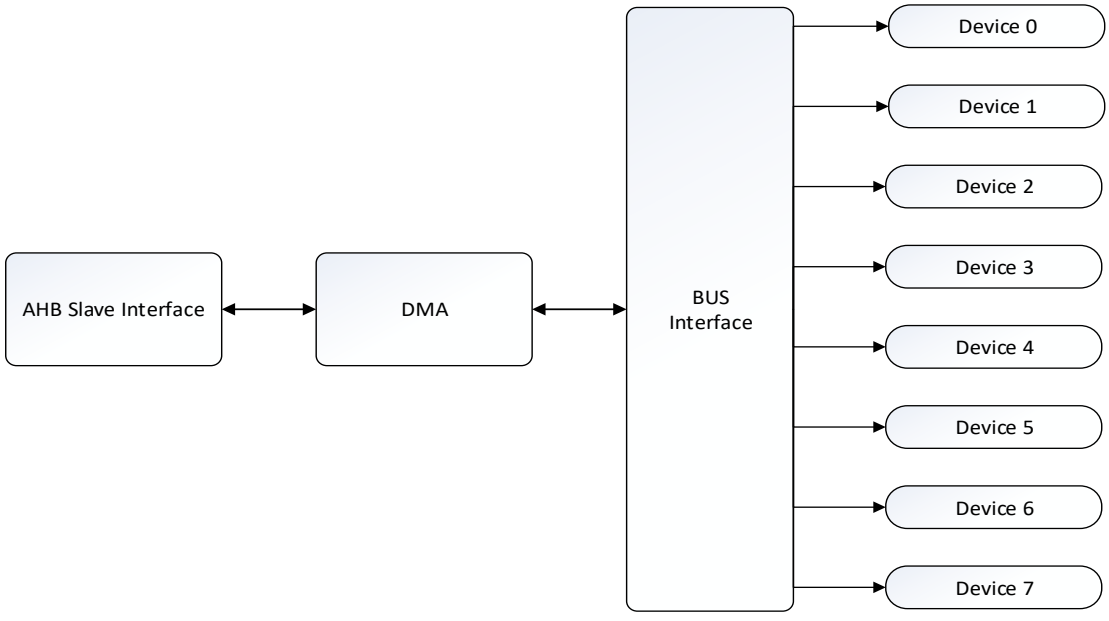


Figure 3- 17. DMA Typical Application Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.3.3. DRQ Type

Table 3- 8. DMA DRQ Table

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	OWA
port3	I2S0_RX	port3	I2S0_TX
port4	I2S1_RX	port4	I2S1_TX
port5	I2S2_RX	port5	I2S2_TX
port6	I2S3_RX	port6	I2S3_TX
port7	Audio Codec	port7	Audio Codec
port8	DMIC	port8	
port9		port9	
port10	NAND0	port10	NAND0
port11		port11	
port12	GPADC	port12	
port13		port13	
port14	UART0_RX	port14	UART0_TX
port15	UART1_RX	port15	UART1_TX
port16	UART2_RX	port16	UART2_TX
port17	UART3_RX	port17	UART3_TX
port18	UART4_RX	port18	UART4_TX
port19		port19	
port20		port20	
port21		port21	
port22	SPI0_RX	port22	SPI0_TX
port23	SPI1_RX	port23	SPI1_TX
port24	SPI2_RX	port24	SPI2_TX
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	OTG_EP1	Port30	OTG_EP1
Port31	OTG_EP2	Port31	OTG_EP2
Port32	OTG_EP3	Port32	OTG_EP3
Port33	OTG_EP4	Port33	OTG_EP4
Port34	OTG_EP5	Port34	OTG_EP5
Port35		Port35	
Port36		Port36	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40	R_UART-RX	Port40	R_UART-TX
Port41		Port41	
Port42		Port42	LEDC
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1
Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47		Port47	
Port48		Port48	
Port49		Port49	
Port50	R_TWI0	Port50	R_TWI0
Port51	R_TWI1	Port51	R_TWI1

3.10.3.4. DMA Descriptor

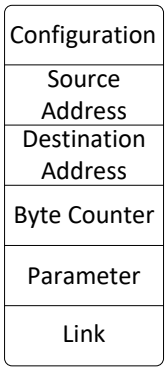


Figure 3- 18. DMA Descriptor

DMA descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words, in turn, configuration, source address, destination address, byte counter, parameter, link.

(1) Configuration : Configure the following information by DMA_CFG_REG.

- **DRQ type of source and destination:** The DRQ signal of devices is as driving signal of DMA transfer.
- **Transferred address count mode**: IO mode indicates the address is fixed during transfer; linear mode indicates the address is increasing during transfer.
- **Transferred block length**: Block length is the amount of DMA transferred data in one-shot valid DRQ. The block length supports 1-bit,4-bit,8-bit or 16-bit mode.
- **Transferred data width**: Data width indicates the data width of every operation, and supports 8-bit,16-bit,32-bit or 64-bit mode.

(2) Source Address: Configure the transferred source address.

(3) Destination Address: Configure the transferred destination address.

DMA reads data from the source address, then writes data to the destination address.

In descriptor, the **Source/Destination Address** stores the lower 32-bit of the 34-bit byte address, and the higher

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2-bit is stored in **Parameter**. The specific position is as follows.

Table 3- 9. Source/Destination Address Distribution

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32-bit of 34-bit byte source address
Destination Address	31:0	DMA transfers the lower 32-bit of 34-bit byte destination address
Paramter	31:20	Reserved
	19:18	DMA transfers the high 2-bit of 34-bit byte destination address
	17:16	DMA transfers the high 2-bit of 34-bit byte source address
	15:8	Reserved
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The address of the next group descriptor, the lower 30-bit of word address
	1:0	The address of the next group descriptor, the higher 2-bit of word address

From the above table, real DMA source address(byte mode) = { Paramter [17:16], Source Address [31:0]};
Real DMA desnitation address(byte mode) = { Paramter [19:18], Destination Address [31:0]};
And real link address (byte mode) = {Link[1:0], Link[31:2], 2'b00}.

(4) Byte counter: Configure the amount of a package. The maximum package is not more than (2^25-1) bytes. If the amount of the package reaches the maximum value, even if DRQ is valid, DMA should stop the current transfer.

(5) Parameter: Configure the interval between data block. The parameter is valid for non-memory peripherals. When DMA detects that DRQ is high level, DMA transfers block cycle. And during time, the changing of DRQ is ignored. After transferred, DMA waits the setting cycle(WAIT_CYC), then executes the next DRQ detection.

(6) Link: If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. DMA will stop transfer after the package is transferred; if the value of the link is not 0xFFFFF800, the value of the link is considered the descriptor address of the next package.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

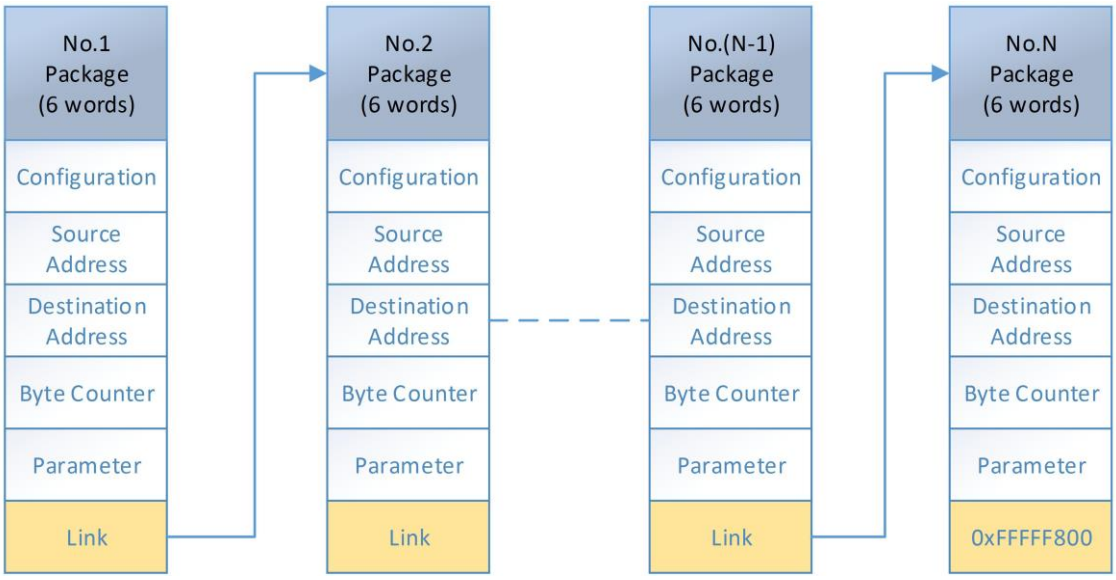


Figure 3- 19. DMA Chain Transfer

3.10.3.5. Interrupt

The half package interrupt is enabled, DMA sends half package interrupt after the half package transfer completes. The total package interrupt is enabled, DMA sends package end interrupt after the total package transfer completes. The total queue interrupt is enabled, DMA sends queue end interrupt after the total queue completes.
Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts generate very closely, the later interrupt may override the former one. So for CPU, the DMA has only a system interrupt source.

3.10.3.6. Security

DMA supports system Trustzone, and supports the secure mode configuration of DMA channel. Each DMA channel is non-secure by default. When system Trustzone is enabled, DMA is secure, only the secure devices can access DMA, any non-secure access is invalid.

When DMA channel is configured to non-secure, then the channel can only access the non-secure memory area. DMA cannot write data to secure memory area, the read-back data from secure memory area is 0.

3.10.3.7. Clock Gating

DMA_CLK_GATE module is the auto clock gating control module by hardware. DMA_CLK_GATE module is mainly used to generate the clock of DMA sub-module and the local circuit in module, including clock gating of channel and clock gating of public part.

The clock gating of the channel indicates DMA clock can auto-enable when the system accesses the current DMA channel register and DMA channel is enabled. When DMA transfer is completed, DMA channel clock can auto-disable after 16 HCLK delay, meanwhile the clock of DMA channel, the corresponding channel control and FIFO control will be

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

closed.

The clock gating of the common part indicates the clock of the common circuit can auto-disable when all DMA channels are opened. The common circuit includes the common circuit of FIFO control module, MPORT module and memory bus clock.

DMA clock gating can support all the functions stated above or not by software.

3.10.3.8. Transfer Mode

DMA supports two data transfer modes: wait mode and handshake mode.

(1) Wait Mode

When device request signal enters DMA, the device request signal is transformed into the internal DRQ signal through block and wait counter. The transformed principle is as follows.

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically.
- After the internal DRQ holds low automatically at the DMA cycle of wait counter times, DMA restarts to detect the external request, if the external request signal is valid, then the next transfer starts.

(2) Handshake Mode

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically; meanwhile within the last DMA operation before reaching block amount, DMA follows the operating demand to send DMA last signal simultaneously.
- The DMA last signal that is used as a part of DMA demand transmits at BUS, when the device receives the operating demand of DMA last at BUS, the device can judge DMA transfer block length finished, that is before transmit the request again, DMA operation cannot appear, and a DMA active signal is generated to the DMA controller. Notice that each DRQ signal of device corresponds to an active signal, if the device has many DRQ signals, then DMA returns different active signal through different bus operation.
- When DMA receives the transmitted active signal of devices, DMA ACK signal is returned to devices.
- After the device receives DMA ACK signal, if all operations of devices are completed, FIFO status and DRQ status are refreshed, then active signal is set as invalid.
- When DMA detects the falling edge of active signal, then the corresponding ACK signal is set as invalid, and DMA restarts to detect the external request signal. If the request signal is valid, then the next transfer starts.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

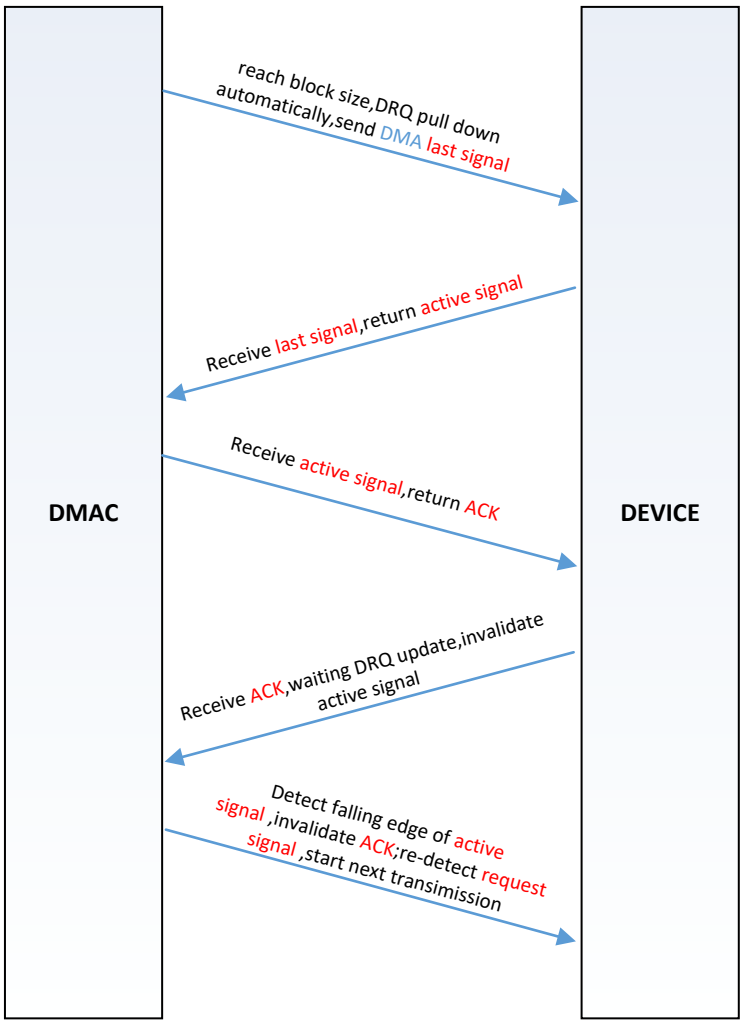


Figure 3- 20. DMA Transfer Mode

3.10.3.9. Auto-alignment Function

The DMA supports address auto alignment of non-IO devices, that is when the start address of non-IO devices is non 32-byte aligned, DMA firstly aligns the burst transfer within 32-byte to 32-byte. If the device of a DMA channel is configured to non-IO type, and the start address is 0x86, then DMA firstly aligns 26-byte burst transfer to 0xA0, then DMA transfers by 64-byte burst(maximum transfer amount of MBUS allowed). The address 32-byte alignment helps to improve the DRAM access efficiency.

IO devices do not support address alignment, so the bit width of IO devices must match the address offset, or not DMA ignores the non-consistency and indirectly transmits data of the corresponding bit width to the address.

The DMA descriptor address does not support auto-aligned function. The address must ensure word-aligned, or not DMA cannot identify descriptor.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.3.10. Operating Mode

3.10.3.10.1. DMA Clock Control

- The DMA clock is synchronous with AHB1 clock. Make sure that open the DMA gating bit of AHB1 clock before access DMA register.
- The reset input signal of DMA is asynchronous with AHB1, and is low valid by default. Make sure that de-assert the reset signal of DMA before access DMA register.
- To avoid indefinite state within registers , firstly de-assert the reset signal, secondly open the gating bit of AHB1.
- DMA has the function of clock auto gating, DMA clock can be disabled in DMA idle state using software to reduce power consumption. DMA enables clock auto gating by default.

3.10.3.10.2. DMA Transfer Process

The DMA transfer process is as follows.

(1) Request DMA channel, and judge the idle state of the channel by whether DMA channel is enabled.
(2) Write the descriptor(6 words) into memory, the descriptor must be word-aligned. Refer to ***3.9.3.4 DMA descriptor*** in detail.
(3) Write the start address of storing descriptor to **DMA_DESC_ADDR_REG**.
(4) Enable DMA channel, and write the corresponding channel to **DMA_EN_REG**.
(5) DMA obtains the descriptor information.
(6) Start to transmit a package, when half package is completed, DMA sends **Half Package Transfer Interrupt**; when total package is completed, DMA sends **Package End Transfer Interrupt**. These interrupt status can be read by **DMA_IRQ_PEND_REG**.
(7) Set **DMA_PAU_REG** to pause or resume the data transfer.
(8) After completed the total package transfer, DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; if the link is other value, the next package starts to transmit. When the transfer ends, DMA sends **Queue End Transfer Interrupt**.
(9) Disable the DMA channel.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

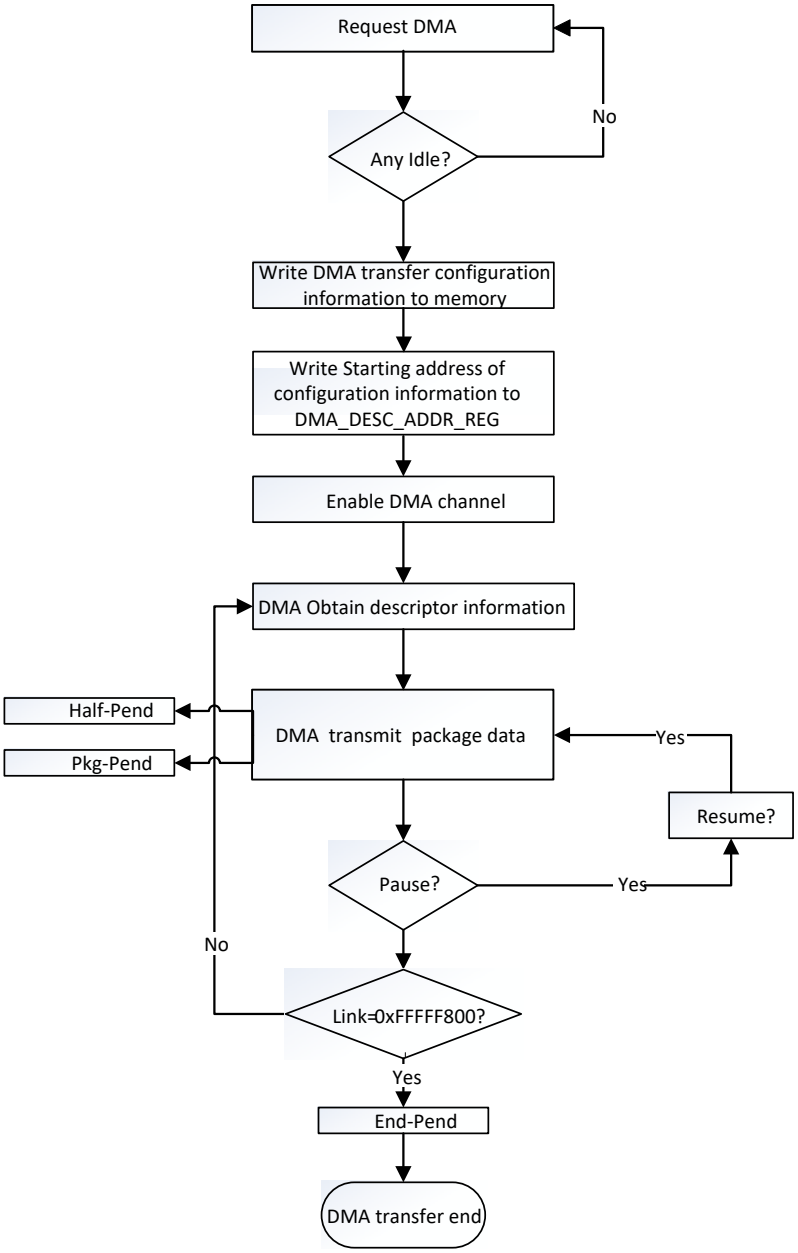


Figure 3- 21. DMA Transfer Process

3.10.3.10.3. DMA Interrupt

(1) Enable interrupt: write the corresponding interrupt enable of **DMA_IRQ_EN_REG**, when the corresponding interrupt condition is satisfied, the corresponding interrupt generates.

(2) After enter the interrupt process, write **DMA_IRQ_PEND_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.4. Programming Guidelines

(1) The transfer width of IO type device is consistent with the offset of start address.

(2) MBUS protocol does not support read operation of non-integer word, so for non-integer word read operation, device must ignore redundant inconsistent data between data width and configuration, that is, the device of non-integer word must interpret DMA demand through its FIFO width instead of read demand width.

(3) When the DMA transfer is paused, this is equivalent to invalid DRQ. Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32-byte data.

DMA application example :

```
writel(0x00000000, mem_address + 0x00);   //Setting configuration, mem_address must be word-aligned
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);   //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);   // Setting data package size
writel(0x00000000, mem_address + 0x10);   //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);    //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);      // Enable DMA channel0 transfer
```

DMA supports increasing data package in transfer, there are a few points to note here.

- When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.
- If data packages are needed to increase, then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package, if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package, then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.
- To ensure that the data changed valid, we can read again the value of **DMA Channel Descriptor Address Register** after changed the data. If there is not 0xFFFFF800, then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package needs some time, during this time, DMA channel may get back the descriptor of the last package. At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then the increasing data package is succeed, and fail otherwise.
- To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.5. Register List

Module Name	Base Address
DMA	0x03002000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register 0
DMA_SEC_REG	0x0020	DMA Security Register
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~7)
DMA_PAU_REG	0x0100+N*0x0040+0x0004	DMA Channel Pause Register(N=0~7)
DMA_DESC_ADDR_REG	0x0100+N*0x0040+0x0008	DMA Channel Start Address Register(N=0~7)
DMA_CFG_REG	0x0100+N*0x0040+0x000C	DMA Channel Configuration Register(N=0~7)
DMA_CUR_SRC_REG	0x0100+N*0x0040+0x0010	DMA Channel Current Source Register(N=0~7)
DMA_CUR_DEST_REG	0x0100+N*0x0040+0x0014	DMA Channel Current Destination Register(N=0~7)
DMA_BCNT_LEFT_REG	0x0100+N*0x0040+0x0018	DMA Channel Byte Counter Left Register(N=0~7)
DMA_PARA_REG	0x0100+N*0x0040+0x001C	DMA Channel Parameter Register(N=0~7)
DMA_MODE_REG	0x0100+N*0x0040+0x0028	DMA Mode Register(N=0~7)
DMA_FDESC_ADDR_REG	0x0100+N*0x0040+0x002C	DMA Former Descriptor Address Register(N=0~7)
DMA_PKG_NUM_REG	0x0100+N*0x0040+0x0030	DMA Package Number Register(N=0~7)

3.10.6. Register Description

3.10.6.1. 0x0000 DMA IRQ Enable Register 0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			DMA 3 Package End Transfer Interrupt Enable 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable

3.10.6.2. 0x0010 DMA IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.6.3. 0x0020 DMA Security Register (Default Value: 0x0000_00FF)

Offset:0x0020			Register Name: DMA_SEC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x1	DMA7_SEC DMA channel 7 security 0: Secure 1: Non-secure
6	R/W	0x1	DMA6_SEC DMA channel 6 security 0: Secure 1: Non-secure
5	R/W	0x1	DMA5_SEC DMA channel 5 security 0: Secure 1: Non-secure
4	R/W	0x1	DMA4_SEC DMA channel 4 security 0: Secure 1: Non-secure
3	R/W	0x1	DMA3_SEC DMA channel 3 security 0: Secure 1: Non-secure
2	R/W	0x1	DMA2_SEC DMA channel 2 security 0: Secure 1: Non-secure
1	R/W	0x1	DMA1_SEC DMA channel 1 security 0: Secure 1: Non-secure
0	R/W	0x1	DMA0_SEC DMA channel 0 security 0: Secure 1: Non-secure

3.10.6.4. 0x0028 DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT DMA MCLK interface circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT DMA common circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT DMA channel circuit auto gating bit 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, the bit-2 should be set up.

3.10.6.5. 0x0030 DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
30:8	/	/	/
7	R	0x0	DMA7_STATUS DMA Channel 7 Status 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status 0: Idle

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status 0: Idle 1: Busy

3.10.6.6. 0x0100+N*0x0040 DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040 (N=0~7)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN DMA Channel Enable 0: Disable 1: Enable

3.10.6.7. 0x0104+N*0x0040 DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0004(N=0~7)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE Pausing DMA Channel Transfer Data 0: Resume Transferring 1: Pause Transferring

3.10.6.8. 0x0108+N*0x0040 DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0008(N=0~7)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	DMA_DESC_LOW_ ADDR DMA Channel Descriptor Word Address, Low 30 bits. The Descriptor Address must be word-aligned.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1:0	R/W	0x0	DMA_DESC_HIGH_ ADDR DMA Channel Descriptor High Address, High 2 bits The real address is as below: DMA Channel Descriptor Address = {bit[1:0],bit[31:2],2'b00};

3.10.6.9. 0x010C+N*0x0040 DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x000C(N=0~7)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	BMODE_SEL 0: Normal mode 1: BMODE
30:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH DMA Destination Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	R	0x0	DMA_ADDR_MODE DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE DMA Destination Block Size 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH DMA Source Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE DMA Source Address Mode 0: Linear Mode 1: IO Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:6	R	0x0	DMA_SRC_BLOCK_SIZE DMA Source Block Size 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.10.6.10. 0x0110+N*0x0040 DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0010(N=0~7)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC DMA Channel Current Source Address, read only.

3.10.6.11. 0x0114+N*0x0040 DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0014(N=0~7)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST DMA Channel Current Destination Address, read only.

3.10.6.12. 0x0118+N*0x0040 DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0018(N=0~7)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT DMA Channel Byte Counter Left, read only.

3.10.6.13. 0x011C+N*0x0040 DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x001C(N=0~7)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC Wait Clock Cycles

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.10.6.14. 0x0128+N*0x0040 DMA Mode Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0028(N=0~7)			Register Name: DMA_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE 0: Wait mode 1: Handshake mode
2	R/W	0x0	DMA_SRC_MODE 0: Wait mode 1: Handshake mode
1:0	/	/	/

3.10.6.15. 0x012C+N*0x0040 DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x002C(N=0~7)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR This register is used to store the former value of DMA Channel Descriptor Address Register.

3.10.6.16. 0x0130+N*0x0040 DMA Package Number Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0030(N=0~7)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM This register will record the number of packages which has been completed in one transmission.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.11. Thermal Sensor Controller

3.11.1. Overview

Thermal sensors have became common elements in wide range of modern system on chip (SoC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller (THS) embeds three thermal sensors, sensor0 is located in CPU, sensor1 is located in GPU, and sensor2 is located in DDR. The thermal sensor can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

The THS has the following features:

- Temperature Accuracy : ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Power supply voltage: 1.8 V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.11.2. Block Diagram

Figure 3-22 shows a block diagram of the Thermal Sensor Controller.

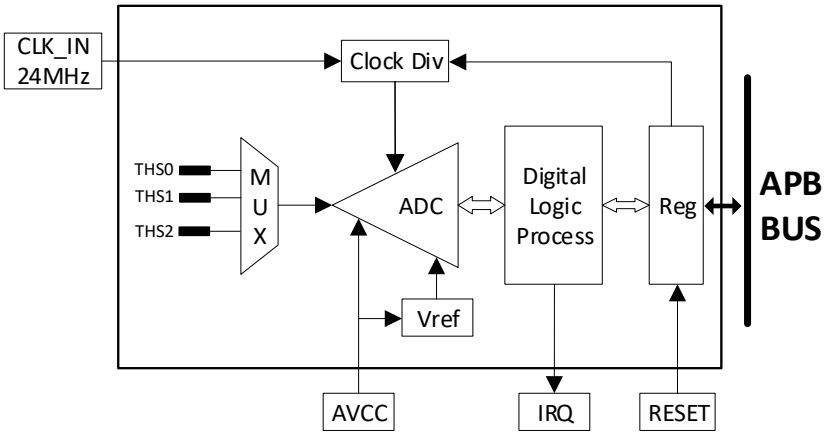


Figure 3- 22. Thermal Sensor Controller Block Diagram

3.11.3. Operations and Functional Descriptions

3.11.3.1. Clock Sources

The THS gets one clock source. Table 3-9 describes the clock source for Thermal Sensor Controller. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 3- 9. Thermal Sensor Controller Clock Sources

Clock Sources	Description
OSC24M	24MHz clock

3.11.3.2. Timing Requirements

CLK_IN = 24 MHz
CONV_TIME(Conversion Time) = 1/(24 MHz/14 Cycles) =0.583 (us)
TACQ> 1/(24 MHz/24 Cycles)
THERMAL_PER > ADC Sample Frequency > TACQ+CONV_TIME

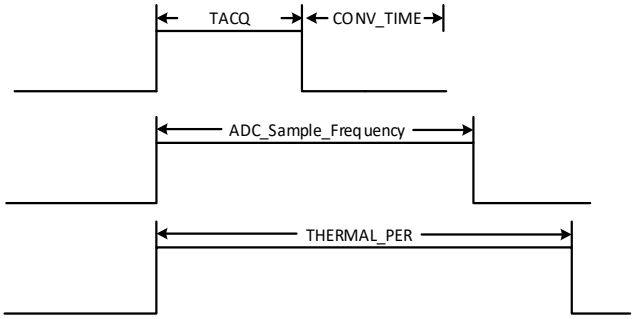


Figure 3- 23. Thermal Sensor Time Requirement

3.11.3.3. Interrupt

The THS has four interrupt sources, such as DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ and ALARM_OFF_IRQ. Figure 3-22 shows the thermal sensor interrupt sources.

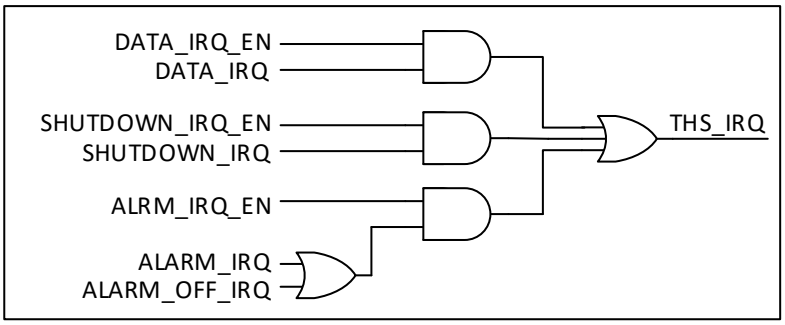


Figure 3- 24. Thermal Sensor Controller Interrupt Source

When temperature is higher than Alarm_Threshold (Alarm Threshold for hot temperature), ALARM_IRQ is generated. When temperature is lower than Alarm_Off_Thershold (Alarm threshold for hysteresis temperature), ALARM_OFF_IRQ is generated. And ALARM_OFF_IRQ is fall edge trigger.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.11.3.4. THS Temperature Conversion Formula

T= (sensor_data -2794)/(-14.882), the unit of T is Celsius.
sensor_data: read from sensor data register.

3.11.4. Programming Guidelines

The initial process of the THS is as follows.

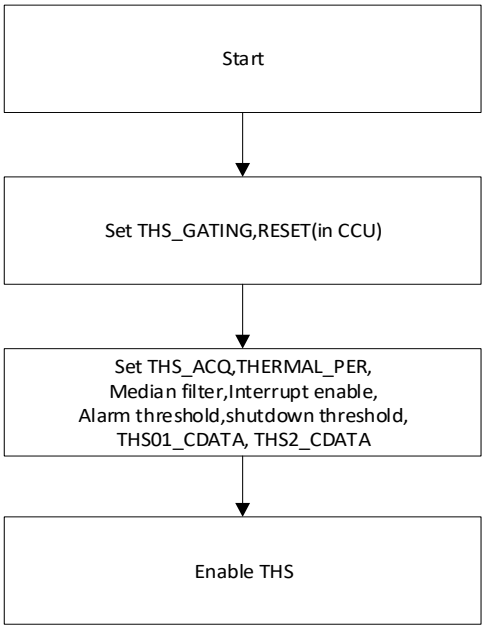


Figure 3- 25. THS Initial Process

The formula of THS is y=-ax+b. In FT stage, THS is calibrated through ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.

Before enabling THS, read EFUSE value and write the value to **THS01_CDATA, THS2_CDATA**.

(1).Query Mode

Step1: Write 0x1 to the bit16 of **THS_BGR_REG** to dessert reset.
Step2: Write 0x1 to the bit0 of **THS_BGR_REG** to open THS clock.
Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.
Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS_CDATA** to calibrate THS.
Step9: Write 0x1 to the bit[0] 0f **THS_EN** to enable THS.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step10: Read the bit[0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.
Step11: Read the bit[11:0] of **THS_DATA**, calculate THS temperature based on THS Temperature Conversion Formula in Section 3.10.3.4.

(2). Interrupt Mode

Step1: Write 0x1 to the bit16 of **THS_BGR_REG** to dessert reset.
Step2: Write 0x1 to the bit0 of **THS_BGR_REG** to open THS clock.
Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.
Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS_CDATA** to calibrate THS.
Step9: Write 0x1 to the bit[0] of **THS_DATA_INTC** to enable the interrupt of THS.
Step10: Set GIC interface based on IRQ 53, write the bit[21] of the 0x03021104 register to 0x1.
Step11: Put interrupt handler address into interrupt vector table.
Step12: Write 0x1 to the bit[0] 0f **THS_EN** to enable THS.
Step13: Read the bit[0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.
Step14: Read the bit[11:0] of **THS_DATA**, calculate THS temperature based on THS Temperature Conversion Formula in Section 3.10.3.4.

3.11.5. Register List

Module Name	Base Address
Thermal Sensor	0x05070400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm Threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm Threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm Threshold Control Register
THS01_SHUTDOWN_CTRL	0x0080	THS0 & THS1 Shutdown Threshold Control Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

THS2_SHUTDOWN_CTRL	0x0084	THS2 Shutdown Threshold Control Register
THS01_CDATA	0x00A0	THS0 & THS1 Calibration Data
THS2_CDATA	0x00A4	THS2 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register

3.11.6. Register Description

3.11.6.1. 0x0000 THS Control Register(Default Value : 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(N+1) , N > 0x17 The default value indicates 50 kHz.
15:0	R/W	0x2F	TACQ ADC Acquire Time CLK_IN/(n+1) The default value indicates 2us.

3.11.6.2. 0x0004 THS Enable Register(Default Value : 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:17	R/W	0x0	Ctrl for psensor
16	R/W	0x0	PSENSOR_EN Enable temperature measurement psensor 0:Sensor is T sensor 1:Sensor is P sensor
15:3	/	/	/
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Enable temperature measurement sensor0 0:Disable 1:Enable

3.11.6.3. 0x0008 THS Period Control Register(Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x3A	THERMAL_PER 4096*(n+1)/CLK_IN The default value indicates 10 ms.
11:0	/	/	/

3.11.6.4. 0x0010 THS Data Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	THS2_DATA_IRQ_EN Selects temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects temperature measurement data of sensor0 0:Disable 1:Enable

3.11.6.5. 0x0014 THS Shut Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.11.6.6. 0x0018 THS Alarm Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ALARM_INT2_EN Selects alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects alarm interrupt for sensor0 0:Disable 1:Enable

3.11.6.7. 0x0020 THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	THS2_DATA_IRQ _STS Data interrupt status for sensor2 Write ‘1’ to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ _STS Data interrupt status for sensor1 Write ‘1’ to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ _STS Data interrupt status for sensor0 Write ‘1’ to clear this interrupt.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.11.6.8. 0x0024 THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.9. 0x0028 THS Alarm Off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	ALARM_ OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_ OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_ OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.11.6.10. 0x002C THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.11.6.11. 0x0030 Median Filter Control Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

3.11.6.12. 0x0040 THS0 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal Sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal Sensor0 alarm threshold for hysteresis temperature

3.11.6.13. 0x0044 THS1 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal Sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal Sensor1 alarm threshold for hysteresis temperature

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.11.6.14. 0x0048 THS2 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal Sensor2 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal Sensor2 alarm threshold for hysteresis temperature

3.11.6.15. 0x0080 THS0&1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS01_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal Sensor1 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal Sensor0 shutdown threshold for hot temperature

3.11.6.16. 0x0084 THS2 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: THS2_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal Sensor2 shutdown threshold for hot temperature

3.11.6.17. 0x00A0 THS0&1 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS01_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.11.6.18. 0x00A4 THS2 Calibration Data Register (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: THS2_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.11.6.19. 0x00C0 THS0 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.11.6.20. 0x00C4 THS1 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.11.6.21. 0x00C8 THS2 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12. IOMMU

3.12.1. Overview

IOMMU(I/O Memory management unit) is designed for product specific memory requirements. It maps the virtual address(sent by peripheral access memory) to the physical address. IOMMU allows multiple ways to manage the location of physical address, and it can use physical address which has potentially conflict mapping for different processes to allocate memory space, and also allow application of non-continuous address mapping to continuous virtual address space.

Features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE, VE, CSI, ISP, G2D parallel address mapping
- Supports DE, VE, CSI, ISP, G2D bypass function independently
- Supports DE, VE, CSI, ISP, G2D prefetch independently
- Supports DE, VE, CSI, ISP, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

3.12.2. Block Diagram

The internal module of IOMMU mainly has the following parts.

Micro TLB: level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Prefetch Logic: Each Micro TLB corresponds to a Prefetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from memory and stored in the secondary TLB to improve hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address VA missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count hit efficiency and latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

Figure 3-26 shows the internal block diagram of IOMMU.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

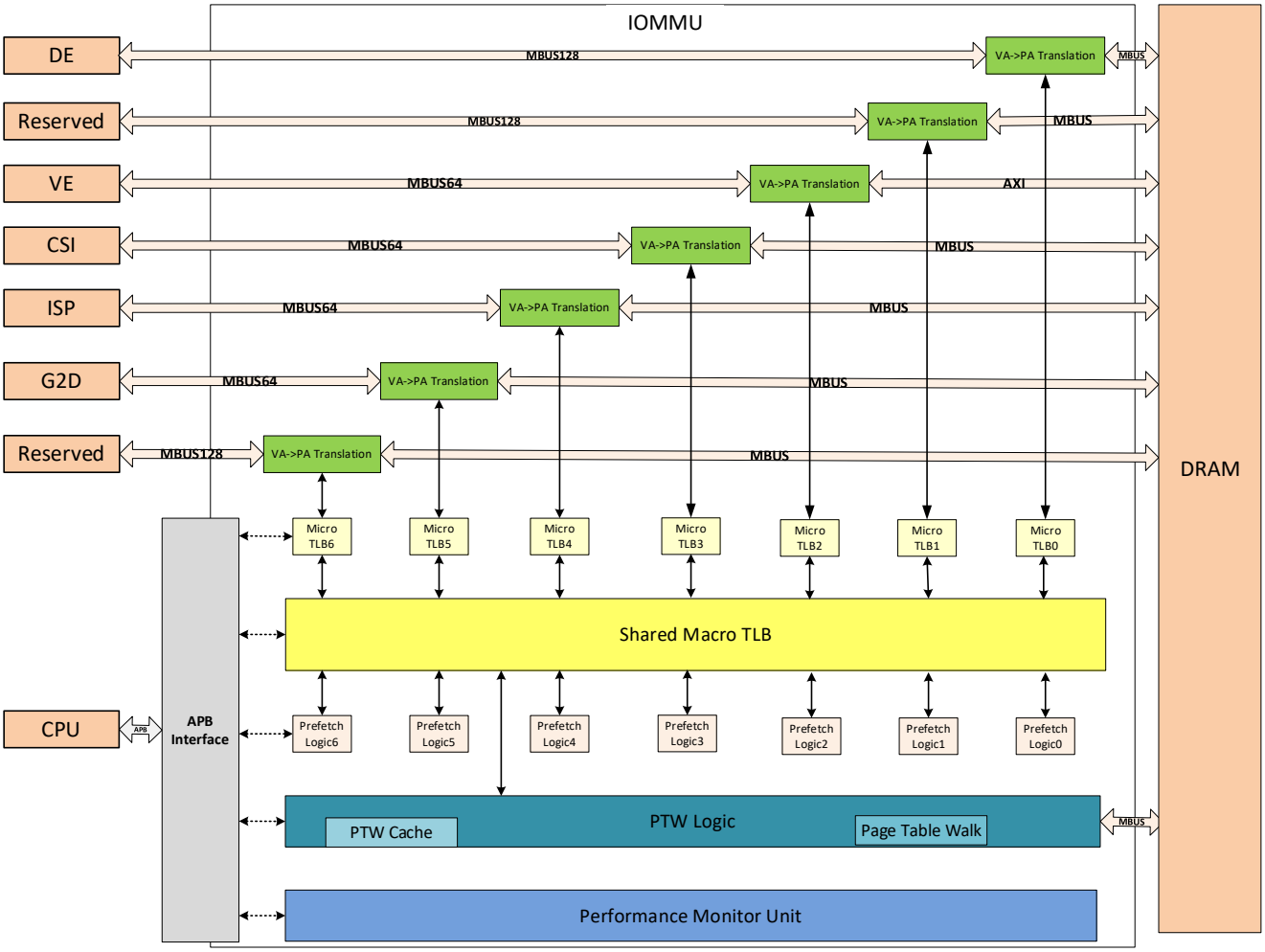


Figure 3- 26. IOMMU Block Diagram

Table 3- 10. Correspondence Relation between Master and Module

Master Number	Module
Master0	DE
Master1	Reserved
Master2	VE
Master3	CSI
Master4	ISP
Master5	G2D
Master6	Reserved

3.12.3. Operations and Functional Descriptions

3.12.3.1. Clock Sources

IOMMU contains two clock domains in the module. Address mapping is generated by MBUS clock domain, and Register and interrupt processing are generated by APB clock domain. The two domains are asynchronous, and they

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

are from different clock sources.

3.12.3.2. Operation Modes

3.12.3.2.1. Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the ***IOMMU Reset Register***;
- Write the base address of the first TLB to the ***IOMMU Translation Table Base Register***;
- Set the ***IOMMU Interrupt Enable Register***;
- Enable the IOMMU by configuring the ***IOMMU Enable Register*** in the final.

3.12.3.2.2. Address Changing

In the process of address mapping, The peripheral virtual address VA[31:12] are retrieved in the Level1 TLB, when TLB hits, the mapping finished, or they are retrieved in the Level2 TLB in the same way. If TLB hits, it will write the hit mapping to the Level1 TLB, and hits in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, it will trigger the PTW. After opening peripheral bypass function by setting IOMMU Bypass Register, IOMMU will not map the address for peripheral typed the address, and it will output the virtual address as physical address. The typical application is as follows.

- **Micro TLB hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB hits, it will return a corresponding physical addresses and the Level2 page table of permission Index;
c). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB misses, then continue to search Macro TLB;
c). If Macro TLB hits, it will return the Level2 page table to Micro TLB;
d). Micro TLB receives the page table, and puts it to Micro TLB(if this Micro TLB is full, there has replace activities), at the same time, sends page table entries to address translation module;
e). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB miss, PTW Cache hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB misses, then continue to search Macro TLB;
c). If Macro TLB misses, then it will send the request to the PTW to return the corresponding page table;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

d). PTW first accesses PTW Cache, confirms that the required Level1 page table exists in the PTW Cache, sends the page table to PTW logic;

e). PTW logic returns the corresponding Level2 page table from memory page table according to Level1 page table, checks the effectiveness, and sends to Macro TLB;

f). Macro TLB stores the Level2 page table (may happen replace activities), and will return the Level2 page table to Micro TLB;

g). Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;

h). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB miss, PTW Cache miss**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;

b). If Micro TLB misses, then continue to search Macro TLB;

c). If Macro TLB misses, there will send the request to the PTW to return the corresponding page table;

d). PTW accesses PTW Cache, there is no necessary Level1 page table;

e). PTW accesses memory, gets the corresponding Level1 page table and stores in the PTW Cache; (may happen replace activities)

f). PTW logic returns the corresponding Level2 page table from memory page table according to Level1 page table, checks the effectiveness, and sends to Macro TLB;

g). Macro TLB stores the Level2 page table (may happen replace activities), and will return the Level 2 page table to Micro TLB;

h). Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;

i). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Permission error**

a). Permission checking always performs in the address conversion;

b). Once the permission checking makes mistake, the new access of the master suspends, before this visit continues;

c). Set the error status register;

d). Trigger interrupt.

- **Invalid Level1 page table**

a). Invalid Level1 page table is checked when PTW logic reads the new level page table from memory;

b). The PTW read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the PTW cache;

c). If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in PTW Cache with target page table is found to be invalid after using;
If a page table is invalid, then total cache line(that is two page tables) need to be invalidated.

- **Invalid Level2 page table**

a). Invalid Level2 page table checks when Macro TLB reads the new level page table from memory;
b). The Macro TLB read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the Macro TLB;
c). If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in Macro TLB with target page table is found to be invalid after using.
If a page table is invalid, then total cache line(that is two page tables) need to be invalidated.

The internal address switch process shows in Figure 3-27.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

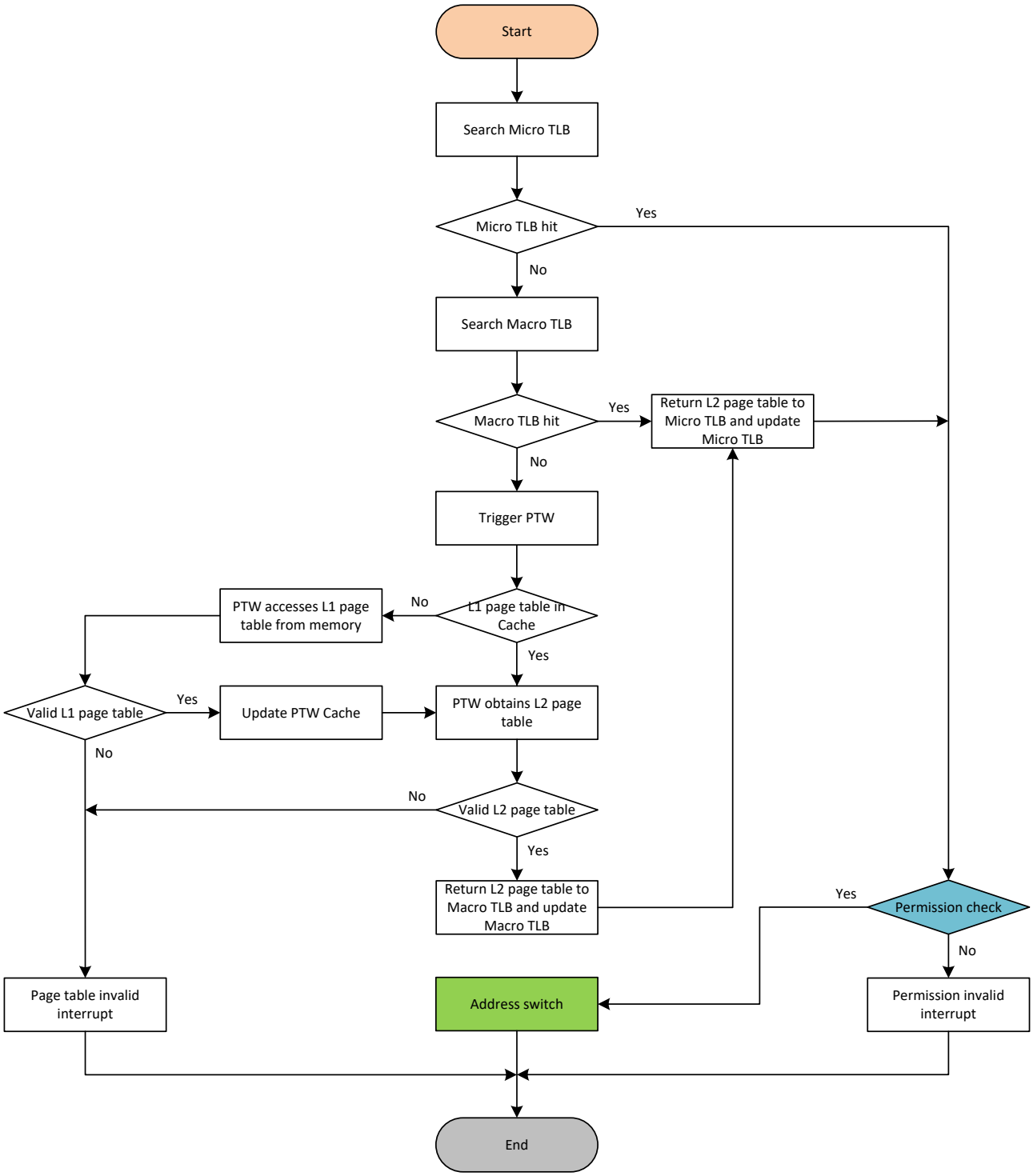


Figure 3- 27. Internal Switch Process

3.12.3.2.3. VA-PA Mapping

IOMMU page table is defined as Level2 mapping, the first level is 1M address space mapping, the second level is 4K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

address space. This version does not support 1K, 16K and other page table size. IOMMU supports a page table only, its meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of the page table is defined by software, and it needs 16 KB address alignment; Page table of the Level2 table item needs 1 KB address alignment. A complete VA-PA address translation process is shown in Figure 3-28.

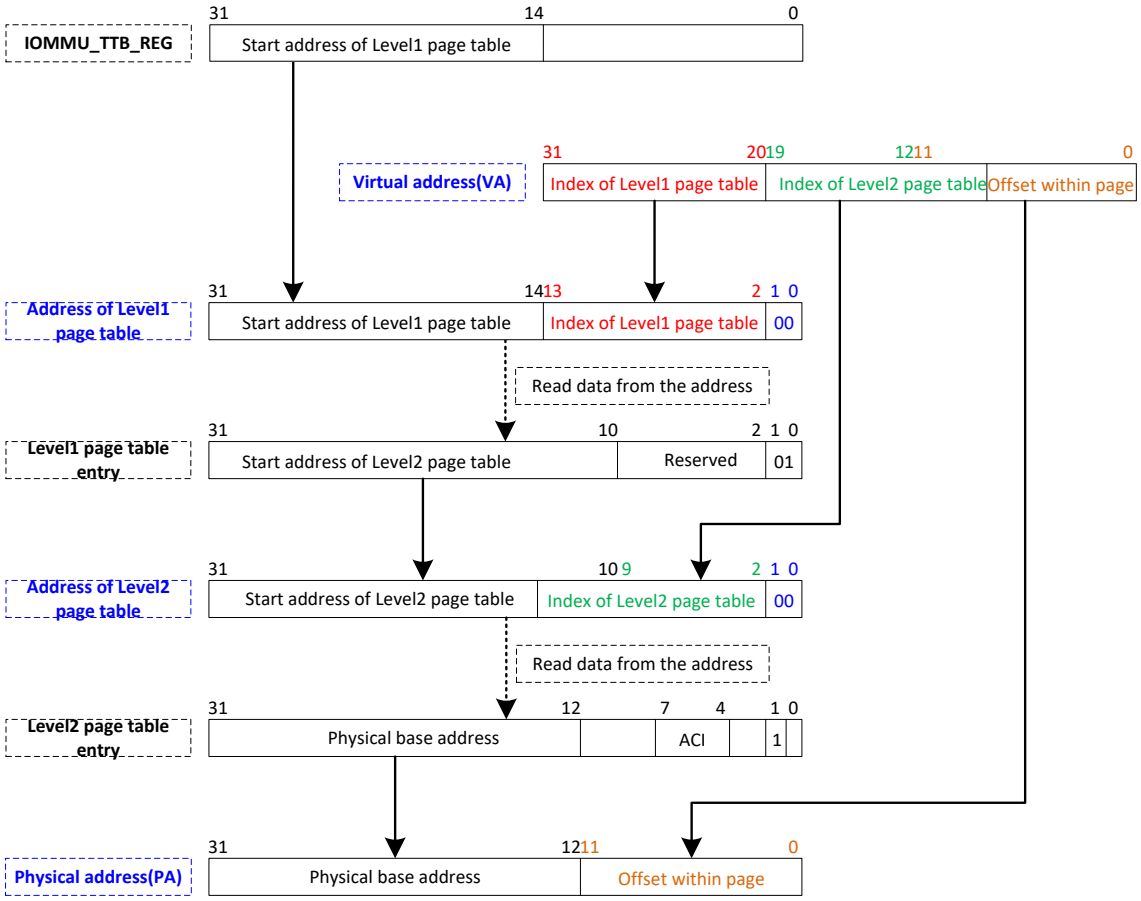


Figure 3- 28. VA-PA Switch Process

3.12.3.2.4. Clear and Invalidate TLB

When multi page table content refresh, or table address changes, all VA-PA mapping which has been cached in TLB will no longer be valid, then you need configure **IOMMU TLB Flush Enable Register** to clear the TLB or PTW Cache. First suspend access to TLB or Cache, then configure the corresponding Flush bit of **IOMMU TLB Flush Enable Register** , after operation takes effect, related peripherals can continue to send new access memory operations.

When some page table is invalid or incorrect mapping, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports two modes.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

(1) Mode0

Firstly, set **IOMMU TLB Invalidation Mode Select Register** to 0 to select mode0;
Secondly, write target address to **IOMMU TLB Invalidation Address Register**;
Thirdly, set configuration values to **IOMMU TLB Invalidation Address Mask Register**, the requirements are as follows:

- The value of **IOMMU TLB Invalidation Address Mask Register** cannot be less than the **IOMMU TLB Invalidation Address Register**.
- The higher bit of **IOMMU TLB Invalidation Address Mask Register** must be continuous 1, the lower bit must be continuous 0, for example, 0xfffff000, 0xffffe000, 0xffffc000, 0xffff8000, 0xffff0000 belongs to the legal value; and 0xffffd000, 0xffffb000, 0xfffa000, 0xffff9000, 0xffff7000 belongs to illegal values.

Finally, configure **IOMMU TLB Invalidation Enable Register** to enable invalid operation. Among the way to determine the invalid address is to get maximum valid bit and determine target address range by target address AND mask address. The process is shown as follows.

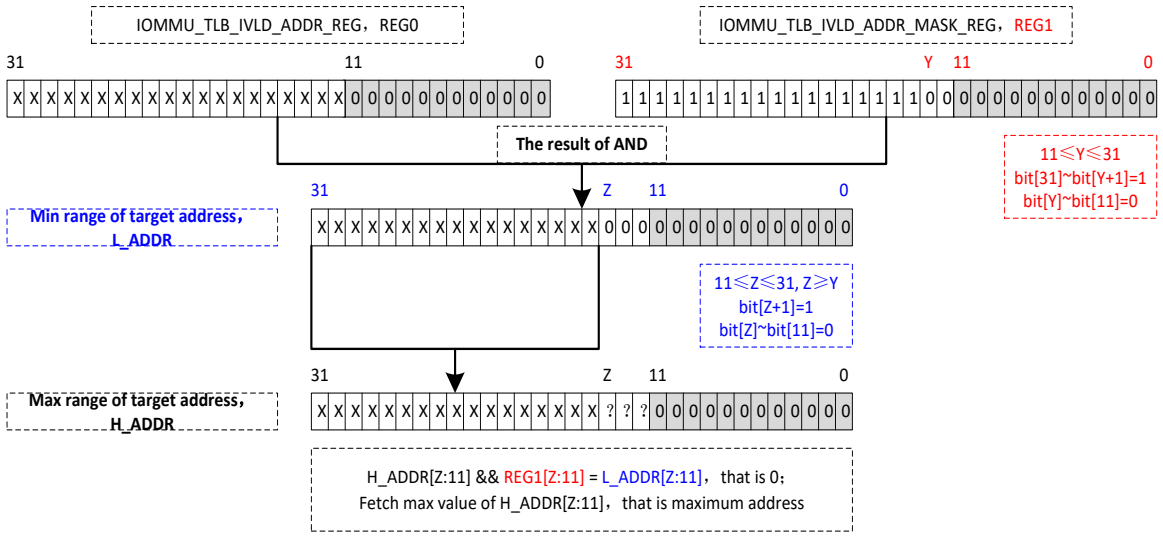


Figure 3- 29. Invalid TLB Address Range

For example:
a). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFF000 by default, the result of AND is target address, that is, only target address is invalid.
b). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF0000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.
c). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.
d). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF8000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.
e). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

(2) Mode1

Firstly, set **IOMMU TLB Invalidation Mode Select Register** to 1 to select mode1;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Secondly, set the starting address of invalid TLB by **IOMMU TLB Invalidation Start Address Register,** and set the ending address of invalid TLB **by IOMMU TLB Invalidation Start Address Register;**
Finally, configure **IOMMU TLB Invalidation Enable Register** to enable invalid operation, then invalid related TLB operation can be completed.

3.12.3.3. Page Table Format

3.12.3.3.1. Level1 Page Table

The format of Level1 page table is as follows.

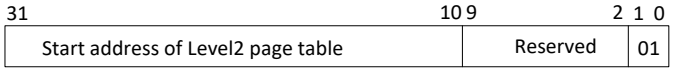


Figure 3- 30. Level1 Page Table Format

Bit[31:10]: Base address of Level2 page table;
Bit[9:2]: Reserved;
Bit[1:0]: 01 is valid page table; others are fault;

3.12.3.3.2. Level2 Page Table

The format of Level2 page table is as follows.

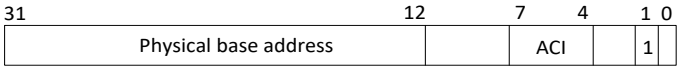


Figure 3- 31. Level1 Page Table Format

Bit[31:12]: Physical address of 4K address;
Bit[11:8]: Reserved;
Bit[7:4]: ACI, permission control index; correspond to permission control bit of **IOMMU Domain Authority Control Register**;
Bit[3:2]: Reserved;
Bit[1]: 1 is valid page table; 0 is fault;
Bit[0]: Reserved

3.12.3.3.3. Permission Index

The read/write access control of series register such as **IOMMU Domain Authority Control Register** is as follows.

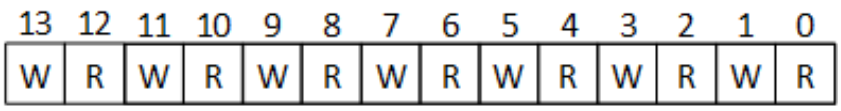


Figure 3- 32. Read/Write Permission Control

Bit[1:0]/Bit[17:16]: Master0 read/write permission control;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit[3:2]/Bit[19:18]: Master1 read/write permission control;
Bit[5:4]/Bit[21:20]: Master2 read/write permission control;
Bit[7:6]/Bit[23:22]: Master3 read/write permission control;
Bit[9:8]/Bit[25:24]: Master4 read/write permission control;
Bit[11:10]/Bit[27:26]: Master5 read/write permission control;
Bit[13:12]/Bit[29:28]: Master6 read/write permissiom control.

The value of **IOMMU Domain Authority Control Register** is read-only by default. Other registers can configure through system requirement. In address switch process, the corresponding relation between ACI and Domain is as follows.

Table 3- 11. Relation between ACI and Domain

ACI	Domain	Register
0	Domain 0	IOMMU Domain Authority Control Register 0
1	Domain 1	IOMMU Domain Authority Control Register 0
2	Domain 2	IOMMU Domain Authority Control Register 1
3	Domain 3	IOMMU Domain Authority Control Register 1
4	Domain 4	IOMMU Domain Authority Control Register 2
5	Domain 5	IOMMU Domain Authority Control Register 2
6	Domain 6	IOMMU Domain Authority Control Register 3
7	Domain 7	IOMMU Domain Authority Control Register 3
8	Domain 8	IOMMU Domain Authority Control Register 4
9	Domain 9	IOMMU Domain Authority Control Register 4
10	Domain 10	IOMMU Domain Authority Control Register 5
11	Domain 11	IOMMU Domain Authority Control Register 5
12	Domain 12	IOMMU Domain Authority Control Register 6
13	Domain 13	IOMMU Domain Authority Control Register 6
14	Domain 14	IOMMU Domain Authority Control Register 7
15	Domain 15	IOMMU Domain Authority Control Register 7

After enabled **IOMMU Domain Authority Overwrite Register**, the read/write control permission can override all **IOMMU Domain Authority Control Register**.

3.12.4. Programming Guidelines

3.12.4.1. IOMMU Reset

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

3.12.4.2. IOMMU Enable

Before opening the IOMMU address mapping function, Translation Table Base register should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.4.3. Configure TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG [0] is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

3.12.4.4. Clear TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

3.12.4.5. Read/Write VA Data

For virtual address, read and write the corresponding physical address data to make sure whether IOMMU module address mapping function is normal. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

3.12.4.6. PMU Statistics

When PMU function is used for the first time, set **IOMMU PMU Enable Register** to enable statistics function; when reading the relevant Register, clear the enable bit of **IOMMU PMU Enable Register**; when PMU function is used next time, first **IOMMU PMU Clear Register** is set, after counter is cleared, set the enable bit of **IOMMU PMU Enable Register**.

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, there may need to return a Level2 page table to hit from Macro TLB; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number
M1: Micro TLB access number
N2: Macro TLB hit number
M2: Macro TLB access number

3.12.5. Register List

Module Name	Base Address
IOMMU	0x030F0000

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
IOMMU_RESET _REG	0x0010	IOMMU ResetRegister
IOMMU_ENABLE_REG	0x0020	IOMMU EnableRegister
IOMMU_BYPASS_REG	0x0030	IOMMU BypassRegister
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto GatingRegister
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table BaseRegister
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB EnableRegister
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB PrefetchRegister
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_DM_AUT_CTRL_REG0	0x00B0	IOMMU Domain Authority Control Register 0
IOMMU_DM_AUT_CTRL_REG1	0x00B4	IOMMU Domain Authority Control Register 1
IOMMU_DM_AUT_CTRL_REG2	0x00B8	IOMMU Domain Authority Control Register 2
IOMMU_DM_AUT_CTRL_REG3	0x00BC	IOMMU Domain Authority Control Register 3
IOMMU_DM_AUT_CTRL_REG4	0x00C0	IOMMU Domain Authority Control Register 4
IOMMU_DM_AUT_CTRL_REG5	0x00C4	IOMMU Domain Authority Control Register 5
IOMMU_DM_AUT_CTRL_REG6	0x00C8	IOMMU Domain Authority Control Register 6
IOMMU_DM_AUT_CTRL_REG7	0x00CC	IOMMU Domain Authority Control Register 7
IOMMU_DM_AUT_OVWT_REG	0x00D0	IOMMU Domain Authority Overwrite Register
IOMMU_INT_ENABLE _REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR _REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA _REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR_REG0	0x0110	IOMMU Interrupt Error Address Register 0
IOMMU_INT_ERR_ADDR_REG1	0x0114	IOMMU Interrupt Error Address Register 1
IOMMU_INT_ERR_ADDR_REG2	0x0118	IOMMU Interrupt Error Address Register 2
IOMMU_INT_ERR_ADDR_REG3	0x011C	IOMMU Interrupt Error Address Register 3
IOMMU_INT_ERR_ADDR_REG4	0x0120	IOMMU Interrupt Error Address Register 4
IOMMU_INT_ERR_ADDR_REG5	0x0124	IOMMU Interrupt Error Address Register 5
IOMMU_INT_ERR_ADDR_REG6	0x0128	IOMMU Interrupt Error Address Register 6
IOMMU_INT_ERR_ADDR_REG7	0x0130	IOMMU Interrupt Error Address Register 7
IOMMU_INT_ERR_ADDR_REG8	0x0134	IOMMU Interrupt Error Address Register 8
IOMMU_INT_ERR_DATA_REG0	0x0150	IOMMU Interrupt Error Data Register 0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

IOMMU_INT_ERR_DATA_REG1	0x0154	IOMMU Interrupt Error Data Register 1
IOMMU_INT_ERR_DATA_REG2	0x0158	IOMMU Interrupt Error Data Register 2
IOMMU_INT_ERR_DATA_REG3	0x015C	IOMMU Interrupt Error Data Register 3
IOMMU_INT_ERR_DATA_REG4	0x0160	IOMMU Interrupt Error Data Register 4
IOMMU_INT_ERR_DATA_REG5	0x0164	IOMMU Interrupt Error Data Register 5
IOMMU_INT_ERR_DATA_REG6	0x0168	IOMMU Interrupt Error Data Register 6
IOMMU_INT_ERR_DATA_REG7	0x0170	IOMMU Interrupt Error Data Register 7
IOMMU_INT_ERR_DATA_REG8	0x0174	IOMMU Interrupt Error Data Register 8
IOMMU_L1PG_INT _REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT _REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE _REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR _REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW_REG0	0x0230	IOMMU PMU Access Low Register 0
IOMMU_PMU_ACCESS_HIGH_REG0	0x0234	IOMMU PMU Access High Register 0
IOMMU_PMU_HIT_LOW_REG0	0x0238	IOMMU PMU Hit Low Register 0
IOMMU_PMU_HIT_HIGH_REG0	0x023C	IOMMU PMU Hit High Register 0
IOMMU_PMU_ACCESS_LOW_REG1	0x0240	IOMMU PMU Access Low Register 1
IOMMU_PMU_ACCESS_HIGH_REG1	0x0244	IOMMU PMU Access High Register 1
IOMMU_PMU_HIT_LOW_REG1	0x0248	IOMMU PMU Hit Low Register 1
IOMMU_PMU_HIT_HIGH_REG1	0x024C	IOMMU PMU Hit High Register 1
IOMMU_PMU_ACCESS_LOW_REG2	0x0250	IOMMU PMU Access Low Register 2
IOMMU_PMU_ACCESS_HIGH_REG2	0x0254	IOMMU PMU Access High Register 2
IOMMU_PMU_HIT_LOW_REG2	0x0258	IOMMU PMU Hit Low Register 2
IOMMU_PMU_HIT_HIGH_REG2	0x025C	IOMMU PMU Hit High Register 2
IOMMU_PMU_ACCESS_LOW_REG3	0x0260	IOMMU PMU Access Low Register 3
IOMMU_PMU_ACCESS_HIGH_REG3	0x0264	IOMMU PMU Access High Register 3
IOMMU_PMU_HIT_LOW_REG3	0x0268	IOMMU PMU Hit Low Register 3
IOMMU_PMU_HIT_HIGH_REG3	0x026C	IOMMU PMU Hit High Register 3
IOMMU_PMU_ACCESS_LOW_REG4	0x0270	IOMMU PMU Access Low Register 4
IOMMU_PMU_ACCESS_HIGH_REG4	0x0274	IOMMU PMU Access High Register 4
IOMMU_PMU_HIT_LOW_REG4	0x0278	IOMMU PMU Hit Low Register 4
IOMMU_PMU_HIT_HIGH_REG4	0x027C	IOMMU PMU Hit High Register 4
IOMMU_PMU_ACCESS_LOW_REG5	0x0280	IOMMU PMU Access Low Register 5
IOMMU_PMU_ACCESS_HIGH_REG5	0x0284	IOMMU PMU Access High Register 5
IOMMU_PMU_HIT_LOW_REG5	0x0288	IOMMU PMU Hit Low Register 5
IOMMU_PMU_HIT_HIGH_REG5	0x028C	IOMMU PMU Hit High Register 5
IOMMU_PMU_ACCESS_LOW_REG6	0x0290	IOMMU PMU Access Low Register 6
IOMMU_PMU_ACCESS_HIGH_REG6	0x0294	IOMMU PMU Access High Register 6
IOMMU_PMU_HIT_LOW_REG6	0x0298	IOMMU PMU Hit Low Register 6
IOMMU_PMU_HIT_HIGH_REG6	0x029C	IOMMU PMU Hit High Register 6
IOMMU_PMU_ACCESS_LOW_REG7	0x02D0	IOMMU PMU Access Low Register 7

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

IOMMU_PMU_ACCESS_HIGH_REG7	0x02D4	IOMMU PMU Access High Register 7
IOMMU_PMU_HIT_LOW_REG7	0x02D8	IOMMU PMU Hit Low Register 7
IOMMU_PMU_HIT_HIGH_REG7	0x02DC	IOMMU PMU Hit High Register 7
IOMMU_PMU_ACCESS_LOW_REG8	0x02E0	IOMMU PMU Access Low Register 8
IOMMU_PMU_ACCESS_HIGH_REG8	0x02E4	IOMMU PMU Access High Register 8
IOMMU_PMU_HIT_LOW_REG8	0x02E8	IOMMU PMU Hit Low Register 8
IOMMU_PMU_HIT_HIGH_REG8	0x02EC	IOMMU PMU Hit High Register 8
IOMMU_PMU_TL_LOW_REG0	0x0300	IOMMU Total Latency Low Register 0
IOMMU_PMU_TL_HIGH_REG0	0x0304	IOMMU Total Latency High Register 0
IOMMU_PMU_ML _REG0	0x0308	IOMMU Max Latency Register 0
IOMMU_PMU_TL_LOW_REG1	0x0310	IOMMU Total Latency Low Register 1
IOMMU_PMU_TL_HIGH_REG1	0x0314	IOMMU Total Latency High Register 1
IOMMU_PMU_ML _REG1	0x0318	IOMMU Max Latency Register 1
IOMMU_PMU_TL_LOW_REG2	0x0320	IOMMU Total Latency Low Register 2
IOMMU_PMU_TL_HIGH_REG2	0x0324	IOMMU Total Latency High Register 2
IOMMU_PMU_ML _REG2	0x0328	IOMMU Max Latency Register 2
IOMMU_PMU_TL_LOW_REG3	0x0330	IOMMU Total Latency Low Register 3
IOMMU_PMU_TL_HIGH_REG3	0x0334	IOMMU Total Latency High Register 3
IOMMU_PMU_ML _REG3	0x0338	IOMMU Max Latency Register 3
IOMMU_PMU_TL_LOW_REG4	0x0340	IOMMU Total Latency Low Register 4
IOMMU_PMU_TL_HIGH_REG4	0x0344	IOMMU Total Latency High Register 4
IOMMU_PMU_ML _REG4	0x0348	IOMMU Max Latency Register 4
IOMMU_PMU_TL_LOW_REG5	0x0350	IOMMU Total Latency Low Register 5
IOMMU_PMU_TL_HIGH_REG5	0x0354	IOMMU Total Latency High Register 5
IOMMU_PMU_ML _REG5	0x0358	IOMMU Max Latency Register 5
IOMMU_PMU_TL_LOW_REG6	0x0360	IOMMU Total Latency Low Register 6
IOMMU_PMU_TL_HIGH_REG6	0x0364	IOMMU Total Latency High Register 6
IOMMU_PMU_ML _REG6	0x0368	IOMMU Max Latency Register 6

3.12.6. Register Description

3.12.6.1. 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			**Register Name: IOMMU_RESET _REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	IOMMU_RESET IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; Or all bus operations are completed; Or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30:18	/	/	/
17	R/W	0x1	PTW_CACHE_RESET PTW Cache address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.
16	R/W	0x1	MACRO_TLB_RESET Macro TLB address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.
15:7	/	/	/
6	R/W	0x1	MASTER6_RESET Master6 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, the bit is used to reset PTW Cache individually.
5	R/W	0x1	MASTER5_RESET Master5 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, the bit is used to reset PTW Cache individually.
4	R/W	0x1	MASTER4_RESET Master4 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, the bit is used to reset PTW Cache individually.
3	R/W	0x1	MASTER3_RESET Master3 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, the bit is used to reset PTW Cache individually.
2	R/W	0x1	MASTER2_RESET Master2 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, the bit is used to reset PTW Cache individually.
1	R/W	0x1	MASTER1_RESET

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Master1 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, the bit is used to reset PTW Cache individually.
0	R/W	0x1	MASTER0_RESET Master0 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, the bit is used to reset PTW Cache individually.

3.12.6.2. 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before IOMMU address mapping function opens, configure the Translation Table Base register; or ensure all masters are in bypass status or no the status of sending bus demand(such as reset)

3.12.6.3. 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007F)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_BYPASS Master6 bypass switch After bypass function is opened, IOMMU can not map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
5	R/W	0x1	MASTER5_BYPASS Master5 bypass switch After bypass function is opened, IOMMU can not map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable bypass function
4	R/W	0x1	MASTER4_BYPASS Master4 bypass switch After bypass function is opened, IOMMU can not map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
3	R/W	0x1	MASTER3_BYPASS Master3 bypass switch After bypass function is opened, IOMMU can not map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x1	MASTER2_BYPASS Master2 bypass switch After bypass function is opened, IOMMU can not map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
1	R/W	0x1	MASTER1_BYPASS Master1 bypass switch After bypass function is opened, IOMMU can not map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x1	MASTER0_BYPASS Master0 bypass switch After bypass function is opened, IOMMU can not map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

Operating the register belongs to non-accurate timing sequence control function. That is, before the function is valid, master operation will complete address mapping function, and after the operation will not perform address mapping. It is suggested that master is in reset state or in no any bus operation before operating the register .

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.4. 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control. The purpose is decreasing power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

3.12.6.5. 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_007F)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	Reserved
5	R/W	0x1	MASTER5_WBUF_CTRL Master5 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: G2D does not write buffer, so the bit is invalid.**
4	R/W	0x1	MASTER4_WBUF_CTRL Master4 write buffer control bit 0: Disable write buffer 1: Enable write buffer
3	R/W	0x1	MASTER3_WBUF_CTRL Master3 write buffer control bit 0: Disable write buffer 1: Enable write buffer
2	R/W	0x1	MASTER2_WBUF_CTRL Master2 write buffer control bit 0: Disable write buffer 1: Enable write buffer
1	R/W	0x1	MASTER1_WBUF_CTRL Master1 write buffer control bit 0: Disable write buffer 1: Enable write buffer
0	R/W	0x1	MASTER0_WBUF_CTRL Master0 write buffer control bit 0: Disable write buffer 1: Enable write buffer

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.6. 0x0048 IOMMU Out Of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_OOO_CTRL Master6 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
5	R/W	0x1	MASTER5_OOO_CTRL Master5 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	MASTER4_OOO_CTRL Master4 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	MASTER3_OOO_CTRL Master3 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
2	R/W	0x1	MASTER2_OOO_CTRL Master2 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	MASTER1_OOO_CTRL Master1 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	MASTER0_OOO_CTRL Master0 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

3.12.6.7. 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_4KB_BDY_PRT_CTRL Master6 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W	0x1	MASTER5_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
4	R/W	0x1	MASTER4_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
3	R/W	0x1	MASTER3_4KB_BDY_PRT_CTRL Master3 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
2	R/W	0x1	MASTER2_4KB_BDY_PRT_CTRL Master2 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
1	R/W	0x1	MASTER1_4KB_BDY_PRT_CTRL Master1 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
0	R/W	0x1	MASTER0_4KB_BDY_PRT_CTRL Master0 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect

NOTE

When the virtual address sent by master is over the 4KB boundary, 4KB protection unit will split it into two serial access.

3.12.6.8. 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	R/W	0x0	TTB Level1 page table starting address, aligned to 16 KB. When operating the register, IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or Bypass function of all main equipment is set to 1, or no the state of transfer bus commands (such as setting).
13:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.9. 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x1	PTW_CACHE_ENABLE PTW Cache enable bit 0: Disable 1: Enable
16	R/W	0x1	MACRO_TLB_ENABLE Macro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO_TLB1_ENABLE Micro TLB1 enable bit 0: Disable 1: Enable
0	R/W	0x1	MICRO_TLB0_ENABLE Micro TLB0 enable bit 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.10. 0x0070 IOMMU TLB Prefetch Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	MICRO_TLB6_PREFETCH Micro TLB6 prefetch enable 0: Disable 1: Enable
5	R/W	0x0	MICRO_TLB5_PREFETCH Micro TLB5 prefetch enable 0: Disable 1: Enable **Note: When G2D accesses DDR, the prefetch function is suggested to disable.**
4	R/W	0x0	MICRO_TLB4_PREFETCH Micro TLB4 prefetch enable 0: Disable 1: Enable
3	R/W	0x0	MICRO_TLB3_PREFETCH Micro TLB3 prefetch enable 0: Disable 1: Enable
2	R/W	0x0	MICRO_TLB2_PREFETCH Micro TLB2 prefetch enable 0: Disable 1: Enable
1	R/W	0x0	MICRO_TLB1_PREFETCH Micro TLB1 prefetch enable 0: Disable 1: Enable
0	R/W	0x0	MICRO_TLB0_PREFETCH Micro TLB0 prefetch enable 0: Disable 1: Enable

3.12.6.11. 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PTW_CACHE_FLUSH Clear PTW Cache 0: No clear operation or clear operation completed

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
16	R/WAC	0x0	MACRO_TLB_FLUSH Clear Macro TLB 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
15:7	/	/	/
6	R/WAC	0x0	MICRO_TLB6_FLUSH Clear Micro TLB6 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
5	R/WAC	0x0	MICRO_TLB5_FLUSH Clear Micro TLB5 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
4	R/WAC	0x0	MICRO_TLB4_FLUSH Clear Micro TLB4 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
3	R/WAC	0x0	MICRO_TLB3_FLUSH Clear Micro TLB3 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
2	R/WAC	0x0	MICRO_TLB2_FLUSH Clear Micro TLB2 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
1	R/WAC	0x0	MICRO_TLB1_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
0	R/WAC	0x0	MICRO_TLB0_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.

NOTE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

When performing flush operation, all TLB/Cache access will be paused.
Before flush starts, the operation that has entered TLB continues to complete.

3.12.6.12. 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL 0: Use invalid TLB with Mask mode 1: Use invalid TLB with Start and End mode

3.12.6.13. 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_STA_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.12.6.14. 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: IOMMU_TLB_IVLD_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_END_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.12.6.15. 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR TLB invalid address, 4KB aligned
11:0	/	/	/

Operation:

1) Set the virtual address which needs to be operated in **IOMMU_TLB_IVLD_ADDR_REG**.
2) Set the mask of virtual address which needs to be operated in **IOMMU_TLB_IVLD_ADDR_MASK_REG**.
3) Write '1' to **IOMMU_TLB_IVLD_ENABLE_REG[0].**
4) Read **IOMMU_TLB_IVLD_ENABLE_REG[0]**, when it is '0', it indicates that invalidation behavior is finished.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

When performing invalidation operation, TLB/Cache operation has not affected.

After or Before invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.16. 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB invalid address mask register, 4KB aligned
11:0	/	/	/

3.12.6.17. 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	TLB_IVLD_ENABLE Enable TLB invalid operation 0: No-operation or operation completed 1: Enable is invalid After invalidation operation completed, the bit can clear 0 automatically. When operating Invalidation, TLB/Cache operation has not affected. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.18. 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	PC_IVLD_ADDR PTW Cache invalid address, 1MB aligned.
19:0	/	/	/

3.12.6.19. 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8	Register Name: IOMMU_PC_IVLD_ENABLE_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_ENABLE Enable PTW Cache invalid operation 0: No-operation or operation completed 1: Enable is invalid After invalidation operation completed, the bit can clear 0 automatically. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.20. 0x00B0 IOMMU Domain Authority Control Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM1_M6_WT_AUT_CTRL Domain1 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM1_M6_RD_AUT_CTRL Domain1 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM1_M5_WT_AUT_CTRL Domain1 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM1_M5_RD_AUT_CTRL Domain1 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM1_M4_WT_AUT_CTRL Domain1 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM1_M4_RD_AUT_CTRL Domain1 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM1_M3_WT_AUT_CTRL Domain1 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM1_M3_RD_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain1 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM1_M2_WT_AUT_CTRL Domain1 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
20	R/W	0x0	DM1_M2_RD_AUT_CTRL Domain1 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM1_M1_WT_AUT_CTRL Domain1 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM1_M1_RD_AUT_CTRL Domain1 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM1_M0_WT_AUT_CTRL Domain1 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM1_M0_RD_AUT_CTRL Domain1 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R	0x0	DM0_M6_WT_AUT_CTRL Domain0 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R	0x0	DM0_M6_RD_AUT_CTRL Domain0 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R	0x0	DM0_M5_WT_AUT_CTRL Domain0 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R	0x0	DM0_M5_RD_AUT_CTRL Domain0 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R	0x0	DM0_M4_WT_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain0 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R	0x0	DM0_M4_RD_AUT_CTRL Domain0 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R	0x0	DM0_M3_WT_AUT_CTRL Domain0 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R	0x0	DM0_M3_RD_AUT_CTRL Domain0 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R	0x0	DM0_M2_WT_AUT_CTRL Domain0 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R	0x0	DM0_M2_RD_AUT_CTRL Domain0 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R	0x0	DM0_M1_WT_AUT_CTRL Domain0 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R	0x0	DM0_M1_RD_AUT_CTRL Domain0 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R	0x0	DM0_M0_WT_AUT_CTRL Domain0 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R	0x0	DM0_M0_RD_AUT_CTRL Domain0 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

NOTE

Software can be set up 15 different permission control types , which are set in IOMMU_DM_AUT_CTRL_REG0 ~ 7. As well as a default access control type, domain0. The read/write operation of DOMIAN1 ~ 15 is unlimited by default.

Software needs to set the corresponding permission control domain index of the page table item in the secondary

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

page table entries[7:4], the default value is 0, use domian0, namely the read/write operation is not controlled. Setting REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All Level2 page table type are covered by the type of REG_ARD_OVWT. The read/write operation is permitted by default.

3.12.6.21. 0x00B4 IOMMU Domain Authority Control Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM3_M6_WT_AUT_CTRL Domain3 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM3_M6_RD_AUT_CTRL Domain3 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM3_M5_WT_AUT_CTRL Domain3 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM3_M5_RD_AUT_CTRL Domain3 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM3_M4_WT_AUT_CTRL Domain3 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM3_M4_RD_AUT_CTRL Domain3 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM3_M3_WT_AUT_CTRL Domain3 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM3_M3_RD_AUT_CTRL Domain3 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM3_M2_WT_AUT_CTRL Domain3 write permission control for master2 0: The write-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The write-operation is prohibited
20	R/W	0x0	DM3_M2_RD_AUT_CTRL Domain3 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM3_M1_WT_AUT_CTRL Domain3 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM3_M1_RD_AUT_CTRL Domain3 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM3_M0_WT_AUT_CTRL Domain3 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM3_M0_RD_AUT_CTRL Domain3 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM2_M6_WT_AUT_CTRL Domain2 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM2_M6_RD_AUT_CTRL Domain2 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	DM2_M5_WT_AUT_CTRL Domain2 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM2_M5_RD_AUT_CTRL Domain2 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM2_M4_WT_AUT_CTRL Domain2 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM2_M4_RD_AUT_CTRL Domain2 read permission control for master4 0: The read-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The read-operation is prohibited
7	R/W	0x0	DM2_M3_WT_AUT_CTRL Domain2 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM2_M3_RD_AUT_CTRL Domain2 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM2_M2_WT_AUT_CTRL Domain2 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM2_M2_RD_AUT_CTRL Domain2 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM2_M1_WT_AUT_CTRL Domain2 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM2_M1_RD_AUT_CTRL Domain2 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM2_M0_WT_AUT_CTRL Domain2 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM2_M0_RD_AUT_CTRL Domain2 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.22. 0x00B8 IOMMU Domain Authority Control Register 2 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM5_M6_WT_AUT_CTRL Domain5 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM5_M6_RD_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain5 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM5_M5_WT_AUT_CTRL Domain5 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM5_M5_RD_AUT_CTRL Domain5 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM5_M4_WT_AUT_CTRL Domain5 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM5_M4_RD_AUT_CTRL Domain5 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM5_M3_WT_AUT_CTRL Domain5 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM5_M3_RD_AUT_CTRL Domain5 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM5_M2_WT_AUT_CTRL Domain5 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
20	R/W	0x0	DM5_M2_RD_AUT_CTRL Domain5 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM5_M1_WT_AUT_CTRL Domain5 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM5_M1_RD_AUT_CTRL Domain5 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM5_M0_WT_AUT_CTRL Domain5 write permission control for master0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM5_M0_RD_AUT_CTRL Domain5 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM4_M6_WT_AUT_CTRL Domain4 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM4_M6_RD_AUT_CTRL Domain4 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	DM4_M5_WT_AUT_CTRL Domain4 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM4_M5_RD_AUT_CTRL Domain4 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM4_M4_WT_AUT_CTRL Domain4 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM4_M4_RD_AUT_CTRL Domain4 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	DM4_M3_WT_AUT_CTRL Domain4 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM4_M3_RD_AUT_CTRL Domain4 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM4_M2_WT_AUT_CTRL Domain4 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM4_M2_RD_AUT_CTRL Domain4 read permission control for master2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM4_M1_WT_AUT_CTRL Domain4 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM4_M1_RD_AUT_CTRL Domain4 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM4_M0_WT_AUT_CTRL Domain4 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM4_M0_RD_AUT_CTRL Domain4 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.23. 0x00BC IOMMU Domain Authority Control Register 3 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM7_M6_WT_AUT_CTRL Domain7 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM7_M6_RD_AUT_CTRL Domain7 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM7_M5_WT_AUT_CTRL Domain7 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM7_M5_RD_AUT_CTRL Domain7 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM7_M4_WT_AUT_CTRL Domain7 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

24	R/W	0x0	DM7_M4_RD_AUT_CTRL Domain7 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM7_M3_WT_AUT_CTRL Domain7 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM7_M3_RD_AUT_CTRL Domain7 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM7_M2_WT_AUT_CTRL Domain7 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
20	R/W	0x0	DM7_M2_RD_AUT_CTRL Domain7 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM7_M1_WT_AUT_CTRL Domain7 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM7_M1_RD_AUT_CTRL Domain7 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM7_M0_WT_AUT_CTRL Domain7 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM7_M0_RD_AUT_CTRL Domain7 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM6_M6_WT_AUT_CTRL Domain6 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM6_M6_RD_AUT_CTRL Domain6 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	R/W	0x0	DM6_M5_WT_AUT_CTRL Domain6 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM6_M5_RD_AUT_CTRL Domain6 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM6_M4_WT_AUT_CTRL Domain6 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM6_M4_RD_AUT_CTRL Domain6 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	DM6_M3_WT_AUT_CTRL Domain6 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM6_M3_RD_AUT_CTRL Domain6 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM6_M2_WT_AUT_CTRL Domain6 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM6_M2_RD_AUT_CTRL Domain6 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM6_M1_WT_AUT_CTRL Domain6 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM6_M1_RD_AUT_CTRL Domain6 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM6_M0_WT_AUT_CTRL Domain6 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM6_M0_RD_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain6 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.24. 0x00C0 IOMMU Domain Authority Control Register 4 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM9_M6_WT_AUT_CTRL Domain9 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM9_M6_RD_AUT_CTRL Domain9 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM9_M5_WT_AUT_CTRL Domain9 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM9_M5_RD_AUT_CTRL Domain9 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM9_M4_WT_AUT_CTRL Domain9 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM9_M4_RD_AUT_CTRL Domain9 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM9_M3_WT_AUT_CTRL Domain9 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM9_M3_RD_AUT_CTRL Domain9 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM9_M2_WT_AUT_CTRL Domain9 write permission control for master2 0: The write-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The write-operation is prohibited
20	R/W	0x0	DM9_M2_RD_AUT_CTRL Domain9 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM9_M1_WT_AUT_CTRL Domain9 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM9_M1_RD_AUT_CTRL Domain9 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM9_M0_WT_AUT_CTRL Domain9 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM9_M0_RD_AUT_CTRL Domain9 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM8_M6_WT_AUT_CTRL Domain8 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM8_M6_RD_AUT_CTRL Domain8 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	DM8_M5_WT_AUT_CTRL Domain8 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM8_M5_RD_AUT_CTRL Domain8 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM8_M4_WT_AUT_CTRL Domain8 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM8_M4_RD_AUT_CTRL Domain8 read permission control for master4 0: The read-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The read-operation is prohibited
7	R/W	0x0	DM8_M3_WT_AUT_CTRL Domain8 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM8_M3_RD_AUT_CTRL Domain8 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM8_M2_WT_AUT_CTRL Domain8 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM8_M2_RD_AUT_CTRL Domain8 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM8_M1_WT_AUT_CTRL Domain8 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM8_M1_RD_AUT_CTRL Domain8 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM8_M0_WT_AUT_CTRL Domain8 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM8_M0_RD_AUT_CTRL Domain8 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.25. 0x00C4 IOMMU Domain Authority Control Register 5 (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM11_M6_WT_AUT_CTRL Domain11 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM11_M6_RD_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain11 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM11_M5_WT_AUT_CTRL Domain11 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM11_M5_RD_AUT_CTRL Domain11 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM11_M4_WT_AUT_CTRL Domain11 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM11_M4_RD_AUT_CTRL Domain11 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM11_M3_WT_AUT_CTRL Domain11 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM11_M3_RD_AUT_CTRL Domain11 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM11_M2_WT_AUT_CTRL Domain11 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
20	R/W	0x0	DM11_M2_RD_AUT_CTRL Domain11 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM11_M1_WT_AUT_CTRL Domain11 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM11_M1_RD_AUT_CTRL Domain11 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM11_M0_WT_AUT_CTRL Domain11 write permission control for master0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM11_M0_RD_AUT_CTRL Domain11 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM10_M6_WT_AUT_CTRL Domain10 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM10_M6_RD_AUT_CTRL Domain10 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	DM10_M5_WT_AUT_CTRL Domain10 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM10_M5_RD_AUT_CTRL Domain10 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM10_M4_WT_AUT_CTRL Domain10 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM10_M4_RD_AUT_CTRL Domain10 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	DM10_M3_WT_AUT_CTRL Domain10 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM10_M3_RD_AUT_CTRL Domain10 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM10_M2_WT_AUT_CTRL Domain10 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM10_M2_RD_AUT_CTRL Domain10 read permission control for master2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM10_M1_WT_AUT_CTRL Domain10 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM10_M1_RD_AUT_CTRL Domain10 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM10_M0_WT_AUT_CTRL Domain10 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM10_M0_RD_AUT_CTRL Domain10 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.26. 0x00C8 IOMMU Domain Authority Control Register 6 (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM13_M6_WT_AUT_CTRL Domain13 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM13_M6_RD_AUT_CTRL Domain13 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM13_M5_WT_AUT_CTRL Domain13 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM13_M5_RD_AUT_CTRL Domain13 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM13_M4_WT_AUT_CTRL Domain13 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

24	R/W	0x0	DM13_M4_RD_AUT_CTRL Domain13 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM13_M3_WT_AUT_CTRL Domain13 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM13_M3_RD_AUT_CTRL Domain13 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM13_M2_WT_AUT_CTRL Domain13 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
20	R/W	0x0	DM13_M2_RD_AUT_CTRL Domain13 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM13_M1_WT_AUT_CTRL Domain13 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM13_M1_RD_AUT_CTRL Domain13 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM13_M0_WT_AUT_CTRL Domain13 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM13_M0_RD_AUT_CTRL Domain13 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM12_M6_WT_AUT_CTRL Domain12 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM12_M6_RD_AUT_CTRL Domain12 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	R/W	0x0	DM12_M5_WT_AUT_CTRL Domain12 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM12_M5_RD_AUT_CTRL Domain12 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM12_M4_WT_AUT_CTRL Domain12 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM12_M4_RD_AUT_CTRL Domain12 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	DM12_M3_WT_AUT_CTRL Domain12 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM12_M3_RD_AUT_CTRL Domain12 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM12_M2_WT_AUT_CTRL Domain12 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM12_M2_RD_AUT_CTRL Domain12 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM12_M1_WT_AUT_CTRL Domain12 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM12_M1_RD_AUT_CTRL Domain12 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM12_M0_WT_AUT_CTRL Domain12 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM12_M0_RD_AUT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Domain12 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.27. 0x00CC IOMMU Domain Authority Control Register 7 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM15_M6_WT_AUT_CTRL Domain15 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
28	R/W	0x0	DM15_M6_RD_AUT_CTRL Domain15 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
27	R/W	0x0	DM15_M5_WT_AUT_CTRL Domain15 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
26	R/W	0x0	DM15_M5_RD_AUT_CTRL Domain15 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
25	R/W	0x0	DM15_M4_WT_AUT_CTRL Domain15 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
24	R/W	0x0	DM15_M4_RD_AUT_CTRL Domain15 read permission control for master4 0: The read-operation is permitted 1: The read-operation is prohibited
23	R/W	0x0	DM15_M3_WT_AUT_CTRL Domain15 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
22	R/W	0x0	DM15_M3_RD_AUT_CTRL Domain15 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
21	R/W	0x0	DM15_M2_WT_AUT_CTRL Domain15 write permission control for master2 0: The write-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The write-operation is prohibited
20	R/W	0x0	DM15_M2_RD_AUT_CTRL Domain15 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited
15:14	/	/	/
13	R/W	0x0	DM14_M6_WT_AUT_CTRL Domain14 write permission control for master6 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	DM14_M6_RD_AUT_CTRL Domain14 read permission control for master6 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write permission control for master5 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read permission control for master5 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	DM14_M4_WT_AUT_CTRL Domain14 write permission control for master4 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read permission control for master4 0: The read-operation is permitted

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: The read-operation is prohibited
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write permission control for master3 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read permission control for master3 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write permission control for master2 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read permission control for master2 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write permission control for master1 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read permission control for master1 0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	DM14_M0_WT_AUT_CTRL Domain14 write permission control for master0 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	DM14_M0_RD_AUT_CTRL Domain14 read permission control for master0 0: The read-operation is permitted 1: The read-operation is prohibited

3.12.6.28. 0x00D0 IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read permission overwrite enable 0: Disable 1: Enable
30:14	/	/	/
13	R/W	0x0	M6_WT_AUT_OVWT_CTRL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Master6 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
12	R/W	0x0	M6_RD_AUT_OVWT_CTRL Master6 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read permission overwrite control

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: The read-operation is permitted 1: The read-operation is prohibited
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write permission overwrite control 0: The write-operation is permitted 1: The write-operation is prohibited
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read permission overwrite control 0: The read-operation is permitted 1: The read-operation is prohibited

NOTE

Setting the REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All the property of Level2 are covered by the property defined in REG_ARD_OVWT. Allow read and write for all by default.

3.12.6.29. 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

NOTE

Invalid page table and permission error can not make one device or multi-devices in system work normally.

Permission error usually happens in MicroTLB. The error generates interrupt, and waits for processing through software.

Invalid page table usually happens in MacroTLB. The error can not influence the access of other devices. So the error page table needs go back the way it comes, but the error should not be written in each level TLB.

3.12.6.30. 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			**Register Name: IOMMU_INT_CLR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

3.12.6.31. 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

3.12.6.32. 0x0110 IOMMU Interrupt Error Address Register 0 (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR0 Virtual address that caused Micro TLB0 to interrupt

3.12.6.33. 0x0114 IOMMU Interrupt Error Address Register 1 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR1 Virtual address that caused Micro TLB1 to interrupt

3.12.6.34. 0x0118 IOMMU Interrupt Error Address Register 2 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR2 Virtual address that caused Micro TLB2 to interrupt

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.35. 0x011C IOMMU Interrupt Error Address Register 3 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR3 Virtual address that caused Micro TLB3 to interrupt

3.12.6.36. 0x0120 IOMMU Interrupt Error Address Register 4 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR4 Virtual address that caused Micro TLB4 to interrupt

3.12.6.37. 0x0124 IOMMU Interrupt Error Address Register 5 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR5 Virtual address that caused Micro TLB5 to interrupt

3.12.6.38. 0x0128 IOMMU Interrupt Error Address Register 6 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR6 Virtual address that caused Micro TLB6 to interrupt

3.12.6.39. 0x0130 IOMMU Interrupt Error Address Register 7 (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR7 Virtual address that caused L1 page table to interrupt

3.12.6.40. 0x0134 IOMMU Interrupt Error Address Register 8 (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R	0x0	INT_ERR_ADDR8 Virtual address that caused L2 page table to interrupt

3.12.6.41. 0x0150 IOMMU Interrupt Error Data Register 0 (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA0 Corresponding page table of virtual address that caused Micro TLB0 to interrupt

3.12.6.42. 0x0154 IOMMU Interrupt Error Data Register 1 (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA1 Corresponding page table of virtual address that caused Micro TLB1 to interrupt

3.12.6.43. 0x0158 IOMMU Interrupt Error Data Register 2 (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA2 Corresponding page table of virtual address that caused Micro TLB2 to interrupt

3.12.6.44. 0x015C IOMMU Interrupt Error Data Register 3 (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA3 Corresponding page table of virtual address that caused Micro TLB3 to interrupt

3.12.6.45. 0x0160 IOMMU Interrupt Error Data Register 4 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R	0x0	INT_ERR_DATA4 Corresponding page table of virtual address that caused Micro TLB4 to interrupt

3.12.6.46. 0x0164 IOMMU Interrupt Error Data Register 5 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA5 Corresponding page table of virtual address that caused Micro TLB5 to interrupt

3.12.6.47. 0x0168 IOMMU Interrupt Error Data Register 6 (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA6 Corresponding page table of virtual address that caused Micro TLB6 to interrupt

3.12.6.48. 0x0170 IOMMU Interrupt Error Data Register 7 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA7 Corresponding page table of virtual address that caused L1 page table to interrupt

3.12.6.49. 0x0174 IOMMU Interrupt Error Data Register 8 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA8 Corresponding page table of virtual address that caused L2 page table to interrupt

3.12.6.50. 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180	Register Name: IOMMU_L1PG_INT_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT Debug mode address switch causes L1 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT Master6 address switch causes L1 page table to occur interrupt.
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

3.12.6.51. 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DBG_MODE_L2PG_INT Debug mode address switch causes L2 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT Master6 address switch causes L2 page table to occur interrupt.
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.52. 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA Virtual address of read/write

3.12.6.53. 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA_DATA Data of read/write virtual address

3.12.6.54. 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MODE_SEL 0: Prefetch 1: Debug Mode It is used to chose prefetch mode or Debug mode.
31:9	/	/	/
8	R/W	0x0	VA_CONFIG 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation completes 1: Start After the operation completes, the bit can clear to 0 automatically.

Read operation process:

a) Write IOMMU_VA_REG[31:0];

b) Write IOMMU_VA_CONFIG_REG[8] to 0;

c) Write IOMMU_VA_CONFIG_REG[0] to 1 to start read-process;

d) Query IOMMU_VA_CONFIG_REG[0] until it is 0;

e) Read IOMMU_VA_DATA_REG[31:0];

Write operation process:

a) Write IOMMU_VA _REG[31:0];

b) Write IOMMU_VA_DATA_REG[31:0];

c) Write IOMMU_VA_CONFIG_REG[8] to 1;

d) Write IOMMU_VA_CONFIG_REG[0] to 1 to start write-process;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

e) Query IOMMU_VA_CONFIG_REG[0] until it is 0;

3.12.6.55. 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disable statistical function 1: Enable statistical function

3.12.6.56. 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation completes 1: Clear counter data After the operation completes, the bit can clear to 0 automatically.

3.12.6.57. 0x0230 IOMMU PMU Access Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW0 Record total number of Micro TLB0 access , lower 32-bit register

3.12.6.58. 0x0234 IOMMU PMU Access High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access , higher 11-bit register

3.12.6.59. 0x0238 IOMMU PMU Hit Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0238	Register Name: IOMMU_PMU_HIT_LOW_REG0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0 Record total number of Micro TLB0 hit , lower 32-bit register

3.12.6.60. 0x023C IOMMU PMU Hit High Register 0 (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit , higher 11-bit register

3.12.6.61. 0x0240 IOMMU PMU Access Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access , lower 32-bit register

3.12.6.62. 0x0244 IOMMU PMU Access High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access , higher 11-bit register

3.12.6.63. 0x0248 IOMMU PMU Hit Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit , lower 32-bit register

3.12.6.64. 0x024C IOMMU PMU Hit High Register 1 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit , higher 11-bit register

3.12.6.65. 0x0250 IOMMU PMU Access Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access , lower 32-bit register

3.12.6.66. 0x0254 IOMMU PMU Access High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access , higher 11-bit register

3.12.6.67. 0x0258 IOMMU PMU Hit Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit , lower 32-bit register

3.12.6.68. 0x025C IOMMU PMU Hit High Register 2 (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit , higher 11-bit register

3.12.6.69. 0x0260 IOMMU PMU Access Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.70. 0x0264 IOMMU PMU Access High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access , higher 11-bit register

3.12.6.71. 0x0268 IOMMU PMU Hit Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW3 Record total number of Micro TLB3 hit, lower 32-bit register

3.12.6.72. 0x026C IOMMU PMU Hit High Register 3 (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit , higher 11-bit register

3.12.6.73. 0x0270 IOMMU PMU Access Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register

3.12.6.74. 0x0274 IOMMU PMU Access High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.75. 0x0278 IOMMU PMU Hit Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit, lower 32-bit register

3.12.6.76. 0x027C IOMMU PMU Hit High Register 4 (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit, higher 11-bit register

3.12.6.77. 0x0280 IOMMU PMU Access Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register

3.12.6.78. 0x0284 IOMMU PMU Access High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register

3.12.6.79. 0x0288 IOMMU PMU Hit Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit, lower 32-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.80. 0x028C IOMMU PMU Hit High Register 5 (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit, higher 11-bit register

3.12.6.81. 0x0290 IOMMU PMU Access Low Register6 (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register

3.12.6.82. 0x0294 IOMMU PMU Access High Register 6 (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register

3.12.6.83. 0x0298 IOMMU PMU Hit Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit, lower 32-bit register

3.12.6.84. 0x029C IOMMU PMU Hit High Register 6 (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit, higher 11-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.85. 0x02D0 IOMMU PMU Access Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of Micro TLB7 access, lower 32-bit register

3.12.6.86. 0x02D4 IOMMU PMU Access High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of Micro TLB7 access, higher 11-bit register

3.12.6.87. 0x02D8 IOMMU PMU Hit Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW7 Record total number of Micro TLB7 hit, lower 32-bit register

3.12.6.88. 0x02DC IOMMU PMU Hit High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of Micro TLB7 hit, higher 11-bit register

3.12.6.89. 0x02E0 IOMMU PMU Access Low Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW8 Record total number of PTW Cache access, lower 32-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.90. 0x02E4 IOMMU PMU Access High Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record total number of PTW Cache access, higher 11-bit register

3.12.6.91. 0x02E8 IOMMU PMU Hit Low Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW8 Record total number of PTW Cache hit, lower 32-bit register

3.12.6.92. 0x02EC IOMMU PMU Hit High Register 8 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record total number of PTW Cache hit, higher 11-bit register

3.12.6.93. 0x0300 IOMMU Total Latency Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register

3.12.6.94. 0x0304 IOMMU Total Latency High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.95. 0x0308 IOMMU Max Latency Register 0 (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML0 Record the max latency of Master0.

3.12.6.96. 0x0310 IOMMU Total Latency Low Register 1(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register

3.12.6.97. 0x0314 IOMMU Total Latency High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register

3.12.6.98. 0x0318 IOMMU Max Latency Register 1 (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML1 Record the max latency of Master1.

3.12.6.99. 0x0320 IOMMU Total Latency Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register

3.12.6.100. 0x0324 IOMMU Total Latency High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0324	Register Name: IOMMU_PMU_TL_HIGH_REG2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register

3.12.6.101. 0x0328 IOMMU Max Latency Register 2 (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML2 Record the max latency of Master2.

3.12.6.102. 0x0330 IOMMU Total Latency Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW3 Record total latency of Master3, lower 32-bit register

3.12.6.103. 0x0334 IOMMU Total Latency High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register

3.12.6.104. 0x0338 IOMMU Max Latency Register 3 (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML3 Record the max latency of Master3.

3.12.6.105. 0x0340 IOMMU Total Latency Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW4

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Record total latency of Master4, lower 32-bit register

3.12.6.106. 0x0344 IOMMU Total Latency High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register

3.12.6.107. 0x0348 IOMMU Max Latency Register 4 (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML4 Record the max latency of Master4.

3.12.6.108. 0x0350 IOMMU Total Latency Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW5 Record total latency of Master5, lower 32-bit register

3.12.6.109. 0x0354 IOMMU Total Latency High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register

3.12.6.110. 0x0358 IOMMU Max Latency Register 5 (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML5 Record the max latency of Master5.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.12.6.111. 0x0360 IOMMU Total Latency Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW6 Record total latency of Master6, lower 32-bit register

3.12.6.112. 0x0364 IOMMU Total Latency High Register 6 (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record total latency of Master6, higher 18-bit register

3.12.6.113. 0x0368 IOMMU Max Latency Register 6 (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML6 Record the max latency of Master6.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13. RTC

3.13.1. Overview

The RTC(Real Time Clock) is used to implement time counter and timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and genetates interrupt and wakeup the external devices
- Supports 32.768 kHz calibration function divided by RC16M, and power-off wakeup calibration
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing power-off information

3.13.2. Clock Tree Diagram

The clock tree diagram of RTC is shown in Figure 3-33.

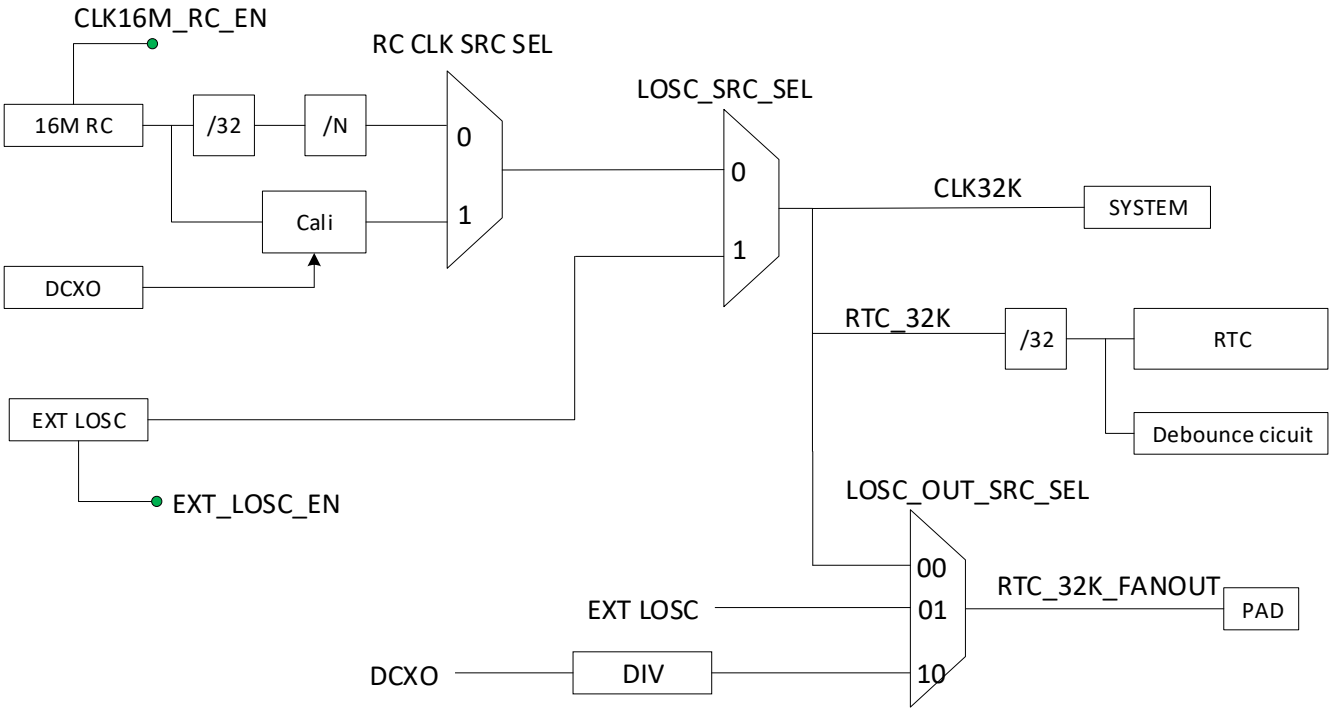


Figure 3- 33. RTC Clock Tree

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

RTC clock tree can be selected by corresponding switch, there are 3 options: RC16M, LOSC from crystal, 32K clock after calibrated.
Clock source: 32.768 kHz low-frequency crystal, the division clock of 16 MHz RC oscillator(uncalibrated), and the division clock after 16 MHz RC calibrated.
Output clock: CLK32K and RTC_32K_FANOUT.

3.13.3. Operations and Functional Descriptions

3.13.3.1. External Signals

Table 3- 12. RTC External Signals

Signal	Description
X32KIN	32.768 kHz oscillator input
X32KOUT	32.768 kHz oscillator output
32KFOUT	32.768 kHz clock fanout Provides low frequency clock for external devices
NMI	Alarm wakeup generates low level into NMI
RTC_VIO	RTC low voltage, generated via internal LDO
VCC_RTC	RTC high voltage, generated via external power

3.13.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC_RTC. When VCC_RTC powers on, the reset signal resets the RTC module; after VCC_RTC reaches stable, the reset signal always holds high level. Watchdog Reset cannot reset RTC.
The RTC module accesses its register by AHBS1.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.3.3. Typical Application

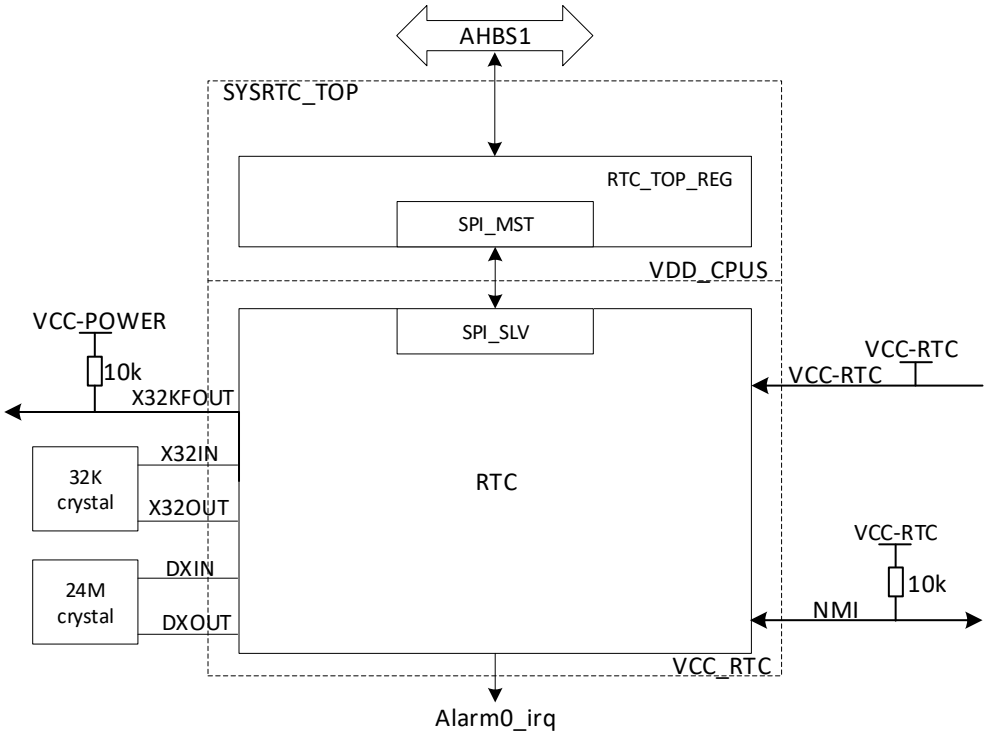


Figure 3- 34. RTC Application Diagram

The external low-frequency oscillator must be 32.768 kHz. If the external peripheral needs low frequency crystal, which can be provided by X32KFOUT.
AP-NMI# and alarm0 in common generate low level signal.

3.13.3.4. Function Implementation

3.13.3.4.1. Clock Sources

The RTC has 2 clock sources: internal RC, external low frequency crystal.
The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency crystal to provide much accuracy clock. The clock accurate of the RTC is related to the accurate of the external low frequency crystal. Usually select 32.768 kHz crystal with ±20 ppm frequency tolerance.

When using internal RC, the clock of RTC can be changed by changing division ratio. When using external clock, the clock cannot be changed.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.3.4.2. Real Time Clock

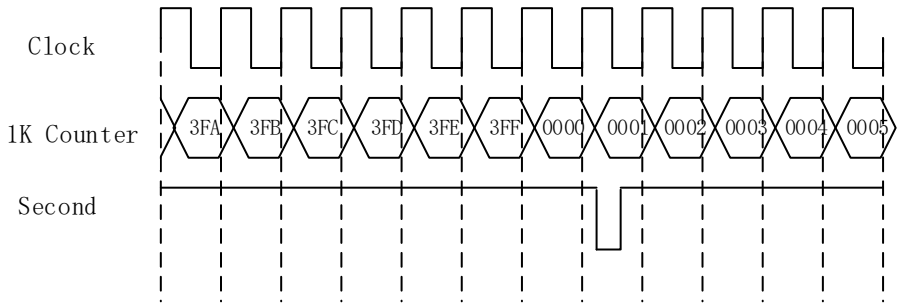


Figure 3- 35. RTC Counter

The 1K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1K counter starts to count again from 0, and the second counter adds 1. The step structure of 1KHz counter is as follows.

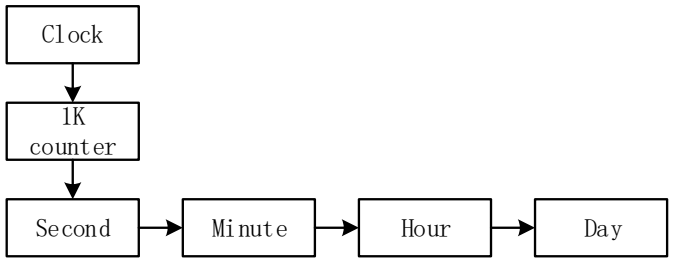


Figure 3- 36. RTC 1KHz Counter Step Structure

According to above implementation, the changing range of each counter is as follows.

Table 3- 13. RTC Counter Changing Range

Counter	Range
Second	0~59
Minute	0~59
Hour	0~23
Day	0~65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.3.4.3. Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.
The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

3.13.3.4.4. Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.13.3.4.5. RTC_VIO

The RTC module has a LDO, the input source of the LDO is VCC_RTC, the output of the LDO is RTC_VIO, the value of RTC_VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

3.13.3.4.6. RC Calibration

The basic circuit of RC calibration is shown in Figure 3-35. Whether to output the calibrated RC clock can be selected by the RC_Cali_SEL control bit, the calibration principle is as follows.

As shown in Figure 3-36, with OSC24M(24 MHz) as the reference clock, calculate the counter number M of RC clock within 1 ms/16 ms/128 ms to obtain the accurate frequency of internal RC. By dividing the accurate frequency by 32.768 kHz, the frequency divider(K) from RC clock to 32.768 kHz is obtained. Lastly, RC16M is divided into 32.768 kHz frequency by the frequency divider(K).

NOTE

The calibration principle is output 32.768 kHz, not input 16 MHz.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

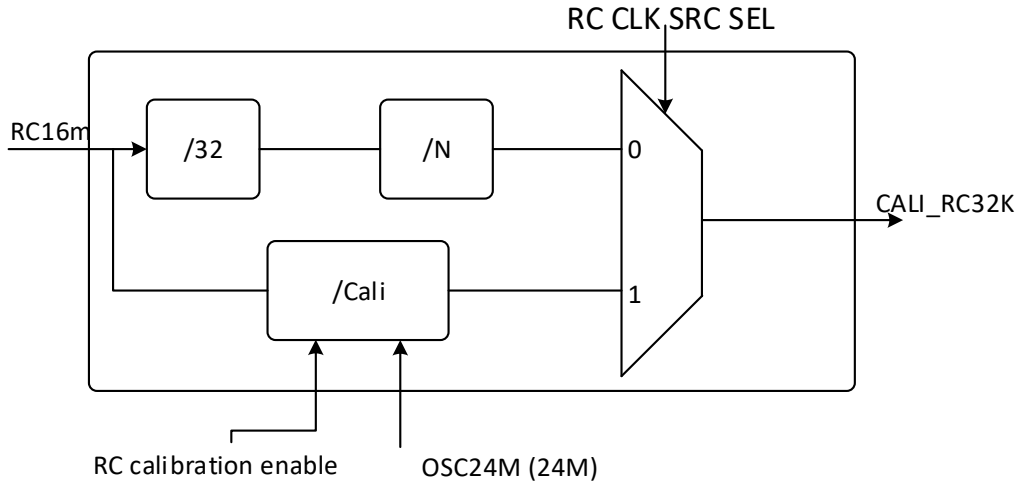


Figure 3- 37. Calibration Circuit

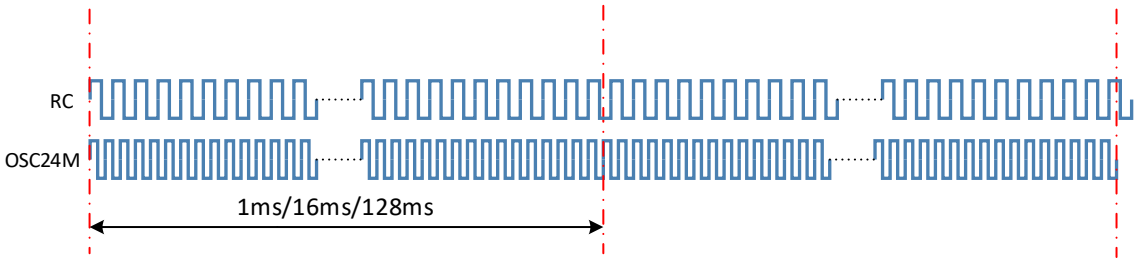


Figure 3- 38. RC Waveform

3.13.3.4.7. DCXO Timed Wakeup

The logic of DCXO timed wakeup circuit is relatively simple, including two controls: timed wakeup hardware automatic enable and timed wakeup time length (software configuration). The timed wakeup means that DCXO circuit is required to wakeup the output clock once every second(1s~60s, usually the ambient temperature changes little in a few seconds) for 32K calibration in the super standby or shutdown scenario,after calibration, DCXO circuit is closed, the closed time is timed wakeup time length(software configuration).The time of DCXO circuit from wakeup starting to stable output is 3 ms~4 ms. Although the timed wakeup function is closed, DCXO circuit always had worked. The process of timed wakeup is shown in Figure 3-39.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

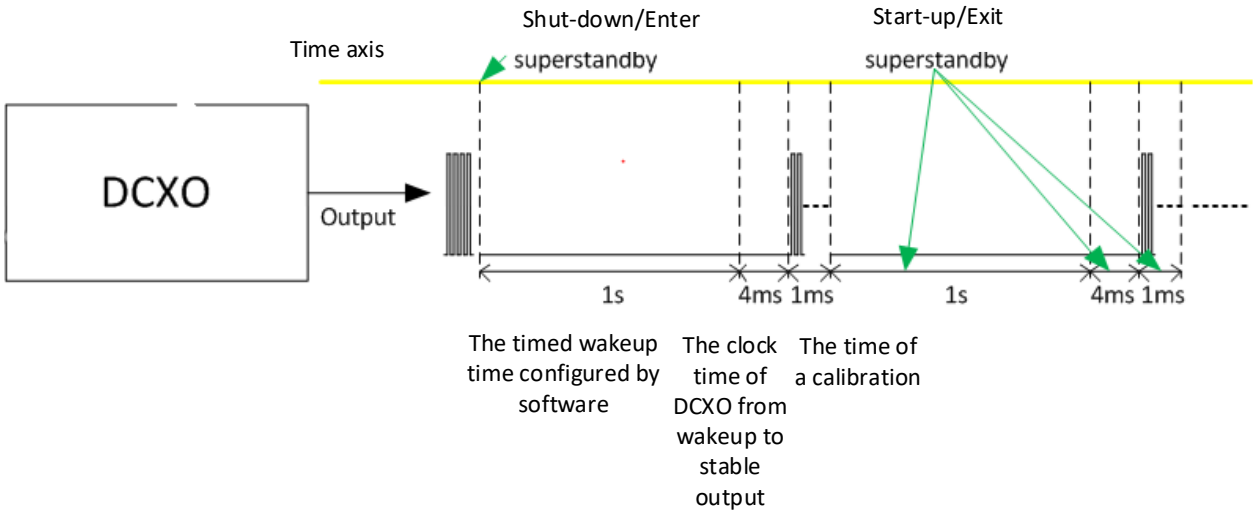


Figure 3- 39. DCXO Timed Wakeup Waveform

The time of a calibration in shutdown or super standby: the timed wakeup time configured by software + the clock time of DCXO from wakeup to stable output + the time of a calibration. The timed wakeup time configured by the software in the figure is 1 s, and can be configured by software in application. It is the theoretical maximum value for DCXO from wakeup to stable output clock in 4 ms , the specific value is subject to IC measured results. In the any time of these three periods, the startup or exit of the super standby action will not cause DCXO abnormal.

The enable signal of DCXO and the enable signal of timed wakeup DCXO is “OR”logic, and they do not contradict each other.

The interval between continuous DCXO enable operation and disable operation is at least greater than 4 us.

3.13.3.5. Operating Mode

3.13.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.

(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external crystal could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.

(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_DAY_REG** and **RTC_HH_MM_SS_REG**.
(2) After configured time, read the bit[8:7] of **LOSC_CTRL_REG** to ensure that configuration is completed.
(3) After update time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.
After configured time at each time, you need ensure the bit[8:7] of LOSC_CTRL_REG is 0 before the next setting is performed.

3.13.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter comparator, write the count-down day, hour, minute, second number to **ALARM0_DAY_REG** and **ALARM0_HH_MM_SS_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time by **ALARM0_DAY_REG** and **ALARM0_HH_MM_SS_REG.** When the setting time reaches, **ALARM0_IRQ_STA_REG** is set to 1 to generate interrupt.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the interrupt process.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, the software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.13.3.5.4. Fanout

Set the bit0 of **LOSC_OUT_GATING_REG** to 1, and ensure external pull-up resistor, voltage, clock source are normal, then 32.768kHz square wave can be output.

3.13.3.5.5. DRAM Data Encrypt

If using DRAM data encrypt, the DRAM data read by CPU is the encrypted data. The steps are as follows.
Before write/read **CRY_KEY_REG** and **CRY_EN_REG**, the bit[15:0] of **CRY_CONFIG_REG** should be written to 0x1689.

CAUTION

Before read/write each time, the step is needed to be performed, or else the register operation is no successful.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.3.5.6. RC Calibration Usage Scenario

- Power-on: Select non-accurate 32K divided by internal RC.
- Normal scenario: Select external accurate 32K, or external calibrated 32K.
- Standby or power-off scenario: Select external accurate 32K, or external calibrated 32K.

3.13.4. Programming Guidelines

3.13.4.1. RTC Clock Sources Setting

Configure **LOSC_CTRL_REG** to set RTC clock source.
For example: select external 32K clock source as RTC clock.

```
writel(0x16aa4000,LOSC_CTRL);       //write key field
writel(0x16aa4001,LOSC_CTRL);       //select external 32K clock
```

3.13.4.2. Real Time Clock

For example: set time- 21', 07:08:09

```
RTC_DAY_REG = 0x00000015;
RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)
Read (RTC_DAY_REG);
Read (RTC_HH_MM_SS_REG);
```

3.13.4.3. Alarm 0

```
irq_request(GIC_SRC_R_Alarm0, Alm0_handler);
irq_enable(GIC_SRC_R_Alarm0);
writel(1, ALARM0_DAY_SET_REG);
writel(1, RTC_HH_MM_SS_REG);          //Set 1 second corresponding to normal mode;
writel(1, ALM0_EN);
writel(1, ALM_CONFIG);                //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1, ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.13.5. Register List

Module Name	Base Address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

RTC	0x07000000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
LOSC_OUT_GATING_REG	0x0060	LOSC Output Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~7)
FBOOT_INFO_REG0	0x0120	Fast Boot Information Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Information Register1
DCXO_CTRL_REG	0x0160	DCXO Control Register
CALI_CTRL_REG	0x0164	Calibration Control Register
RTC_VIO_REG	0x0190	RTC_VIO Regulate Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

3.13.6. Register Description

CAUTION

The register configuration of RTC is AHB bus, it only can support word operation, not byte and half word operation.

3.13.6.1. 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit0 and bit1 can be

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			written with the new value.
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K clk source sel enable 0: Disable, when losc lost, 32k clk source will not change to RC 1: Enable, when losc lost, 32k clk source will change to RC(LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/
8	R/W	0x0	RTC_HHMMSS_ACCE RTC HH-MM-SS access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one second.
7	R/W	0x0	RTC_DAY_ACCE RTC DAY access After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32.768 kHz Crystal Enable 0: Disable 1: Enable
3:2	R/W	0x0	EXT_LOSC_GSM External 32.768 kHz Crystal GSM 00: Low 01: / 10: / 11: High When GSM is changed, 32K oscillation circuit will arise transient instability. If the autos witch function(bit 15) is enabled, 32K changes to RC16M with certain probability. GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If modifying GSM is necessary, firstly disable the auto switch function(bit 15), with a delay of 50us, then change GSM, 32K clock source is changed to external clock.
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescalar

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Register. 0: Low Frequency Clock from 16M RC 1: External 32.768kHz OSC

NOTE

If the bit[8:7] of LOSC_CTRL_REG is set, the RTC HH-MM-SS, DD and ALARM DD-HH-MM-SS register cannot be written.

3.13.6.2. 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when AUTO SWITCH function is enabled. 0: External 32.768 kHz OSC work normally 1: External 32.768 kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect 1: Auto switch pending, it means LOSC_SRC_SEL is changed from 1 to 0. Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar Register. 0: Low Frequency Clock from 16M RC 1: External 32.768 kHz OSC

3.13.6.3. 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N. The clock output = Internal RC/32/N. 00000: 1 00001: 2 00002: 3 ..... 11111: 32

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.6.4. 0x000C Internal OSC Clock Auto Calibration Register (Default Value: 0x01E8_0000)

Offset:0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	RO	0x1e8	32k calibration integer divider factor
21:5	RO	0x0	32k calibration decimal divider factor
4	R/W	0x0	Calibration function Clk16M_RC_enable 0: Auto gating 1: Soft bypass
3:2	R/W	0x0	RC Calibration Precise Selection 00: 1ms calibration precise 01: 16ms calibration precise 10: 128ms calibration precise
1	R/W	0x0	RC calibration enable 0: Close Calibration circuit 1: Open Calibration circuit
0	R/W	0x0	RC CLK SRC SEL Select the RTC 32k clock source from normal RC or Calibrated RC 0: Normal RC 1: Calibrated RC

3.13.6.5. 0x0010 RTC DAY Register

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	UDF	DAY Day Range from 1~65535.

NOTE

Ensure that the bit[7] of LOSC_CTRL_REG is 0 before updating RTC_DAY_REG.

3.13.6.6. 0x0014 RTC HH-MM-SS Register

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND Range from 0~59

NOTE

Ensure that the bit[8] of LOSC_CTRL_REG is 0 before updating RTC_HH_MM_SS_REG.

3.13.6.7. 0x0020 Alarm 0 Day Setting Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_COUNTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on Day.

3.13.6.8. 0x0024 Alarm 0 HH-MM-SS Setting Register

Offset:0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	x	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	x	MINUTE Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND Range from 0~59

3.13.6.9. 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable If this bit is set to “1”, the valid bits of Alarm 0 Counter Register will down count to zero, and the alarm pending bit will be set to “1”. 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.13.6.10. 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.13.6.11. 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.13.6.12. 0x0050 Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.13.6.13. 0x0060 LOSC OUT Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: LOSC_OUT_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	OSC24M_32K_DIVIDER_ENABLE 1: enable the OSC24M to 32K divider circuit

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: disable the OSC24M to 32K divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL 00: RTC_32K(select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: OSC24M divided 32K
0	R/W	0x0	32K_FANOUT_GATING Configuration of LOSC output, and no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

3.13.6.14. 0x0100+N*0x0004 General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~7)			Register Name: GP_DATA_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0~7 value can be stored if the RTC-VIO is larger than 0.7V.

3.13.6.15. 0x0120 Fast Boot Information Register0 (Default Value: 0x0000_0000)

Offset:0x0120			Register Name: FBOOT_INFO_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Fast Boot Information, refer to BROM spec.

3.13.6.16. 0x0124 Fast Boot Information Register1 (Default Value: 0x0000_0000)

Offset:0x0124			Register Name: FBOOT_INFO_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Fast Boot Information, refer to BROM spec.

3.13.6.17. 0x0160 DCXO Control Register (Default Value: 0x083F_10F3 or 0x083F_F0FC)

Offset:0x0160			Register Name: DCXO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DCXO_FANOUT_ENB 0: enable DCXO wake up function 1: disable DCXO wake up function

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value Capacity cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external clk input mode 1: For normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20pF.
3:2	/	/	/
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN 1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

3.13.6.18. 0x0164 Calibration Control Register (Default Value: 0x0000_0043)

Offset:0x0164			Register Name: CALI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	WAKEUP_DCXO_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Wake up DCXO circuit enable.
30:17	/	/	/
16	R/W	0x0	WAKEUP_READY_SLEEP_MODE Calibration wake up ready sleep mode, it must be set before the WAKEUP_DCXO_EN(bit31) is set to 1. 0: Disable 1: Enable
15:12	R/W	0x0	TIMER FOR READY SLEEP Total timer for ready sleep 0000: 15s 0001: 30s 0010: 45s 0011: 60s 0100: 90s 0101: 120s 0110: 150s Others: /
11:8	R/W	0x0	WAKEUP_CNT FOR READY SLEEP Wake up counter for ready sleep 0000: 250ms 0001: 500ms 0010: 750ms 0011: 1s 0100: 1.25s 0101: 1.5s 0110: 1.75s 0111: 2s 1000: 2.25s 1001: 2.5s 1010: 2.75s 1011: 3s 1100: 3.25s 1101: 3.5s 1110: 3.75s 1111: 4s
7:4	R/W	0x4	WAKEUP_CNT FOR SLEEP Wake up counter for sleep 0000: 250ms 0001: 500ms 0010: 1s 0011: 10s 0100: 60s 0101: 120s 0110: 180s 0111: 240s

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1000: 300s 1001: 360s 1010: 420s 1011: 480s 1100: 540s 1101: 600s 1110: 1200s 1111: 1800s
3:0	R/W	0x3	WAIT DCXO SEL Select for DCXO active after DCXO enable 0000: 1ms 0001: 2ms 0010: 3ms 0011: 4ms ... 1111: 16ms

3.13.6.19. 0x0190 RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			**Register Name:RTC_VIO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	V_SEL 0: resistance divider 1: band gap
3	/	/	/
2:0	R/W	0x4	RTC_VIO_REGU These bits are useful for regulating the RTC_VIO from 0.6V to 1.3V, and the regulation step is 0.1V. 000: 1.0V 001: 0.6V (the configuration can cause RTC reset) 010: 0.7V 011: 0.8V 100: 0.9V 101: 1.1V 110: 1.2V 111: 1.3V RTC-VIO is provided power for RTC digital part, the default value is 0.9V. After power-on, software sets the field to 0.8V to save power-consumption.

3.13.6.20. 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0	**Register Name: IC_CHARA_REG**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	IC_CHARA Key Field Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

3.13.6.21. 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset:0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EFUSE_1.8V_POWER_SWITCH_CONTROL 1: open power switch 0: close power switch

3.13.6.22. 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0000)

Offset:0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RTC Reg CFG SPI Clock Gating 0: Gating 1: Not Gating Before configurating RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled. **Note: Frequency division and clock gating can not be set at the same time.**
30:5	/	/	/
4:0	R/W	0x9	RTC Reg CFG SPI Clock Divider: M Actual SPI Clock = AHBS1/(M+1), (0~15) The default frequency of AHBS1 is 200MHz, and the default frequency of SPI Clock is 20MHz. **Note: The SPI clock can not exceed 50MHz, or else RTC register may be abnormal.**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.14. Message Box

3.14.1. Overview

The Message Box(MSGBOX) provides interrupt communication mechanism for on-chip processor.

The MSGBOX has the following features:

- Eight message queues
- Each of queues could be configured as transmitter or receiver for user
- FIFO depth is 4 x 32 bits
- The communication parties are CPUS and CPUX
- The communication parties transmit information through channel
- Message reception and queue-not-full notification interrupt mechanism

3.14.2. Block Diagram

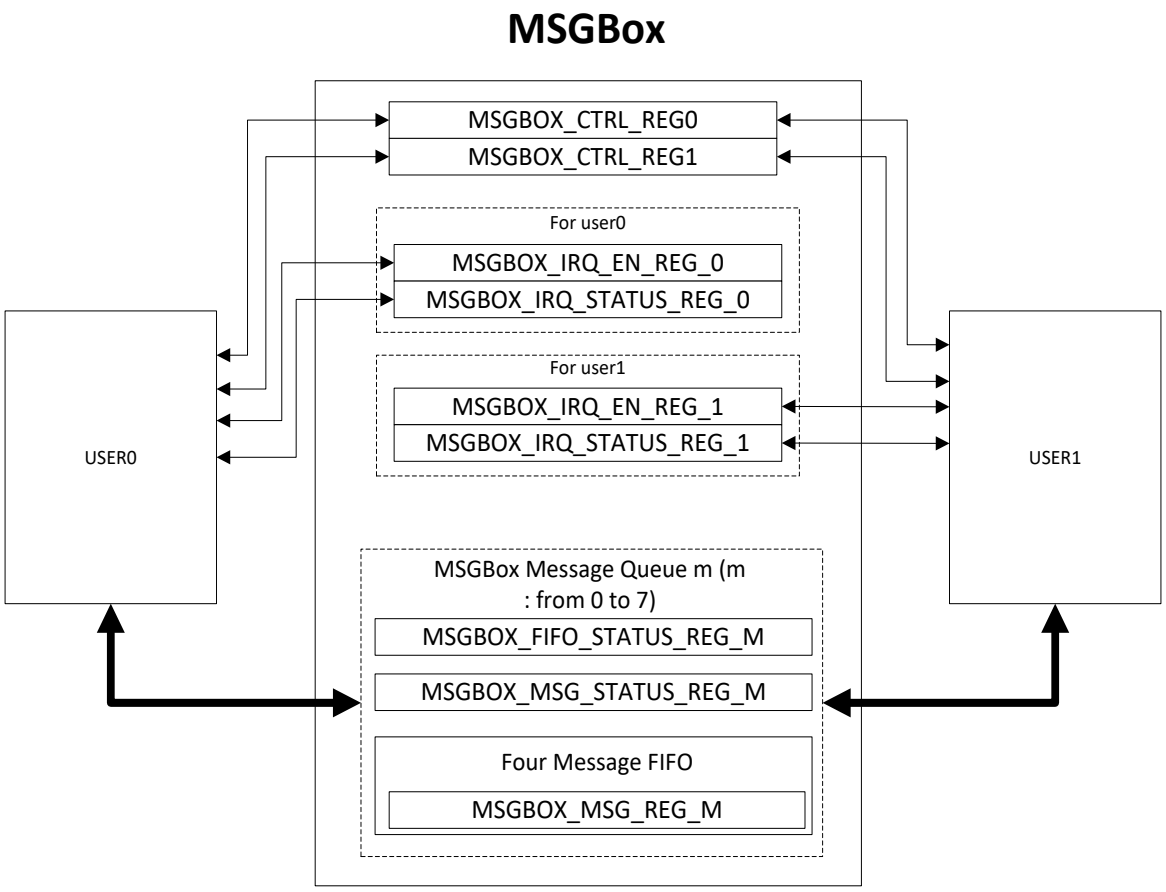


Figure 3- 40. Message Box Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Message Box supports a set of registers for a processor to establish an interconnection channel with the others. The processor determines message queue numbers for interconnection and the used queues to be transmitter or receiver for itself and the interconnectible one. Every queue has a **MSGBox FIFO Status Register** for processor to check out queue FIFO full status and a **MSGBox Message Status Register** for processor to check out message numbers in queue FIFO. Otherwise, every queue has a corresponding IRQ status bit and a corresponding IRQ enable bit, which are used for requesting an interrupt.

3.14.3. Operations and Functional Descriptions

3.14.3.1. Clock and Reset

MSGBOX is on AHB1 bus. To access MSGBOX, perform the following steps about AHB1 bus.
Step1: De-assert MSGBOX reset signal.
Step2: Open MSGBOX gating signal.

3.14.3.2. Typical Application

Two different CPU can build communication by configuring MSGBOX. The communication parties have 8 bidirectional channels. If a party is receiver, then another is transmitter. During communication process, the current status can be judged through interrupt or FIFO status.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

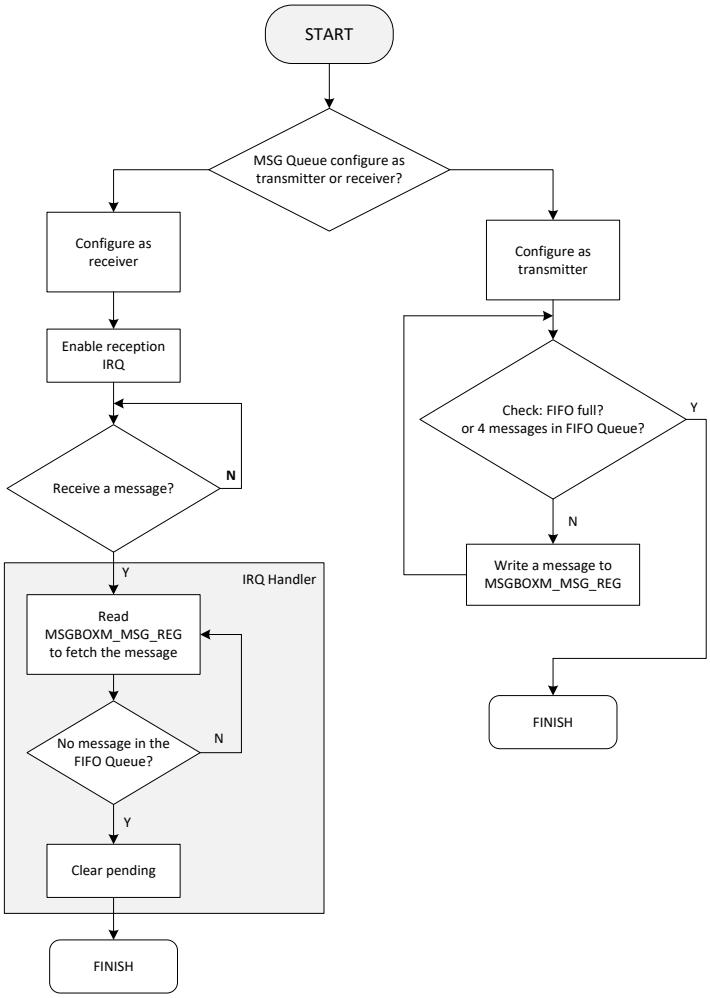


Figure 3- 41. Message Box Typical Application Chart

3.14.3.3. Message Queue Assignment

When a processor needs to transmit or receive a message from the other one, it should configure the Message Queue assignment for the other one and itself. **MSGBOX_CTRL_REG0** and **MSGBOX_CTRL_REG1** hold the eight Message Queues assignment. For an instance, The **RECEPTION_MQ0** bit is set to 0 and the **TRANSMIT_MQ0** bit is set to 1, that means, user1 transmits messages and user0 receives them. Or the **RECEPTION_MQ0** bit and the **TRANSMIT_MQ0** bit are both set to 0, which means user0 transmits messages to itself.

3.14.3.4. Interrupt Request

Message Box provides message reception and queue-not-full notification interrupt mechanism. When a message queue is configured as transmitter for a user, this queue transmit pending bit will always be set to 1 for this user if it is not full. When a message queue is configured as receiver for a user, this queue reception pending bit will be set to 1 for this user only if it receives a new message. For example, message queue0 is configured as a transmitter for user0 and a receiver for user1. If message queue0 is not full always, then TRANSMIT_MQ0_IRQ_PEND bit is set to 1. If TRANSMIT_MQ0_IRQ_EN is set to 1, user0 will request a queue-not-full interrupt. When message queue0 has received

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

a new message, RECEPTION_MQ0_IRQ_PEND would be set to 1 and user1 will request a new message reception interrupt if **RECEPTION_MQ0_IRQ_EN** is set to 1. **MSGBox IRQ Status Register u***(u=0,1)* hold the IRQ status for user0 and user1. **MSGBox IRQ Enable Register u***(u=0,1)* determines whether the user could request the interrupt or not.

3.14.3.5. Transmit and Receive Messages

Every message queue has a couple of private registers for query: **MSGBox Message Status Register**, **MSGBox FIFO Status Register**, and **MSGBox Message Queue Register**.

MSGBox Message Status Register records present message number in the message queue.

MSGBox FIFO Status Register indicates whether the message queue is full obviously.

MSGBox Message Queue Register stores the next to be read message of the message FIFO queue or the message to be written into the queue FIFO. If queue is not full usually ,it indicates that you could write messages into the queue FIFO ,if there is one or more message in the queue FIFO, it indicates that you could read messages from the queue FIFO.

Writing a message into the queue FIFO realizes a transmission and reading a message makes a reception ture. You could transmit messages by writing messages to **MSGBox Message Queue Register** continuously or receive messages by reading **MSGBox Message Queue Register** continuously. The continuous writing or reading operation means it's no need to make a delay between operations.

3.14.3.6. Operating Mode

3.14.3.6.1. Transfer Mode Configuration

- Queue n (n=0~3) transmitter mode: Write 1 to the bit[8*n+4] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7) transmitter mode : Write 1 to the bit[8*(m-4)+4] of **MSGBOX_CTRL_REG1**.
- Queue n (n=0~3) receiver mode: Write 1 to the bit[8*n] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7) receiver mode : Write 1 to the bit[8*(m-4)] of **MSGBOX_CTRL_REG1**.

3.14.3.6.2. Interrupt Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.6.1. Transfer Mode Configuration**.
(2) Interrupt enable bit: Configure the interrupt enable bit of transmitter/receiver through **MSGBOX_IRQ_EN_REG**.
(3) When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data, at this time, to write data to FIFO in interrupt handler ,and clear the pending bit and the enable bit of *Transmitter IRQ*.
(4) When FIFO has new data, an interrupt pending generates to remind the receiver to receive data, at this time, to read data from FIFO in interrupt handler, and clear the pending bit and the enable bit of *Receiver IRQ*.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.14.3.6.3. FIFO Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.6.1. Transfer Mode Configuration**.
(2) When FIFO is not full, the transmitter fills FIFO to 4*32 bits.
(3) When the receiver considers FIFO is full, then the receiver reads FIFO data, and reads **MSGBOXM_MSG_STATUS_REG** to require the current FIFO number.

3.14.3.6.4. Debug

To use MSGBOX in debug mode, performs the following steps:
(1) Write 1 to the bit0 of **MSGBOX_DEBUG_REG**.
(2) The control bit of the corresponding channel is set to 1.

3.14.4. Programming Guidelines

Example: User1 as transmitter of MQ0123 (MQ:Message Queue) and as receiver of MQ4567, User0 as receiver of MQ0123 and as transmitter of MQ4567.

The working process of user1 and user0 is as follows.

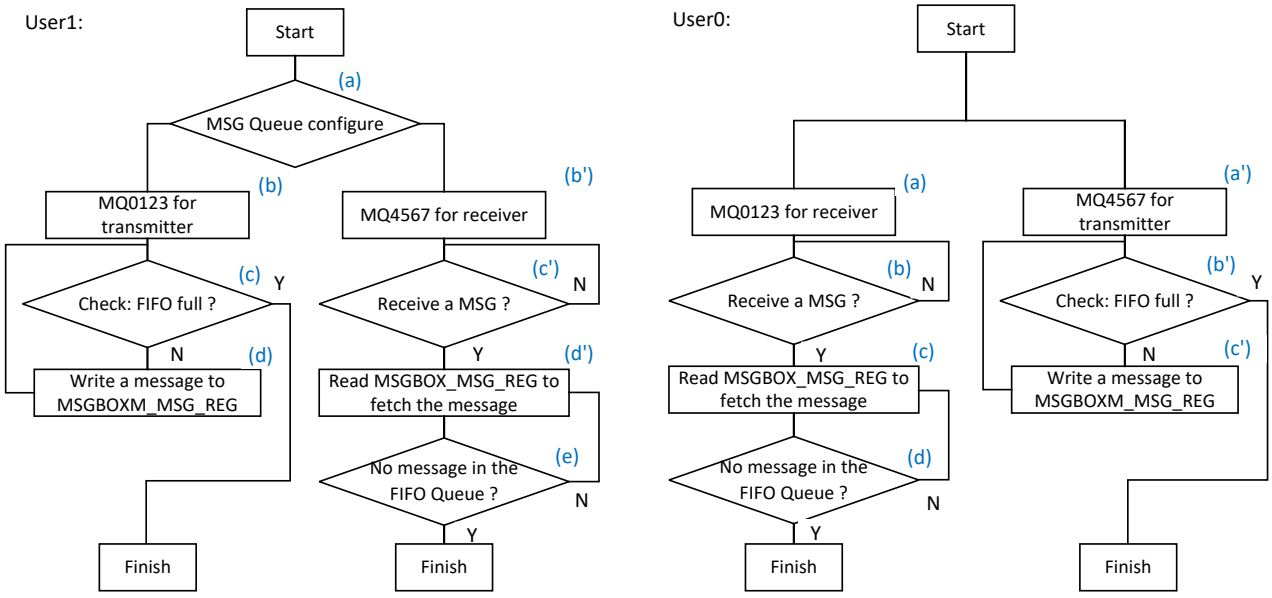


Figure 3- 42. User1 and User0 Working Process

User1:
(a) The user1 is as the transmitter of MQ0123 and as the receiver of MQ4567.
(b) Queue n (n=0~3) transmitter mode: write 1 to the bit[8*n+4] of MSGBOX_CTRL_REG0.
(b') Queue m (m=4~7) receiver mode: write 1 to the bit[8*(m-4)] of MSGBOX_CTRL_REG1.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

(c) Check whether the FIFO is full by the status of MSGBOXM_FIFO_STATUS_REG. If the FIFO is full, the program finish, otherwise, go to step (d).
(c') Check whether to receive a message by the status of MSGBOXM_MSG_STATUS_REG. If you donot receive, then continue to wait, otherwise, go to step (d').
(d) Write a message to MSGBOXM_MSG_REG.
(d') Read MSGBOX_MSG_REG to fetch the message.
(e) If there is no message in FIFO Queue, step up to (d'), otherwise, the program finish.

User0:
(a) The user0 is as the receiver of MQ0123.
(a') The user0 is as the transmitter of MQ4567.
(b) Check whether to receive a message by the status of MSGBOXM_MSG_STATUS_REG. If you donot receive, then continue to wait, otherwise, go to step (c).
(b') Check whether the FIFO is full by the status of MSGBOXM_FIFO_STATUS_REG. If the FIFO is full, the program finish, otherwise, step up to (c').
(c) Read MSGB OX_MSG_REG to fetch the message.
(c') Write a message to MSGBOXM_MSG_REG.
(d) If there is no message in FIFO Queue, go to step (c), otherwise, the program finish.

3.14.5. Register List

Module Name	Base Address
MSGBOX	0x03003000

Register Name	Offset	Description
MSGBOX_CTRL_REG0	0x0000	Message Queue Attribute Control Register 0
MSGBOX_CTRL_REG1	0x0004	Message Queue Attribute Control Register 1
MSGBOXU_IRQ_EN_REG	0x0040+n*0x20	IRQ Enable for User n (n=0,1)
MSGBOXU_IRQ_STATUS_REG	0x0050+n*0x20	IRQ Status for User n (n=0,1)
MSGBOXM_FIFO_STATUS_REG	0x0100+N*0x04	FIFO Status for Message Queue N(N = 0~7)
MSGBOXM_MSG_STATUS_REG	0x0140+N*0x04	Message Status for Message Queue N(N=0~7)
MSGBOXM_MSG_REG	0x0180+N*0x04	Message Register for Message Queue N(N=0~7)
MSGBOX_DEBUG_REG	0x01C0	MSGBOX Debug Register

3.14.6. Register Description

3.14.6.1. MSGBox Control Register 0(Default Value: 0x1010_1010)

Offset: 0x0000			Register Name: MSGBOX_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

28	R/W	0x1	TRANSMIT_MQ3 Message Queue 3 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ3 Message Queue 3 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ2 Message Queue 2 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ2 Message Queue 2 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ1 Message Queue 1 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ1 Message Queue 1 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ0 Message Queue 0 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ0 Message Queue 0 is a receiver of user u 0: user0 1: user1

3.14.6.2. MSGBox Control Register 1(Default Value: 0x1010_1010)

Offset: 0x0004	Register Name: MSGBOX_CTRL_REG1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ7 Message Queue 7 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ7 Message Queue 7 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ6 Message Queue 6 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ6 Message Queue 6 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ5 Message Queue 5 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ5 Message Queue 5 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ4 Message Queue 4 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ4 Message Queue 4 is a receiver of user u 0: user0 1: user1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.14.6.3. MSGBox IRQ Enable Register u(Default Value: 0x0000_0000)

Offset:0x0040+N*0x20(N=0,1)			Register Name: MSGBOX_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	TRANSMIT_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 is not full.)
14	R/W	0x0	RECEPTION_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 has received a new message.)
13	R/W	0x0	TRANSMIT_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 is not full.)
12	R/W	0x0	RECEPTION_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 has received a new message.)
11	R/W	0x0	TRANSMIT_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 is not full.)
10	R/W	0x0	RECEPTION_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 has received a new message.)
9	R/W	0x0	TRANSMIT_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 is not full.)
8	R/W	0x0	RECEPTION_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 has received a new message.)
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 is not full.)
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 has received a new message.)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 is not full.)
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 has received a new message.)
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 is not full.)
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 has received a new message.)
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 is not full.)
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 has received a new message.)

3.14.6.4. MSGBox IRQ Status Register u(Default Value: 0x0000_AAAA)

Offset:0x0050+N*0x20(N=0,1)			**Register Name: MSGBOXU_IRQ_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x1	TRANSMIT_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 is not full. Setting 1 to this bit will clear it.
14	R/W1C	0x0	RECEPTION_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 has received a new message. Setting 1 to this bit will clear it.
13	R/W1C	0x1	TRANSMIT_MQ6_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 is not full. Setting 1 to this bit will clear it.
12	R/W1C	0x0	RECEPTION_MQ6_IRQ_PEND 0: No effect

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Pending. This bit will be pending for user u when Message Queue 6 has received a new message. Setting 1 to this bit will clear it.
11	R/W1C	0x1	TRANSMIT_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 is not full. Setting 1 to this bit will clear it.
10	R/W1C	0x0	RECEPTION_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 has received a new message. Setting 1 to this bit will clear it.
9	R/W1C	0x1	TRANSMIT_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 is not full. Set 1 to this bit will clear it.
8	R/W1C	0x0	RECEPTION_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 has received a new message. Setting 1 to this bit will clear it.
7	R/W1C	0x1	TRANSMIT_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 is not full. Setting 1 to this bit will clear it.
6	R/W1C	0x0	RECEPTION_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 has received a new message. Setting 1 to this bit will clear it.
5	R/W1C	0x1	TRANSMIT_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 is not full. Setting 1 to this bit will clear it.
4	R/W1C	0x0	RECEPTION_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 has received a new message. Setting 1 to this bit will clear it.
3	R/W1C	0x1	TRANSMIT_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 is not full. Setting 1 to this bit will clear it.
2	R/W1C	0x0	RECEPTION_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 has received a new message. Setting 1 to this bit will clear it.
1	R/W1C	0x1	TRANSMIT_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 is not

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			full. Setting 1 to this bit will clear it.
0	R/W1C	0x0	RECEPTION_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 has received a new message. Setting 1 to this bit will clear it.

3.14.6.5. MSGBox FIFO Status Register m(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~7)			Register Name: MSGBOXM_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	FIFO_FULL_FLAG 0: The Message FIFO queue is not full (space is available) 1: The Message FIFO queue is full. This FIFO status register has the status related to the message queue.

3.14.6.6. MSGBox Message Status Register m(Default Value: 0x0000_0000)

Offset:0x0140+N*0x04 (N=0~7)			Register Name: MSGBOXM_MSG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MSG_NUM Number of unread messages in the message queue. Here, limited to four messages per message queue. 000: There is no message in the message FIFO queue. 001: There is 1 message in the message FIFO queue. 010: There are 2 messages in the message FIFO queue. 011: There are 3 messages in the message FIFO queue. 100: There are 4 messages in the message FIFO queue. 101~111:/

3.14.6.7. MSGBox Message Queue Register m(Default Value: 0x0000_0000)

Offset:0x0180+N*0x04 (N=0~7)			Register Name: MSGBOXM_MSG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.14.6.8. MSGBox Debug Register(Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: MSGBOX_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	FIFO_CTRL MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode 1: Disable the corresponding FIFO (Clear FIFO)
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE In the debug mode, each user can transmit messages to itself through each message queue. 0: Normal Mode 1: Debug Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.15. Spinlock

3.15.1. Overview

In multi-core system, the Spinlock offers hardware synchronization mechanism, lock operation can prevent multi processors from handling data-sharing at the same time, and ensure coherence of data.
The Spinlock has the following features:

- Spinlock module includes 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable(less than 200 cycles)

3.15.2. Block Diagram

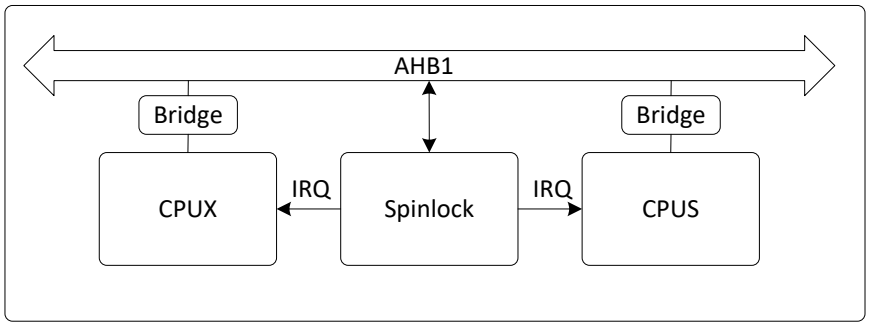


Figure 3- 43. Spinlock Block Diagram

3.15.3. Operations and Functional Descriptions

3.15.3.1. Clock and Reset

The Spinlock is hung on AHB1. Before accessing Spinlock register, open the corresponding gating bit on AHB1 and de-assert reset signal. The correct operation order is to de-assert reset signal at first, and then open the corresponding gating signal.

3.15.3.2. Typical Application

A processor lock spinlock0, when the status is locked, the processor executes specific code, and then unlocks code. Other processors is released to start reading/writing operation.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

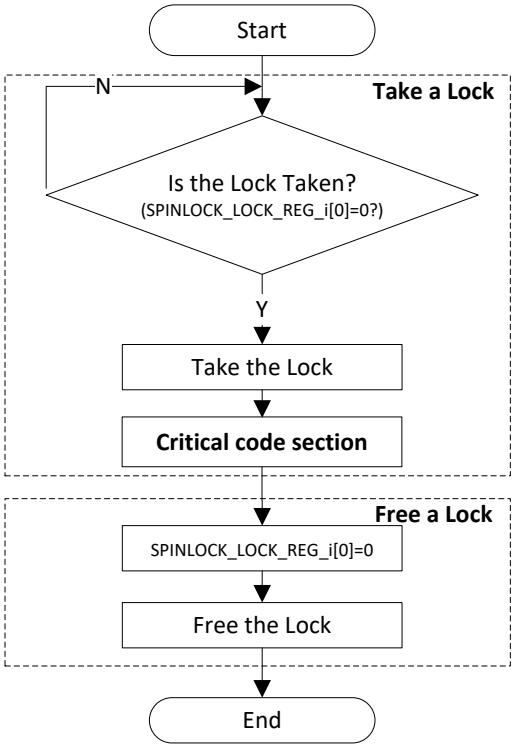


Figure 3- 44. Spinlock Typical Application Diagram

3.15.3.3. Function Implemention

3.15.3.3.1. Spinlock State Machine

When a processor uses the spinlock, it needs to acquire the status of the spinlock through **SPINLOCK_STATUS_REG**.

Reading operation: when the return value is 0, the spinlock comes into locked status; when read this status bit again, the return value is 1, the spinlock comes into locked status.

Writing operation: when the spinlock is in locked status, the spinlock can convert to unlocked status through writing 0. After reset, the spinlock is in unlocked status by default.

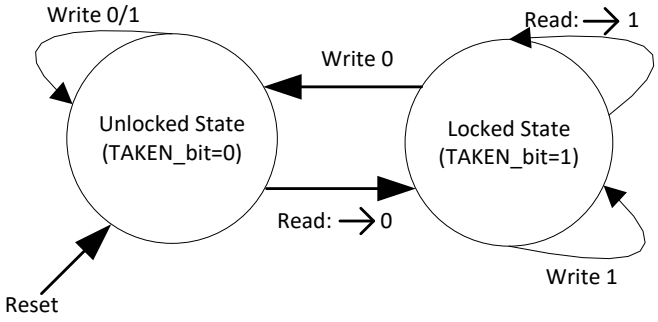


Figure 3- 45. Spinlock State Machine

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.15.3.3.2. Take and Free Spinlock

Checking out **SpinLock Register Status** is necessary when a processor takes a spinlock. This register stores the status of all 32 lock registers: TAKEN or NOT TAKEN(free).

In order to request to take a spinlock, a processor has to do a read-access to the corresponding lock register. If lock register returns 0, the processor takes this spinlock. And if lock register returns 1, the processor must retry.

Writing 0 to a lock register frees the corresponding spinlock. If the lock register is not taken, write-access has no effect. For a taken spinlock, every processor has the privilege to free this spinlock. But it is suggested that the processor which has taken the spinlock free it for strictness.

3.15.3.4. Operating Mode

3.15.3.4.1. Switch Status

(1) When the read value from **SPINLOCKN_LOCK_REG** is 0, the spinlock come into locked status.
(2) Execute application code, the status of **SPINLOCKN_STATUS_REG** is 1.
(3) Write 0 to **SPINLOCKN_LOCK_REG**, the spinlock comes into unlocked status, corresponding spinlock is released.

3.15.4. Programming Guidelines

Take CPU0 synchronization of Spinlock0 for an example, CPU0 takes the spinlock0 firstly in the instance.

To taking/freeing spinlock0, CPU0 and CPUS perform the following steps:

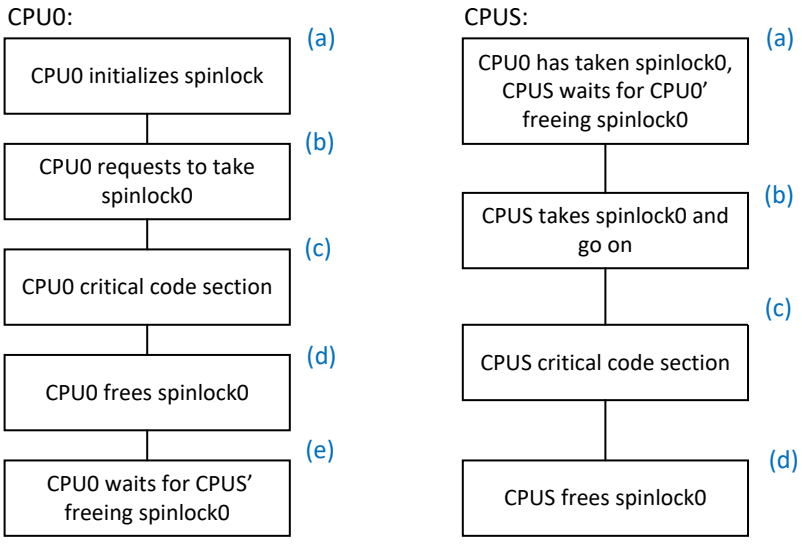


Figure 3- 46. CPU0 and CPUS Taking/Freeing Spinlock0 Process

CPU0:

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

(a) The CPU0 initializes Spinlock.
(b) Firstly, check lock register0(SPINLOCK_STATUS_REG0) status, if it is taken, check till CPU0 frees spinlock0. Then request to take spinlock0, if fail, retry till lock register0 is taken.
(c) Execute CPU0 critical code.
(d) After executing CPU0 critical code, the CPU0 frees spinlock0.
(e) The CPU0 waits for the freeing spinlock0 of CPUS.

CPUS:

(a) If the CPU0 has taken spinlock0, the CPUS waits for the freeing spinlock0 of CPU0.
(b) The CPUS requests to take spinlock0, if fail, retry till lock register0 is taken.
(c) Execute CPUS critical code.
(d) After executing CPUS critical code, the CPUS frees spinlock0.

The following codes are for reference.

```
----------------------------------------------------------------------CPU0 of Cluster0----------------------------------------------------------------------
Step 1: CPU0 initializes Spinlock
        put_wvalue(SPINLOCK_BGR_REG,0x00010000);
        put_wvalue(SPINLOCK_BGR_REG,0x00010001);
Step 2: CPU0 requests to take spinlock0
        rdata=readl(SPINLOCK_STATUS_REG0);                  //Check lock register0 status
        if(rdata != 0)    writel (0, SPINLOCK_LOCK_REG0);   //If it is taken, check till CPU0 frees spinlock0
        rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
        if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If fail, retry till lock register0 is taken
  ---------- CPU0 critical code section ----------
Step 3: CPU0 free spinlock0
        writel (0, SPINLOCK_LOCK_REG0);                     //CPU0 frees spinlock0
Step 4: CPU0 waits for CPUS' freeing spinlock0
        writel (readl(SPINLOCK_STATUS_REG0) == 1);          //CPU0 waits for the freeing spinlock0 of CPUS
----------------------------------------------------------------------CPUS----------------------------------------------------------------------
Step 1: CPU0 has taken spinlock0, CPUS waits for CPU0' freeing spinlock0
        while(readl(SPINLOCK_STATUS_REG0) == 1);            //CPUS waits for the freeing spinlock0 of CPU0
  Step 2: CPUS takes spinlock0 and go on
        rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
        if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If fail, retry till lock register0 is taken
---------- CPUS critical code section ----------
Step 3: CPUS frees spinlock0
        writel (0, SPINLOCK_LOCK_REG0);                     //CPUS frees spinlock0
```

3.15.5. Register List

Module Name	Base Address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Spinlock	0x03004000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_LOCK_REGN	0x0100+N*0x04	Spinlock Register N (N=0~31)

3.15.6. Register Description

3.15.6.1. Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 32 lock registers 01: This instance has 64 lock registers 10: This instance has 128 lock registers 11: This instance has 256 lock registers
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock register 0-31 are in the NotTaken state 1: At least one of the lock register 0-31 is in the Taken state
7:0	/	/	/

3.15.6.2. Spinlock Register Status(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken

3.15.6.3. Spinlock Register N (N=0 to 31)(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 4 Video and Graphics 330
4.1. DE 330
4.2. G2D 331
4.3. Video Decoding 332
4.3.1. Overview 332
4.3.2. Block Diagram 333
4.4. Video Encoding 334
4.4.1. VE 334
4.4.2. JPGE 336

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 4- 1. DE Block Diagram 330
Figure 4- 2. Video Decoding Block Diagram 333
Figure 4- 3. VE Block Diagram 335
Figure 4- 4. JPGE Block Diagram 337

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 4 Video and Graphics

4.1. DE

The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 4-1.

The DE has the following features:

- Output size up to 2048 x 2048
- Four alpha blending channels for main display, three channels for aux display
- Four overlay layers in each channel, and has a independent scaler
- Potter-duff compatible blending operation
- Input format: YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement and fresh tone rectify
  - Adaptive contrast enhancement
  - Content adaptive backlight control
- Supports write back only for high efficient main display and miracast

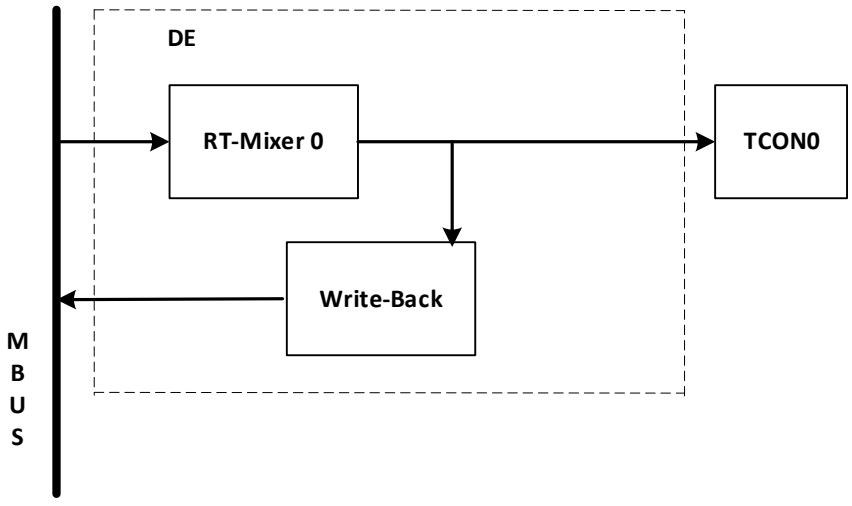


Figure 4- 1. DE Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2. G2D

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports layer size up to 2048 x 2048 pixels
- Supports input/output formats: YUV422 (semi-planar and planar format)/YUV420 (semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.3. Video Decoding

4.3.1. Overview

The Video Decoding consists of Video Control Firmware(VCF) running on ARM processor and embedded hardware Video Engine(VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoding has the following features:

- Supports ITU-T H.265 Main Profile@Level 5.0
  - Maximum video resolution: 4096 x 2048
  - Maximum decoding rate: 60 Mbps, 4K@30fps(enable afbc mode, and the second scaler is 1080p output to display)
- Supports ITU-T H.264 Base/Main/High Profile@Level 5.1
  - Maximum video resolution: 4096 x 2048
  - Maximum decoding rate: 60 Mbps, 4K@30fps(enable afbc mode, and the second scaler is 1080p output to display)
- Supports VP9
  - Maximum video resolution: 1280 x 720
  - Maximum decoding rate: 4 Mbps, 720p@30fps
- Supports AVS/AVS+
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 30 Mbps, 1080p@60fps
- Supports ITU-T H.263 Base Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbps, 1080p@60fps
- Supports VP8
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 40 Mbps, 1080p@60fps
- Supports VC-1 SP/MP/AP
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbps, 1080p@30fps
- Supports MPEG-4 SP/ASP
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbps, 1080p@60fps
- Supports MPEG-2 MP/HL
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbps, 1080p@60fps
- Supports MPEG-1 MP/HL
  - Maximum video resolution: 1920 x 1080

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Maximum decoding rate: 60 Mbps, 1080p@60fps

- Supports MJPEG
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 60 Mbps, 1080p@60fps

4.3.2. Block Diagram

The functional block diagram of the Video Decoding is as follows.

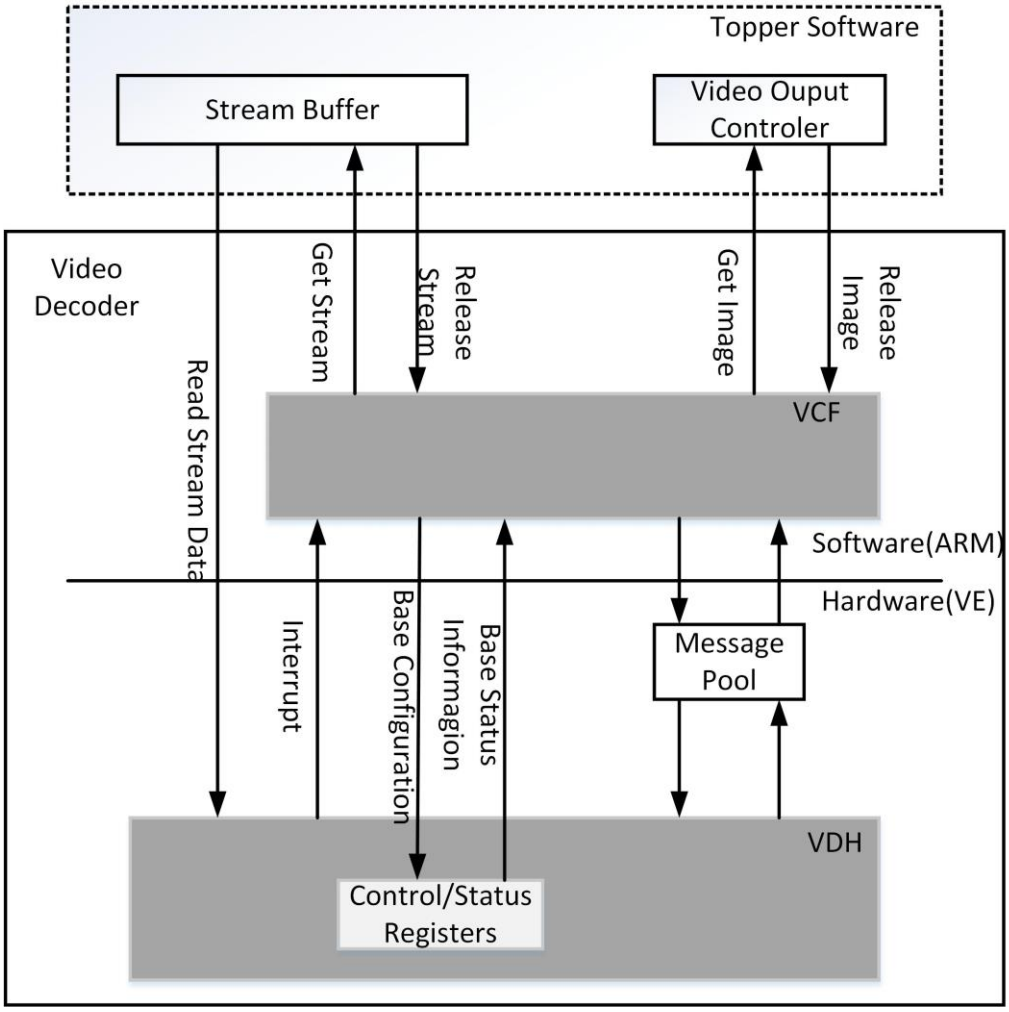


Figure 4- 2. Video Decoding Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.4. Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPGE). The VE supports H.264 encoding, and JPGE supports JPEG/MJPEG encoding.

4.4.1. VE

4.4.1.1. Overview

The VE is a H.264 encoding accelerator implemented by using hardware. It features low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports ITU-T H.264 high profile/main profile/baseline profile@level 5.2 encoding
  - Encoding of multiple slice
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Four prediction unit (PU) types of 16x8, 8x16, 16x16 and 8x8 for inter-prediction
  - Two prediction unit types of Intra16x16 and Intra4x4 for intra-prediction
  - Trans4x4
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
- Supports Classify, MB-RateControl, Fore-3D-Filter, Cyclic-Intra-Refresh, Dynamic-ME and Intra-4x4-Disable Functions in general
- Supports the input picture format of semi-planar YCbCr4:2:0
- Supports H.264 encoding with the performance of 8-megapixel 1080p@60fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192 x 96
  - Maximum picture resolution: 4096 x 4096
  - Step of the picture width or height: 8
- Supports region of interest (ROI) encoding
  - Maximum of 4 ROIs
  - Independent enable/disable control for the encoding function of each ROI
- Supports on-screen display (OSD) encoding protection that can be enabled or disabled
- Supports OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of 16 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP
- Supports the output bit rate ranging from 2 kbit/s to 60 Mbit/s
- Supports Frame Buffer Compression

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.4.1.2. Block Diagram

The functional block diagram of the VE is as follows.

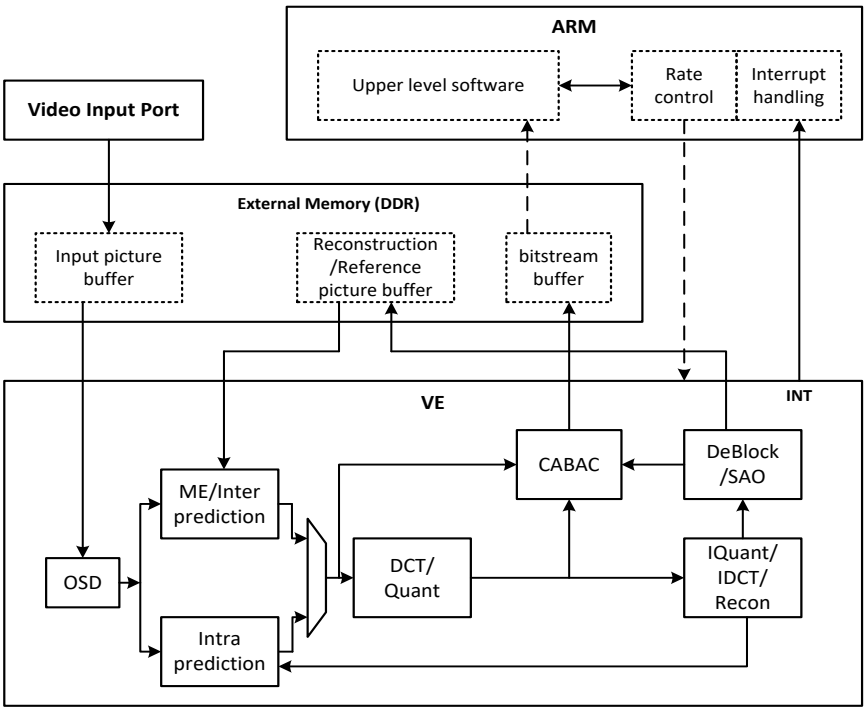


Figure 4- 3. VE Block Diagram

Based on related protocols and algorithms, the VE supports motion estimation/inter-prediction, intra-prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding/stream generation and DeBlock/SAO. The ARM software controls the bit-rate and handles interrupt.

Before the VE is enabled for video encoding, software allocates three types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The VE reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the Video Input Port module.

- **Reconstruction/Reference picture buffer**

  The VE writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, the reference pictures are read from this buffer.

- **Stream buffer**

  This buffer stores encoded streams. The VE writes streams to this buffer during encoding. This buffer is read by software.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.4.2. JPGE

4.4.2.1. Overview

The JPGE is a high-performance JPEG encoder implemented by using hardware. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0 and YCbCr4:2:2
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports JPEG encoding with the performance of 1080p@60fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192 x 96
  - Maximum picture resolution: 4096 x 4096
- Supports the picture width or height step of 8
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlapping
  - OSD overlaying before encoding for a maximum of 16 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports the color-to-gray function
- Supports the MJPEG output bit rate ranging from 2 kbit/s to 60 Mbit/s

4.4.2.2. Block Diagram

The functional block diagram of the JPGE is as follows.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

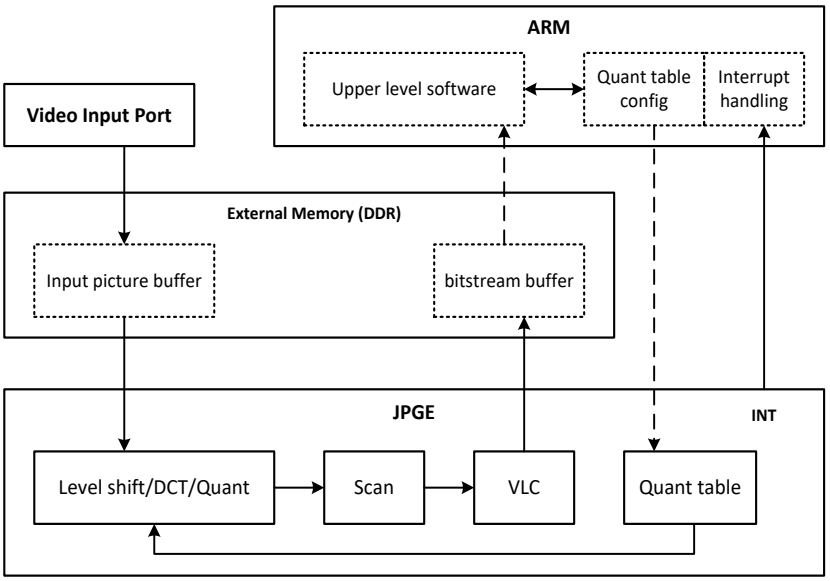


Figure 4- 4. JPGE Block Diagram

The JPGE realizes various protocol processing with large computation such as OSD, level shift, DCT, quantization, scanning, VLC encoding, and stream generation. The ARM software completes the encoding control processing such as quantization table configuration and interrupt processing.

Before the JPGE starts encoding, the software allocates two types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the Video Input Port module.

- **Stream buffer**

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 5 Memory....341
5.1. SDRAM Controller(DRAMC)....341
5.1.1. Overview....341
5.2. Nand Flash Controller(NDFC)....342
5.2.1. Overview....342
5.2.2. Block Diagram....342
5.2.3. Operations and Functional Descriptions....343
5.2.4. Programming Guidelines....352
5.2.5. Register List....354
5.2.6. Register Description....355
5.3. SD/MMC Host Controller(SMHC)....385
5.3.1. Overview....385
5.3.2. Block Diagram....385
5.3.3. Operations and Functional Descriptions....386
5.3.4. Programming Guidelines....390
5.3.5. Register List....393
5.3.6. Register Description....395

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 5- 1. NDFC Block Diagram 343
Figure 5- 2. Conventional Serial Access Cycle Diagram (SAM0) 345
Figure 5- 3. EDO Type Serial Access after Read Cycle (SAM1) 345
Figure 5- 4. Extending EDO Type Serial Access Mode (SAM2) 345
Figure 5- 5. Command Latch Cycle 346
Figure 5- 6. Address Latch Cycle 346
Figure 5- 7. Write Data to Flash Cycle 346
Figure 5- 8. Waiting R/B# Ready Diagram 347
Figure 5- 9. WE# High to RE# Low Timing Diagram 347
Figure 5- 10. RE# High to WE# Low Timing Diagram 347
Figure 5- 11. Address to Data Loading Timing Diagram 348
Figure 5- 12. Page Read Command Diagram 349
Figure 5- 13. Page Program Diagram 349
Figure 5- 14. EF-NAND Page Read Diagram 350
Figure 5- 15. Interleave Page Read Diagram 350
Figure 5- 16. Internal DMA Descriptor Chain Structure 351
Figure 5- 17. SMHC Block Diagram 386
Figure 5- 18. IDMAC Descriptor Structure Diagram 387

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 5- 1. NDFC External Signals....343
Table 5- 2. NDFC Clock Sources....344
Table 5- 3. SMHC External Signals....386
Table 5- 4. SMHC Clock Sources....387

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 5 Memory

5.1. SDRAM Controller (DRAMC)

5.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard DDR3/DDR3L/DDR4 and Low Power DDR2/3/4 SDRAM. It supports up to a 32 Gbits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The SDRAM includes the following features:

- Supports 32-bit one channel
- Supports 2 chip select signals
- Supports LPDDR2/DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 SDRAM
- Supports the power voltage of different memory device: 1.2 V, 1.5 V, 1.35 V and 1.1 V
- Supports clock frequency up to 528 MHz for LPDDR2
- Supports clock frequency up to 792 MHz for DDR3/DDR3L
- Supports clock frequency up to 672 MHz for LPDDR3
- Supports clock frequency up to 792 MHz for DDR4
- Supports clock frequency up to 792 MHz for LPDDR4
- Supports memory capacity up to 32 Gbits (4 GB)
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2. Nand Flash Controller (NDFC)

5.2.1. Overview

The NDFC is the NAND Flash Controller which supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 80 bits error per 1024 bytes data. The on chip ECC and parity checking circuit of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. There are three different kinds of modes for serial read access, mode0 is for conventional serial access , mode1 is for EDO type and the mode2 is for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Configure randomize seed by using software
- Software configure method for various system and memory types
- Supports 2 chip selects, and 2 ready_busy signals
- Up to 8-bit data bus width
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Conventional and EDO serial access method for serial reading Flash
- 80 bits/1 KB On-the-fly BCH code ECC check and error correction
- Output bits number information about corrected error
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers, and interrupt is supported
- One Command FIFO
- Internal DMA controller based on chain-structured descriptor list
- Two 256x32-bit RAM for Pipeline Procession
- Supports SDR, ONFI DDR1.0 , Toggle DDR1.0, ONFI DDR2.0 and Toggle DDR2.0 RAW NAND FLASH
- Maximum IO rate of 50 MHz in SDR mode, and 100 MHz in both DDR1.0 and DDR2.0 mode
- Self-debug for NDFC debug

5.2.2. Block Diagram

The block diagram of the NDFC is shown as follows.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

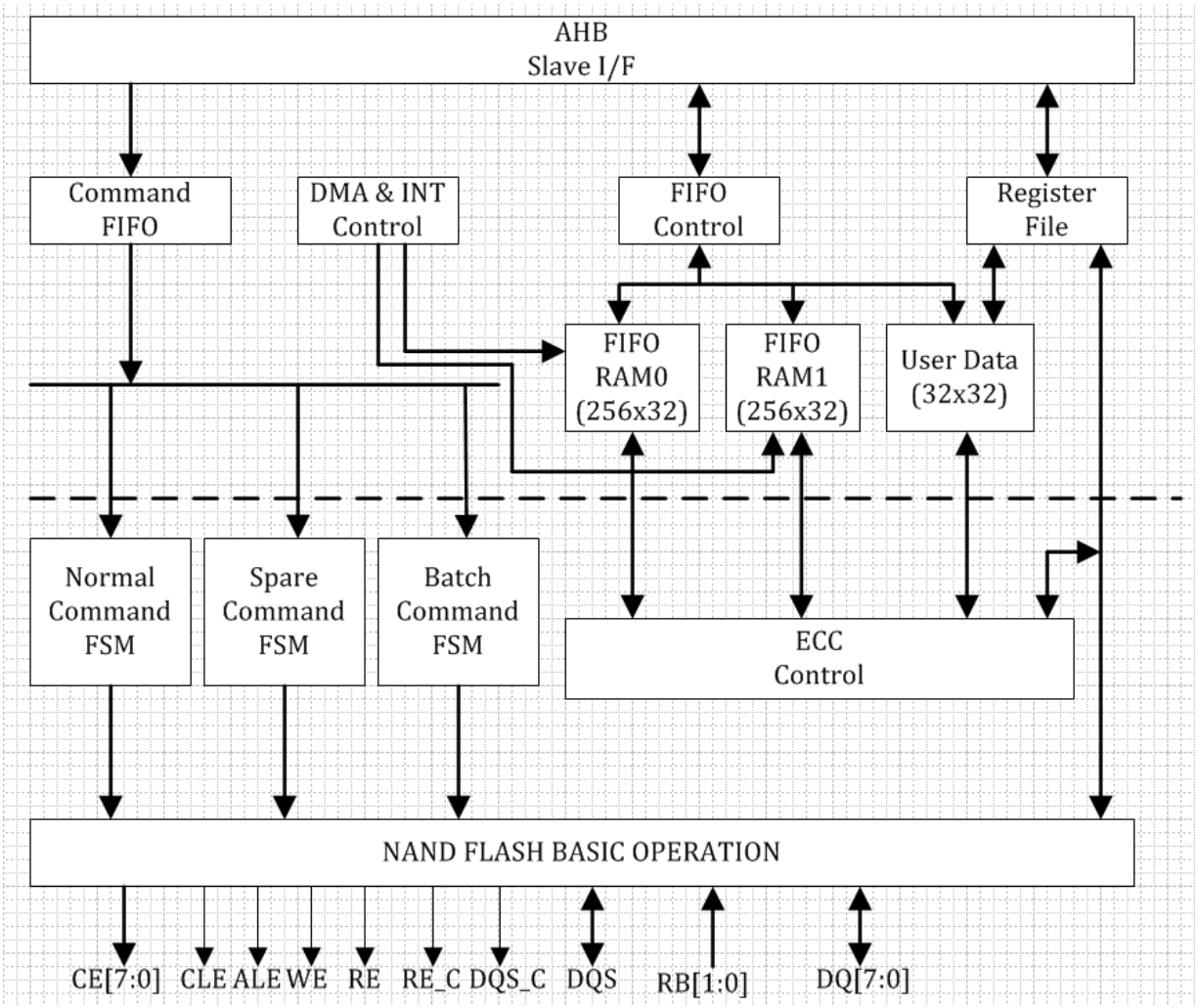


Figure 5- 1. NDFC Block Diagram

5.2.3. Operations and Functional Descriptions

5.2.3.1. External Signals

Table 5-1 describes the external signals of NDFC. DQ0~DQ7 and DQS are bidirectional I/O. WE,ALE,CLE,CE,RE are output pin, RB is input pin. The RB pin in the NAND device is an open-drain driver, which must need a pull-up resistor.

Table 5- 1. NDFC External Signals

Signal	Description	Type
NAND_WE	Write enable	O
NAND_RE	Read enable	O
NAND_ALE	Address latch enable, high is active	O
NAND_CLE	Command latch enable, high is active	O
NAND_CE0	Chip enable, low is active	O
NAND_CE1	Chip enable, low is active	O

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

NAND_RB0	Ready/busy, low is active	I
NAND_RB1	Ready/busy, low is active	I
NAND_DQ0	Data input / output	I/O
NAND_DQ1	Data input / output	I/O
NAND_DQ2	Data input / output	I/O
NAND_DQ3	Data input / output	I/O
NAND_DQ4	Data input / output	I/O
NAND_DQ5	Data input / output	I/O
NAND_DQ6	Data input / output	I/O
NAND_DQ7	Data input / output	I/O
NAND_DQS	Data strobe	I/O

5.2.3.2. Clock Sources

To ensure ECC efficiency, ECC engine and NDFC internal logic use different clock. The clock of NDFC internal logic is set by **NAND_0 Clock Register**, the clock of ECC engine is set by **NAND_1 Clock Register**. Note that **NAND_0 Clock Register** set the internal logic clock of NDFC, but the frequency of external Nand Flash device is half of NDFC internal logic clock. That is, if external Nand Flash runs at 40 MHz, then NDFC need set to 80 MHz.

Both ECC engine and NDFC internal logic have five different clock sources. Users can select one of them to make ECC engine or internal logic clock source. Table 5-2 describles the clock sources of NDFC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5- 2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24 MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600 MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600 MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1.2 GHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1.2 GHz

5.2.3.3. Timing Diagram

Typically, there are two kinds of serial access methods. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

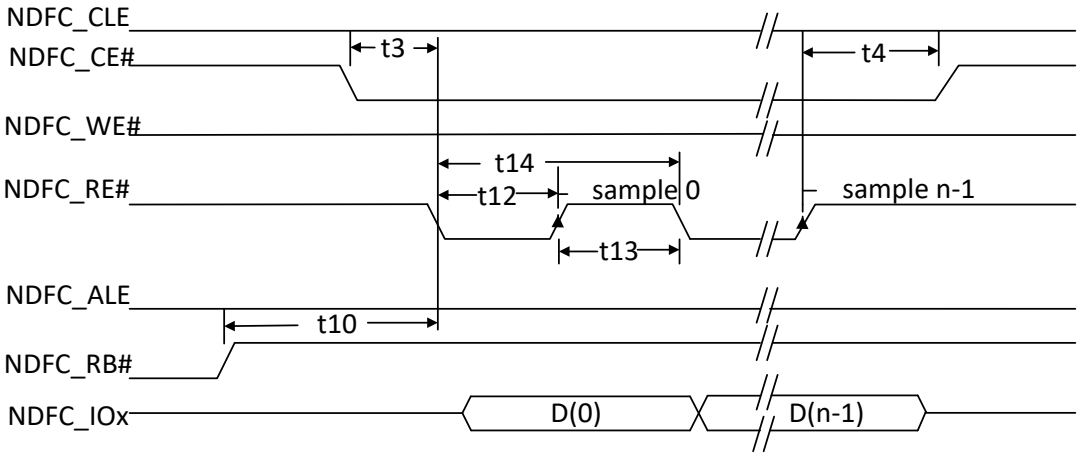


Figure 5- 2. Conventional Serial Access Cycle Diagram (SAM0)

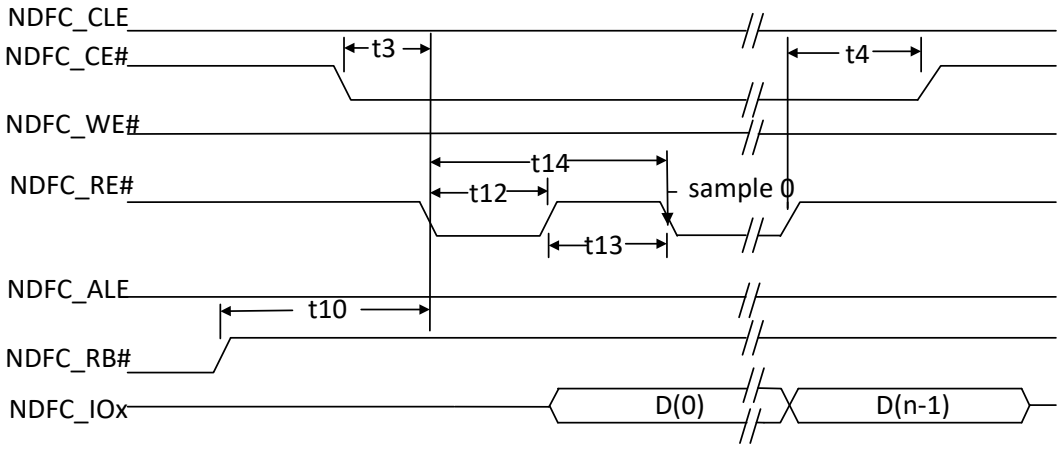


Figure 5- 3. EDO Type Serial Access after Read Cycle (SAM1)

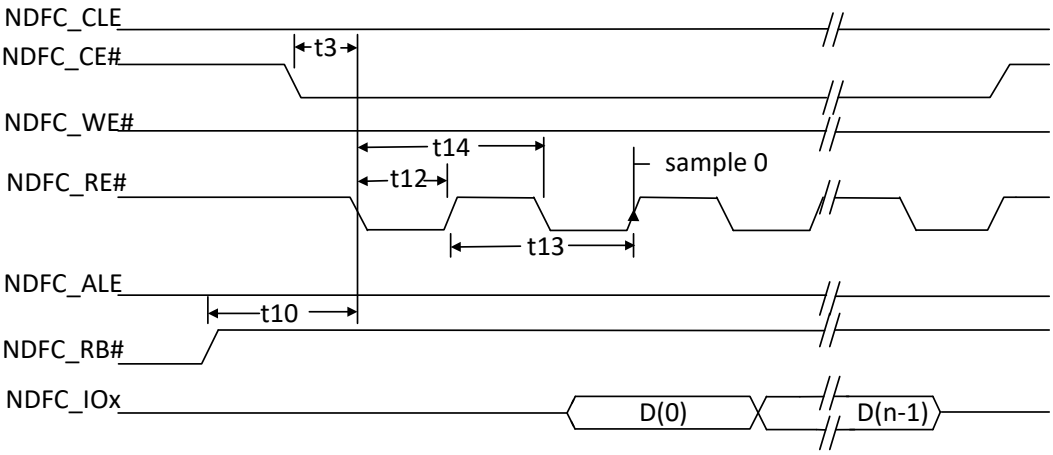


Figure 5- 4. Extending EDO Type Serial Access Mode (SAM2)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

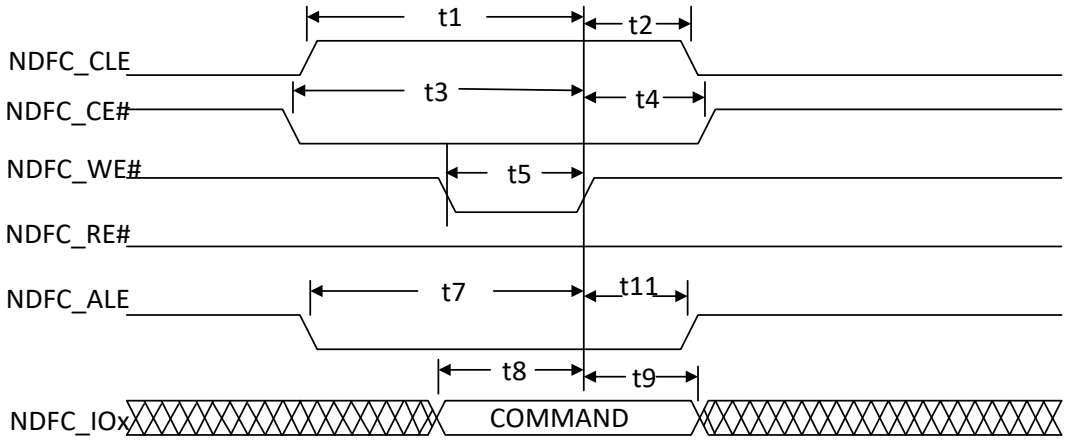


Figure 5- 5. Command Latch Cycle

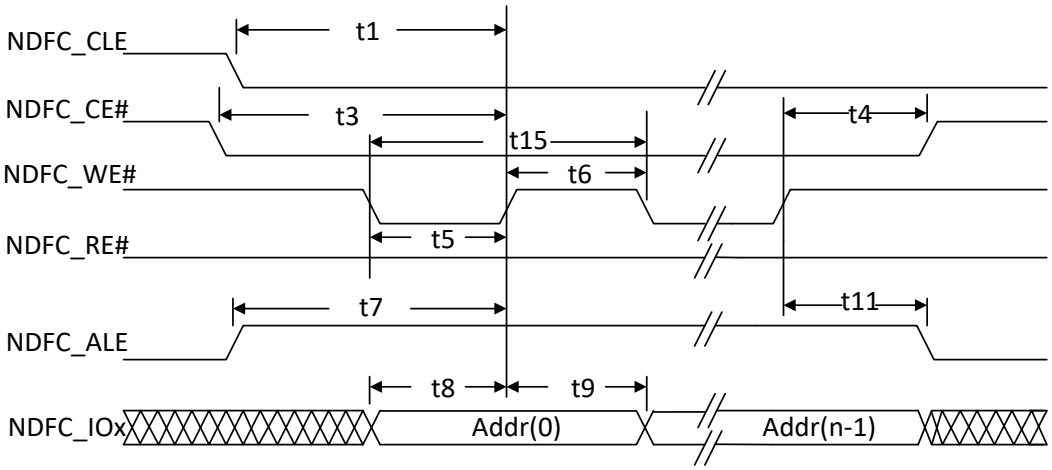


Figure 5- 6. Address Latch Cycle

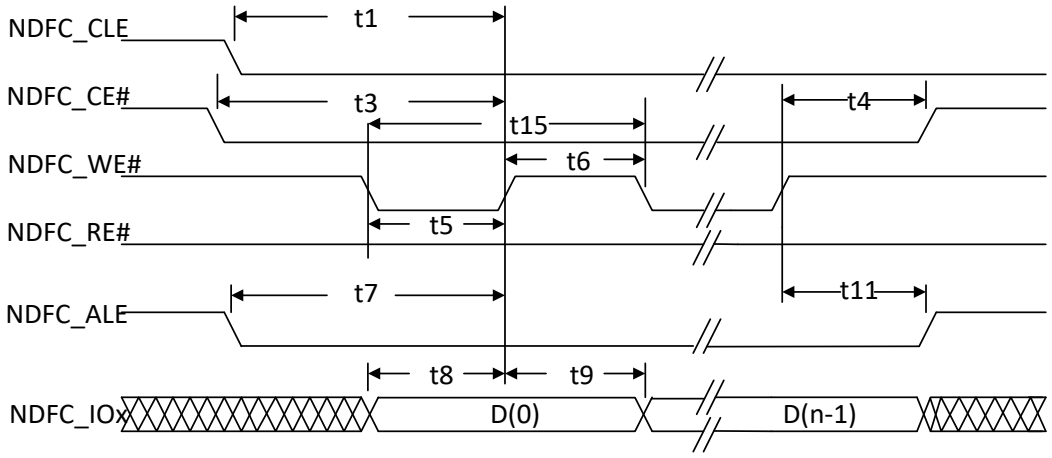


Figure 5- 7. Write Data to Flash Cycle

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 5- 8. Waiting R/B# Ready Diagram

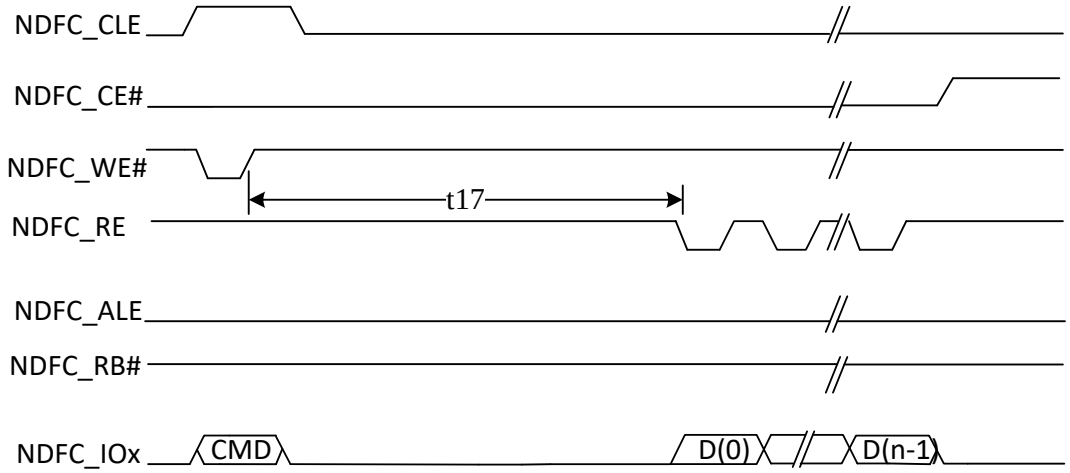


Figure 5- 9. WE# High to RE# Low Timing Diagram

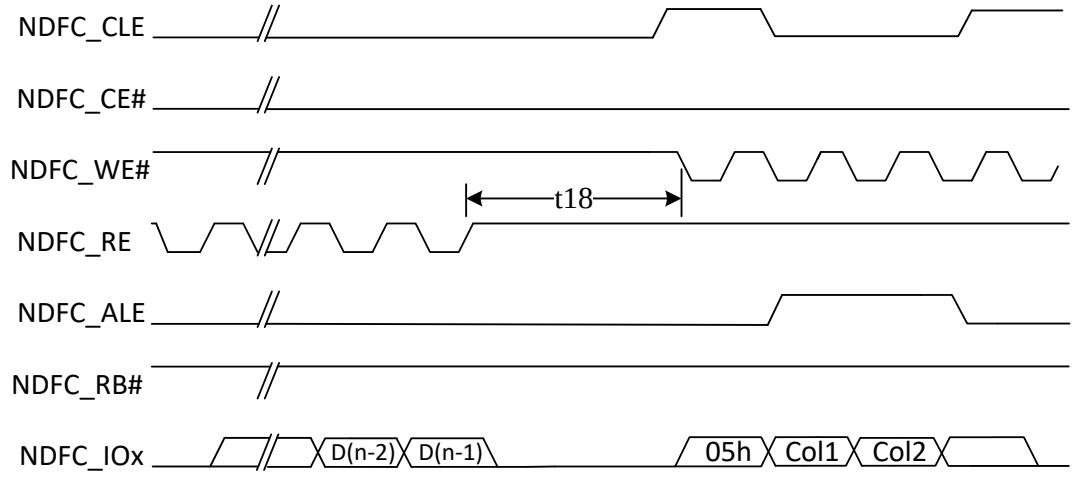


Figure 5- 10. RE# High to WE# Low Timing Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

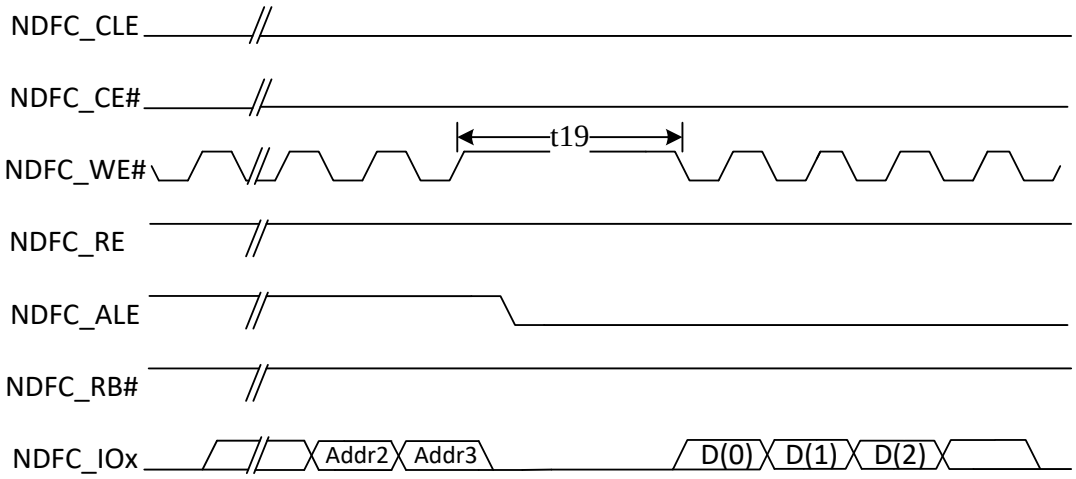


Figure 5- 11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing(ns)	Notes
t1	NDFC_CLE setup time	2T	
t2	NDFC_CLE hold time	2T	
t3	NDFC_CE setup time	2T	
t4	NDFC_CE hold time	2T	
t5	NDFC_WE# pulse width	T(1)	
t6	NDFC_WE# hold time	T	
t7	NDFC_ALE setup time	2T	
t8	Data setup time	T	
t9	Data hold time	T	
t10	Ready to NDFC_RE# low	3T	
t11	NDFC_ALE hold time	2T	
t12	NDFC_RE# pulse width	T	
t13	NDFC_RE# hold time	T	
t14	Read cycle time	2T	
t15	Write cycle time	2T	
t16	NDFC_WE# high to R/B# busy	T_WB(2)	Specified by timing configure register (NDFC_TIMING_CFG)
t17	NDFC_WE# high to NDFC_RE# low	T_WHR(3)	Specified by timing configure register (NDFC_TIMING_CFG)
t18	NDFC_RE# high to NDFC_WE# low	T_RHW(4)	Specified by timing configure register (NDFC_TIMING_CFG)
t19	Address to Data Loading time	T_ADL(5)	Specified by timing configure register (NDFC_TIMING_CFG)

Note(1): T is the cycle of the internal clock.

Note(2),(3),(4),(5): These values are configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

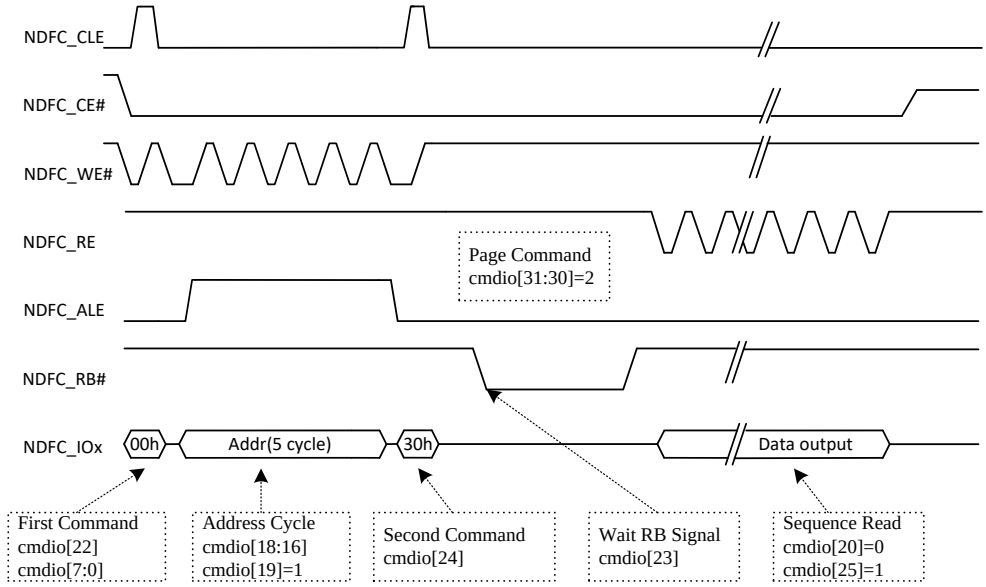


Figure 5- 12. Page Read Command Diagram

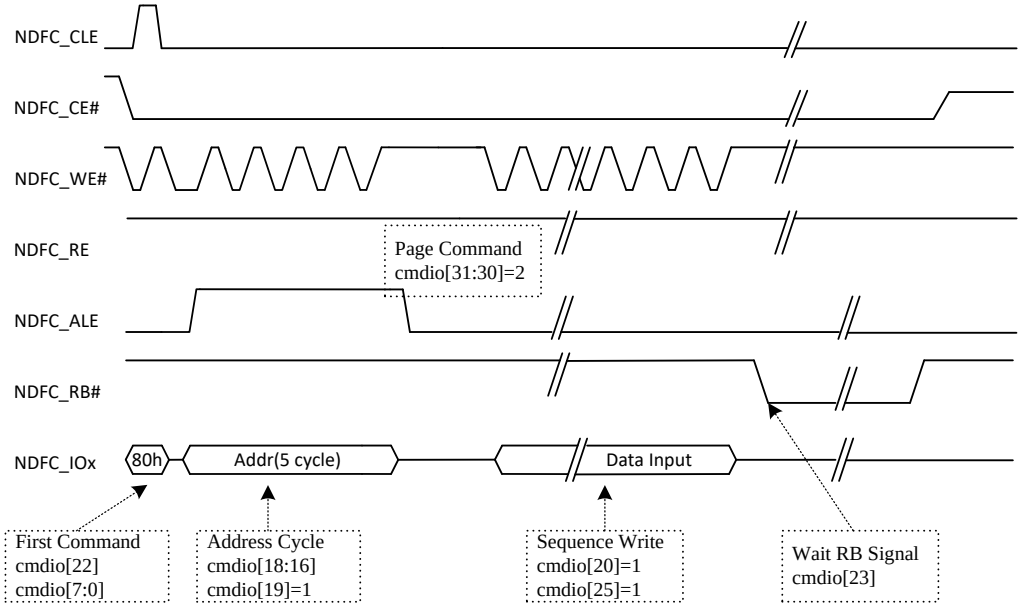


Figure 5- 13. Page Program Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

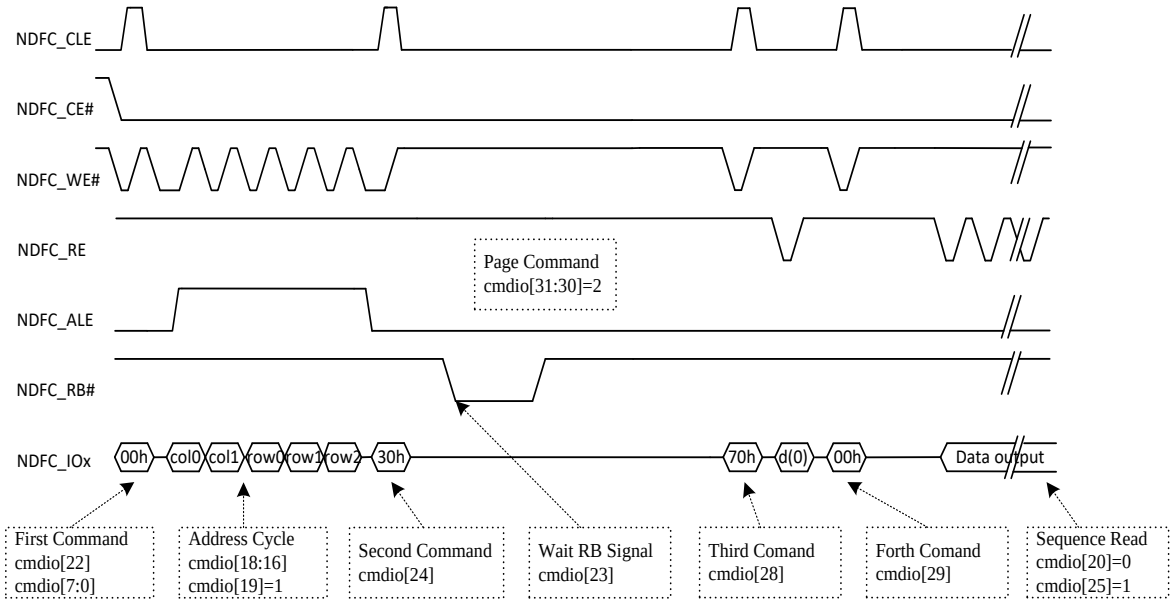


Figure 5- 14. EF-NAND Page Read Diagram

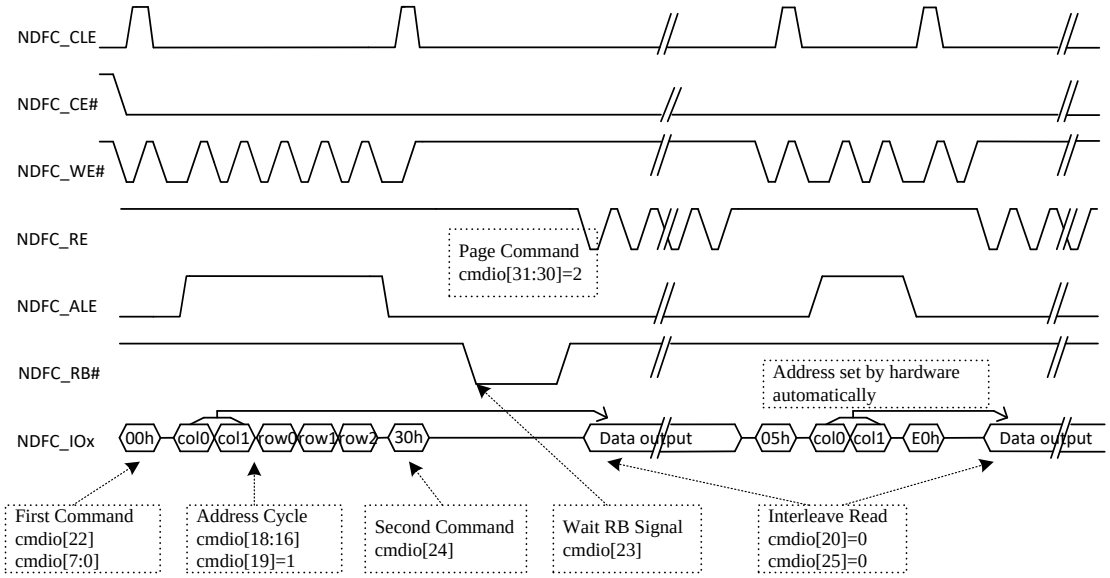


Figure 5- 15. Interleave Page Read Diagram

5.2.3.4. Internal DMA Controller Descriptors

5.2.3.4.1. Descriptor Structure

The internal DMA controller of the NDFC can transfer data between DMA FIFO in NDFC and DMA buffer in host memory using DMA descriptors. DMA descriptors in the host memory with chain structure is shown in Figure 5-16.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

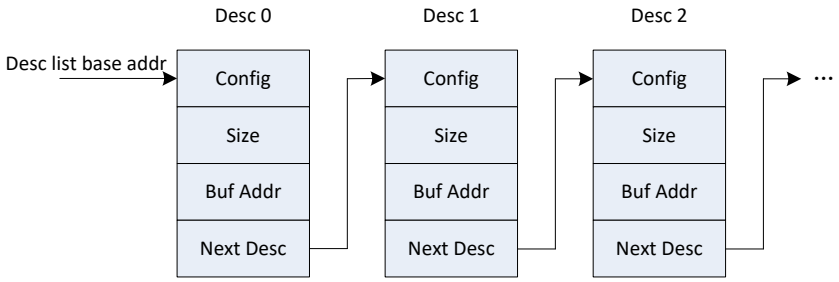


Figure 5- 16. Internal DMA Descriptor Chain Structure

The start address of DMA descriptor list must be word (32-bit) aligned, and will be configured to **NDFC DMA Descriptor List Base Address Register**. Each DMA descriptor consists of four words(32-bit).

5.2.3.4.2. Descriptor Definition

Config	
Bit	**Description**
31:4	/
3	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first descriptor.
2	LAST_FLAG When set, this bit indicates that the buffers pointed by this descriptor are the last data buffer.
1:0	/

Size	
Bit	**Description**
31:16	/
15:0	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 8 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

Buff Addr	
Bit	**Description**
31:0	BUFF_ADDR These bits indicate the physical address of DMA data buffer in host memory. The buffer address must be 4 bytes aligned.

Next Description	
Bit	**Description**
31:0	NEXT_DESC_ADDR These bits indicate the pointer to the physical host memory of the next descriptor is present.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.3.5. NDFC Data Block Mask Register

ECC_DATA_BLOCK is written or read through the value of **NDFC Data Block Mask Register**. But in real application scenario, capacity could not waste, so writing operation usually does not use the function, only reading operation uses. In reading operation, we divides Sequence mode and Interleave mode through the store position of user_data.
Sequence mode: The user_data of every 1K main area data and ECC encoder data are next to the main area data.
Interleave mode: All user_data and ECC encoder data are stored from page_size position.

When any **ECC_DATA_BLOCK** within page is read through batch command(**NDFC_CMD_TYPE** in 0x24 register is 0x10), the register is used differently for Sequence mode and Interleave mode.

Sequence mode can only support continue **ECC_DATA_BLOCK**, the register value can only be 0x1,0x3,0x7,etc. But Interleave mode has not limit.

Whether Sequence mode or Interleave mode, the first reading **ECC_DATA_BLOCK** is used to calculate corresponding column address, and column address is written to 0x14 and 0x18 register.

5.2.3.6. NDFC Enhanced Feature Register

The bit[24] and bit[23:16] of the register are used to judge whether free space need be padded random data except valid data when batch command function is used.

Take a SanDisk chip(SDTNQGAMA-008G) as an example:
Refer to the specification of the SanDisk chip, the page_size of the SanDisk chip is (16384+1280) bytes, but BCH level uses 40bit/1K, if user_data is 32 bytes, then the used space is 1152 bytes(14*40/8*16+32), the 128 bytes (1280-1152) space is not written. If there need be filled with 1 page, then the bit[24] of the register can be set to 1, and the bit[23:16] is written to 0x80, that the controller can automatically pad 128 bytes random data.

NOTE

Make sure that random function is enabled if there need be sent random data, that is, the NDFC_RANDOM_EN of 0x34 register is 0x1, or else the padding data is non-random, is all-0.

5.2.4. Programming Guidelines

5.2.4.1. Initializing Nand Flash

The NAND Flash is initialized as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step2:Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; write 0xFF to NDFC_CMD[NDFC_CMD_LOW_BYTE] to send reset command.
Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

write 1 to clear the flag.

5.2.4.2. Erasing Nand Flash

The NAND Flash is erased as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step2: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB;
Configure NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of address to be transferred;
Write the address of the block to be erased in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x60 to send block erase command.

Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

Step4: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step5: Set NDFC_CMD[NDFC_WAIT_FLAG] to 1 to ensure wait RB, set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command; set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0xD0 to send erasing command.

Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

Step7: Read flash state until flash is ready, configure NDFC_CNT[NDFC_DATA_CNT] to set 1byte transfer data, set NDFC_CMD[NDFC_SEND_FIRST_CMD, NDFC_DATA_TRANS] to 0x3 to send the first command and transfer data. Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x70 to send read status command, read RAM0_BASE to wait ready status.

5.2.4.3. Writing Nand Flash

Step1: Erase the address of the block to be operated.

Step2: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step3: Configure RAM0_BASE to write data to RAM0.

Step4: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;
Set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_DATA_TRANS, NDFC_ACCESS_DIR] to 0x3 to set access direction as writing;
Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x80 to send page program command.

Step5: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step6: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x10 to send end command.

Step7: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.4.4. Reading Nand Flash

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step2: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;

Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command;

Configure NDFC_CMD[NDFC_ACCESS_DIR] to 0 to set access direction as reading;

Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;

Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x00 to send page read command.

Step3: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step4: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x30 to send end command.

Step5: Read RAM0_BASE to get data from flash.

Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

5.2.5. Register List

Module Name	Base Address
NDFC	0x04011000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register
NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_DATA_BLOCK_MASK	0x001C	NDFC Data Block Mask Register
NDFC_CNT	0x0020	NDFC Data Counter Register
NDFC_CMD	0x0024	NDFC Commands IO Register
NDFC_RCMD_SET	0x0028	Read Command Set Register for Vendor's NAND Memory
NDFC_WCMD_SET	0x002C	Write Command Set Register for Vendor's NAND Memory
NDFC_ECC_CTL	0x0034	NDFC ECC Control Register
NDFC_ECC_ST	0x0038	NDFC ECC Status Register
NDFC_DATA_PAT_STA	0x003C	NDFC Data Pattern Status Register
NDFC_EFR	0x0040	NDFC Enhanced Feature Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

NDFC_RDATA_STA_CTL	0x0044	NDFC Read Data Status Control Register
NDFC_RDATA_STA_0	0x0048	NDFC Read Data Status Register 0
NDFC_RDATA_STA_1	0x004C	NDFC Read Data Status Register 1
NDFC_ERR_CNT_N	0x0050+0x04*N	NDFC Error Counter Register(N from 0 to 7)
NDFC_USER_DATA_LEN_N	0x0070+0x04*N	NDFC User Data Length Register(N from 0 to 3)
NDFC_USER_DATA_N	0x0080+0x04*N	NDFC User Data Field Register N (N from 0 to 31)
NDFC_EFNAND_STA	0x0110	NDFC EFNAND Status Register
NDFC_SPARE_AREA	0x0114	NDFC Spare Area Register
NDFC_PAT_ID	0x0118	NDFC Pattern ID Register
NDFC_DDR2_SPEC_CTL	0x011C	NDFC DDR2 Specific Control Register
NDFC_NDMA_MODE_CTL	0x0120	NDFC Normal DMA Mode Control Register
NDFC_MDMA_DLBA_REG	0x0200	NDFC MBUS DMA Descriptor List Base Address Register
NDFC_MDMA_STA	0x0204	NDFC MBUS DMA Interrupt Status Register
NDFC_DMA_INT_MASK	0x0208	NDFC MBUS DMA Interrupt Enable Register
NDFC_MDMA_CUR_DESC_ADDR	0x020C	NDFC MBUS DMA Current Descriptor Address Register
NDFC_MDMA_CUR_BUF_ADDR	0x0210	NDFC MBUS DMA Current Buffer Address Register
NDFC_DMA_CNT	0x0214	NDFC DMA Byte Counter Register
NDFC_IO_DATA	0x0300	NDFC Input/Output Data Register

5.2.6. Register Description

5.2.6.1. 0x0000 NDFC Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: NDFC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	NDFC_DDR_TYPE Type of DDR data interface This bit is valid when NF_TYPE is 0x2 or 0x3. 0: DDR 1: DDR2
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for NAND Flash Chips 0000: NDFC Select Chip 0 0001: NDFC Select Chip 1 0010: NDFC Select Chip 2 0011: NDFC Select Chip 3 0100: NDFC Select Chip 4 0101: NDFC Select Chip 5 0110: NDFC Select Chip 6 0111: NDFC Select Chip 7 1000: NDFC Select Chip 8 1001: NDFC Select Chip 9

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1010: NDFC Select Chip 10 1011: NDFC Select Chip 11 1100: NDFC Select Chip 12 1101: NDFC Select Chip 13 1110: NDFC Select Chip 14 1111: NDFC Select Chip 15
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat Data Mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0x0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB method 1: Access internal RAM by DMA method
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 000: 1KB 001: 2KB 010: 4KB 011: 8KB 100: 16KB 101: 32KB The page size is for main field data.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip Select Signal CE# Control during NAND Operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic controls Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC External R/B Signal Select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W1C	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset
0	R/W	0x0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

5.2.6.2. 0x0004 NDFC Status Register (Default Value: 0x0000_0F00)

Offset: 0x0004			**Register Name: NDFC_ST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is more than threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is more than threshold value. 1: The number of bit 0 during current read operation is less than or equal to the threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
11	R	0x1	NDFC_RB_STATE3 NAND Flash R/B 3 Line State

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x1	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x1	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x1	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE state 1: NDFC FSM in BUSY state When NDFC_STA is 0, NDFC can accept new command and process command.
3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W1C	0x0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
1	R/W1C	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
0	R/W1C	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

5.2.6.3. 0x0008 NDFC Interrupt and DMA Enable Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: NDFC_INT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in normal command work mode or one batch command work mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state. 0: Disable 1: Enable

5.2.6.4. 0x000C NDFC Timing Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: NDFC_TIMING_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE In SDR mode: 00: Normal 01: EDO 10: E-EDO Others: Reserved In DDR mode: 1~15 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0…7] .

5.2.6.5. 0x0010 NDFC Timing Configure Register(Default Value: 0x0000_0095)

Offset: 0x0010			Register Name: NDFC_TIMING_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 12*2T 01: 20*2T 10: 28*2T 11: 60*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS DQS Setup Time for Data Input Start 0: 4*2T 1: 20*2T
10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 2*2T 001: 6*2T 010: 10*2T 011: 14*2T 100: 22*2T 101: 30*2T 110/111: 62*2T
7:6	R/W	0x2	T_RHW Cycle Number from RE# High to WE# Low 00: 4*2T 01: 12*2T 10: 20*2T 11: 28*2T
5:4	R/W	0x1	T_WHR Cycle Number from WE# High to RE# Low 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
3:2	R/W	0x1	T_ADL Cycle Number from Address to Data Loading

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
1:0	R/W	0x1	T_WB Cycle Number from WE# High to Busy 00:14*2T 01: 22*2T 10: 30*2T 11: 38*2T

5.2.6.6. 0x0014 NDFC Address Low Word Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: NDFC_ADDR_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

5.2.6.7. 0x0018 NDFC Address High Word Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: NDFC_ADDR_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7 NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

5.2.6.8. 0x001C NDFC Data Block Mask Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: NDFC_DATA_BLOCK_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 31 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
30	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 30 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
29	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 29 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
28	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 28 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
27	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 27 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
26	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 26 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
25	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 25 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
24	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 24 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable 1 data block = 1024 bytes main field data.
23	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 23 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
22	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 22 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
21	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 21 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
20	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 20 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
19	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 19 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
18	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 18 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
17	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 17 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 16 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
15	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 15 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
14	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 14 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
13	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 13 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
12	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 12 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
11	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 11 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
10	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 10 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
9	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 9 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable 1 data block = 1024 bytes main field data.
8	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 8 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
7	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 7 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
6	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 6 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
5	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 5 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
4	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 4 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
3	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 3 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
2	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 2 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 1 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
0	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 0 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.

5.2.6.9. 0x0020 NDFC Data Counter Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: NDFC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

5.2.6.10. 0x0024 NDFC Command IO Register (Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: NDFC_CMD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common command for normal operation 01: Special command for Flash spare field operation 10: Page command for batch process operation 11: Reserved
29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Donot send fourth set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Donot send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
27	R/W	0x0	NDFC_SEND_RANDOM_CMD2_CTL 0: Donot send random cmd2 (NDFC_RANDOM_CMD2) 1: Send random cmd2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Note: It is only valid in batch cmd operation and writing operation.
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for common command and special command. 0: No action 1: DMA transfer automatically It only is active when NDFC_RAM_METHOD is 1. If this bit is set to 1, NDFC should setup DRQ to fetch data before output to Flash or NDFC should setup DRQ to send to system memory after fetching data from Flash. If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, donot care about this bit for other two commands. 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD 0: Donot send second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it cannot when the internal NDFC_RB wire is BUSY
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Donot send first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field NDFC_ACCESS_DIR
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Donot send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by NDFC_ADR_NUM field
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			111: 8 cycles address field
15:10	/	/	/
9:8	R/W	0x0	NDFC_ADR_NUM_IN_PAGE_CMD The number of address cycles during page command. 00: 2 address cycles 11: 5 address cycles Others: reserved
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC command low byte data This command will be sent to external Flash by NDFC.

5.2.6.11. 0x0028 NDFC Command Set Register 0(Default Value: 0x00E0_0530)

Offset: 0x0028			Register Name: NDFC_CMD_SET0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x00	NDFC_RANDOM_CMD2 Used for Batch Operation
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

5.2.6.12. 0x002C NDFC Command Set Register 1(Default Value: 0x7000_8510)

Offset: 0x002C			Register Name: NDFC_CMD_SET1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND Page Read Operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read Operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

5.2.6.13. 0x0034 NDFC ECC Control Register(Default Value: 0x4A80_0008)

Offset: 0x0034			Register Name: NDFC_ECC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when NDFC_RANDOM_EN is set to '1'.
15:8	R/W	0x0	NDFC_ECC_MODE 00000000: BCH-16 00000001: BCH-24 00000010: BCH-28 00000011: BCH-32 00000100: BCH-40 00000101: BCH-44 00000110: BCH-48 00000111: BCH-52 00001000: BCH-56 00001001: BCH-60 00001010: BCH-64 00001011: BCH-68 00001100: BCH-72 00001101: BCH-76 00001110: BCH-80 Others : Reserved
7	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
6	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
5	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
4	R/W	0x0	NDFC_ECC_EXCEPTION 0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. **Note: It is only active when ECC is ON**
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error Correction function no pipeline with next block operation 1: Error Correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.6.14. 0x0038 NDFC ECC Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: NDFC_ECC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 31 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[31] of this register is corresponding the 31th ECC data block. 1 ECC Data Block = 1024 bytes.
30	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 30 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[30] of this register is corresponding the 30th ECC data block. 1 ECC Data Block = 1024 bytes.
29	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 29 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[29] of this register is corresponding the 29th ECC data block. 1 ECC Data Block = 1024 bytes.
28	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 28 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[28] of this register is corresponding the 28th ECC data block. 1 ECC Data Block = 1024 bytes.
27	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 27 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[27] of this register is corresponding the 27th ECC data block. 1 ECC Data Block = 1024 bytes.
26	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 26 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[26] of this register is corresponding the 26th ECC data block. 1 ECC Data Block = 1024 bytes.
25	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 25 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[25] of this register is corresponding the 25th ECC data block. 1 ECC Data

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Block = 1024 bytes.
24	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 24 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[24] of this register is corresponding the 24th ECC data block. 1 ECC Data Block = 1024 bytes.
23	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 23 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[23] of this register is corresponding the 23th ECC data block. 1 ECC Data Block = 1024 bytes.
22	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 22 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[22] of this register is corresponding the 22th ECC data block. 1 ECC Data Block = 1024 bytes.
21	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 21 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[21] of this register is corresponding the 21th ECC data block. 1 ECC Data Block = 1024 bytes.
20	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 20 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[20] of this register is corresponding the 20th ECC data block. 1 ECC Data Block = 1024 bytes.
19	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 19 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[19] of this register is corresponding the 19th ECC data block. 1 ECC Data Block = 1024 bytes.
18	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 18 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[18] of this register is corresponding the 18th ECC data block. 1 ECC Data Block = 1024 bytes.
17	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 17

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[17] of this register is corresponding the 17th ECC data block. 1 ECC Data Block = 1024 bytes.
16	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 16 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[16] of this register is corresponding the 16th ECC data block. 1 ECC Data Block = 1024 bytes.
15	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 15 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[15] of this register is corresponding the 15th ECC data block. 1 ECC Data Block = 1024 bytes.
14	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 14 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[14] of this register is corresponding the 14th ECC data block. 1 ECC Data Block = 1024 bytes.
13	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 13 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[13] of this register is corresponding the 13th ECC data block. 1 ECC Data Block = 1024 bytes.
12	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 12 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[12] of this register is corresponding the 12th ECC data block. 1 ECC Data Block = 1024 bytes.
11	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 11 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[11] of this register is corresponding the 11th ECC data block. 1 ECC Data Block = 1024 bytes.
10	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 10 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[10] of this register is corresponding the 10th ECC data block. 1 ECC Data

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Block = 1024 bytes.
9	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 9 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[9] of this register is corresponding the 9th ECC data block. 1 ECC Data Block = 1024 bytes.
8	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 8 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[8] of this register is corresponding the 8th ECC data block. 1 ECC Data Block = 1024 bytes.
7	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 7 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[7] of this register is corresponding the 7th ECC data block. 1 ECC Data Block = 1024 bytes.
6	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 6 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[6] of this register is corresponding the 6th ECC data block. 1 ECC Data Block = 1024 bytes.
5	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 5 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[5] of this register is corresponding the 5th ECC data block. 1 ECC Data Block = 1024 bytes.
4	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 4 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[4] of this register is corresponding the 4th ECC data block. 1 ECC Data Block = 1024 bytes.
3	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 3 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[3] of this register is corresponding the 3rd ECC data block. 1 ECC Data Block = 1024 bytes.
2	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[2] of this register is corresponding the 2nd ECC data block. 1 ECC Data Block = 1024 bytes.
1	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 1 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[1] of this register is corresponding the 1st ECC data block. 1 ECC Data Block = 1024 bytes.
0	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 0 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[0] of this register is corresponding the 0 ECC data block. 1 ECC Data Block = 1024 bytes.

5.2.6.15. 0x003C NDFC Data Pattern Status Register(Default Value: 0x0000_0000)

Offset: 0x003C			**Register Name: NDFC_DATA_PAT_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 31 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
30	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 30 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
29	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 29 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
28	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 28 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
27	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 27 when read from external NAND flash. 0: No found

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
26	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 26 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
25	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 25 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
24	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 24 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
23	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 23 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
22	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 22 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
21	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 21 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
20	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 20 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
19	R	0x0	Special pattern (all 0x00 or all 0xff) found Flag for Data Block 19 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
18	R	0x0	Special pattern (all 0x00 or all 0xff) Found flag for Data Block 18 when read from external NAND flash. 0: No found

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
17	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 17 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
16	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 16 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
15	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 15 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
14	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 14 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
13	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 13 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
12	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 12 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
11	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 11 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
10	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 10 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
9	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 9 when read from external NAND flash. 0: No found

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
8	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 8 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
7	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 7 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
6	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 6 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
5	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 5 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
4	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 4 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
3	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 3 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
2	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 2 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
1	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 1 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
0	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 0 when read from external NAND flash. 0: No found

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.

5.2.6.16. 0x0040 NDFC Enhanced Feature Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: NDFC_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DB_CNT_EN Dummy_Byte_Count_EN 0:Disable fill Dummy Byte 1:Enable fill Dummy Byte
23:16	R/W	0x0	DB_CNT Dummy_Byte_Count After PAGE CMD operation finishing sending out the main data , user data and ECC code, controller would send dummy byte to fill the unused space in one page. **Note: It is only valid in PAGE CMD operation(NDFC_CMD_TYPE=0x3), and this function is disabled when Dummy_Byte_Count_EN is 0.** **If the NDFC_RANDOM_EN = 0x0, the value of the dummy byte is 0, so in order to improve the stability, when using this function , it is better to set the NDFC_RANDOM_EN to 0x1.**
15:9	/	/	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit 0: Write Protect is active 1: Write Protect is not active When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special error bits are inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

5.2.6.17. 0x0044 NDFC Read Data Status Control Register(Default Value: 0x0100_0000)

Offset: 0x0044			Register Name: NDFC_RDATA_STA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable to count the number of bit 1 and bit 0 during current read operation 1: Enable to count the number of bit 1 and bit 0 during current read operation The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:19	/	/	/
18:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status If the number of bit 1 during current read operation is less than or equal to threshold value, the bit 13 of NDFC_ST register will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the bit 12 of NDFC_ST register will be set.

5.2.6.18. 0x0048 NDFC Read Data Status Register 0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: NDFC_RDATA_STA_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

5.2.6.19. 0x004C NDFC Read Data Status Register 1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

5.2.6.20. 0x0050+N*0x04 NDFC Error Counter Register N(Default Value: 0x0000_0000)

Offset: 0x0050+N*0x04(N=0~7)			Register Name: NDFC_ERR_CNT_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[8M+7: 8M] (M=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[N*0x04+M] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits ..... 01010000 : 80 corrected bits Others: Reserved **Note: 1 ECC Data Block =1024 bytes**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.6.21. 0x0070+N*0x04 NDFC User Data Length Register N(Default Value: 0x0000_0000)

Offset: 0x0070+N*0x04(N=0~3)			Register Name: NDFC_USER_DATA_LEN_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[4M+3 : 4M] (M=0~7)	R/W	0x0	It's used to indicate user data's length of ECC DATA BLOCK[0x08*N+M]. 0000 : no user data 0001 : 4 bytes user data 0010 : 8 bytes user data 0011 : 12 bytes user data 0100 : 16 bytes user data 0101 : 20 bytes user data 0110 : 24 bytes user data 0111 : 28 bytes user data 1000 : 32 bytes user data Other : reserved

5.2.6.22. 0x0080 + N*0x04 NDFC User Data Register N(Default Value: 0xFFFF_FFFF)

Offset: 0x0080 + N*0x04(N=0~31)			Register Name: NDFC_USER_DATA_N
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xffffffff	USER_DATA All of the user data in one page is stored in NDFC_USER_DATA_N. The start register address of each ECC DATA BLOCK's user data is determined by its length configured in NDFC_USER_DATA_LEN_N. For example: ECC DATA BLOCK[0] user data len = 8 Bytes, address = 0x80 ECC DATA BLOCK[1] user data len = 0 Bytes, ECC DATA BLOCK[2] user data len = 4 Bytes, address = 0x80+8 ECC DATA BLOCK[3] user data len = 4 Bytes, address = 0x80+8+4 ECC DATA BLOCK[4] user data len = 0 Bytes ECC DATA BLOCK[5] user data len = 16 Bytes, address = 0x80+8+4+4 ECC DATA BLOCK[6] user data len = 0 Bytes ECC DATA BLOCK[7] user data len = 0 Bytes

5.2.6.23. 0x110 NDFC EFNAND Status Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The status value for EF-NAND page read operation

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.6.24. 0x0114 NDFC Spare Area Register(Default Value: 0x0000_0400)

Offset: 0x0114			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

5.2.6.25. 0x0118 NDFC Pattern ID Register(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
n (n=0~31)	R	0x0	PAT_ID Special Pattern ID for ECC data block[n] 0: All 0x00 is found 1: All 0xFF is found

5.2.6.26. 0x011C NDFC DDR2 Specific Control Register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: NDFC_DDR2_SPEC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DLEN_WR The number of latency DQS cycle for write 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
11:8	R/W	0x0	DLEN_RD The number of latency DQS cycle for read 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
7:3	/	/	/
2	R/W	0x0	EN_RE_C Enable the complementary RE# signal 0: Disable 1: Enable
1	R/W	0x0	EN_DQS_C Enable the complementary DQS signal

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
0	/	/	/

5.2.6.27. 0x0120 NDFC Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0120			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	DMA_ACT_STA 00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	DMA_ACK_EN 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	DELAY_CYCLE The counts of hold cycles from DMA last signal high to dma_active high

5.2.6.28. 0x0200 NDFC MBUS DMA Descriptor List Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: NDFC_MDMA_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_DESC_BASE_ADDR Start Address of Descriptor List Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the DMA internally. Hence these LSB bits are read-only.

5.2.6.29. 0x0204 NDFC MBUS DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: NDFC_MDMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_FINISH_INT Transfer Finish Interrupt Indicates that data transmission is finished for a descriptor. Writing a ‘1’ clears this bit. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.6.30. 0x0208 NDFC MBUS DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: NDFC_DMA_INT_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_INT_ENB Transfer Interrupt Enable When set, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

5.2.6.31. 0x020C NDFC MBUS DMA Current Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: NDFC_MDMA_CUR_DESC_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_DESC_ADDR Current Descriptor Address Pointer Cleared on reset. Pointer updated by DMA during operation. This register points to the start address of the current descriptor read by the DMA.

5.2.6.32. 0x0210 NDFC MBUS DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: NDFC_MDMA_CUR_BUF_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_BUFF_ADDR Current Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation. This register points to the current Data Buffer Address being accessed by the DMA.

5.2.6.33. 0x0214 NDFC DMA Byte Counter Register(Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: NDFC_DMA_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	DMA_CNT DMA data counter, including MBUS DMA and Normal DMA

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.6.34. 0x0300 NDFC IO Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/Write data into internal RAM Access unit is 32-bit.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3. SD/MMC Host Controller (SMHC)

5.3.1. Overview

The SD-MMC Host Controller(SMHC) controls the read/write operations on the secure digital(SD) card and multimedia card(MMC), and supports various extended devices based on the secure digital input/output(SDIO) protocol. The A133 provides three SMHC interfacs for controlling the SD card, MMC and SDIO device.

The SMHC has the following features:

- Supports eMMC boot operation
- Supports command completion signal and interrupt to host processor and command completion signal disable feature
- SMHC0 supports SD (Version1.0 to 3.0), 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 100 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC1 supports SDIO (Version1.1 to 3.0), 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 100 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC2 supports MMC (Version3.3 to 5.1), 8-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- Hardware CRC generation and error detection
- Programmable baud rate
- Host pull-up control
- Supports SDIO interrupt in 1-bit and 4-bit modes
- Block size of 1 to 65535 bytes
- Descriptor-based internal DMA controller
- Internal 1 KB FIFO for data transfer

5.3.2. Block Diagram

Figure 5-17 shows a block diagram of the SMHC.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

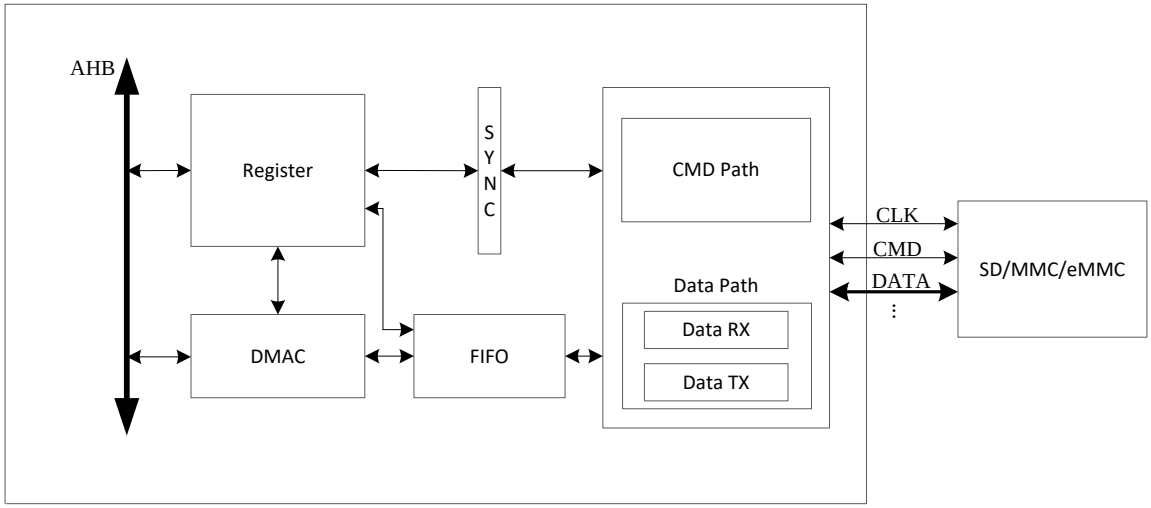


Figure 5- 17. SMHC Block Diagram

5.3.3. Operations and Functional Descriptions

5.3.3.1. External Signals

Table 5-3 describes the external signals of SMHC.

Table 5- 3. SMHC External Signals

Port Name	Width	Type	Description
SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	1	I/O,OD	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	1	I/O,OD	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	1	O	Clock output for MMC
SDC2_CMD	1	I/O,OD	CMD line for MMC
SDC2_D[i] (i=0~7)	8	I/O	Data line for MMC
SDC2_RST	1	O	Reset signal for MMC
SDC2_DS	1	I	Data strobe for MMC

5.3.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 5-4 describes the clock sources of SMHC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 5- 4. SMHC Clock Sources

Clock Sources	Description
OSC24M	24 MHz Crystal
PLL_PERI0(2X)	Peripheral Clock, the default value is 1.2 GHz
PLL_PERI1(2X)	Peripheral Clock, the default value is 1.2 GHz

5.3.3.3. Timing Diagram

Please refer to relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card(eMMC) Electrical Standard(5.0)

5.3.3.4. Internal DMA Controller Description

SMHC has an internal DMA controller (IDMAC) to transfer data between host memory and SMHC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.3.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

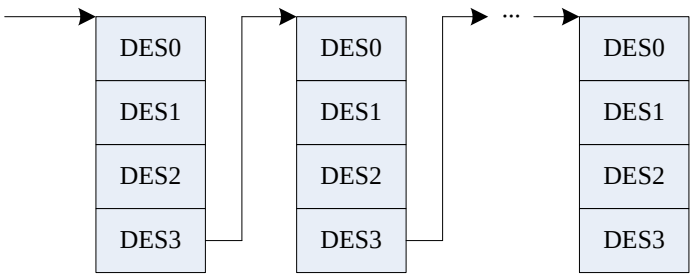


Figure 5- 18. IDMAC Descriptor Structure Diagram

This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

5.3.3.4.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set to 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer.
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor.
0	/	/

5.3.3.4.3. DES1 Definition

Bits	Name	Descriptor
31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

5.3.3.4.4. DES2 Definition

Bits	Name	Descriptor

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. It is a word address.

5.3.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present. It is a word address.

5.3.3.5. Calibrate Delay Chain

There are two delay chains in SMHC v5.30. One is Data Strobe delay chain, used to generate delay to make proper timing between Data Strobe and data signals. Another is sample delay chain, used to generate delay to make proper timing between internal card clock signal and data signals. Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **SMHC Bus Gating Reset Register** and **SMHC0/1/2 Clock Register**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(CCU). Calibration delay chain is an internal function in SMHC and does not need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200 MHz.

Step3: Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain**(bit[5:0]). Then write 0x0 to **delay control register** to clear the value.

Step4: Write 0x8000 to **delay control register** to start calibrate delay chain.

Step5: Wait until the flag(bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of SMHC clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SMHC clock and the result of calibration.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.4. Programming Guidelines

5.3.4.1. Initialization

Before data and command are exchanged between a card and the SMHC, the SMHC need to be initialized. The SMHC is initialized as follows.

Step1: Configure GPIO register as SMHC function by Port Controller module; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST], open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING]; select clock sources and set division factor by configuring the SMHCx_CLK_REG(x=0,1,2) register.

Step2: Configure SMHC_CTRL to reset FIFO and controller, enable total interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupt and error abnormal interrupt, and register interrupt function.

Step3: Configure SMHC_CLKDIV to open clock for device; configure SMHC_CMD as change clock command(for example 0x80202000); send update clock command to deliver clock to device.

Step4: Configure SMHC_CMD to normal command, configure SMHC_CMDARG to set command parameter, configure SMHC_CMD to set response type, etc, then command can send. According to initial process in the protocol, you can finish SMHC initializing by sending corresponding command one by one.

5.3.4.2. Writing a Single Data Block

To Write a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write 0x82 to SMHC_IDMAC to enable IDMAC interrupt, configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 1 data block to the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD24(Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, send CMD24 command to write data to device.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD24 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status, then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.4.3. Reading a Single Data Block

To read a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 1 data block from the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD17 command(Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, send CMD17 command to read data from device to DRAM/SRAM.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD17 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.4. Writing Open-ended Multiple Data Blocks(CMD25+Auto CMD12)

To write open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks to the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25 command(Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, send CMD25 command to write data to device, when data transfer is complete, CMD12 will be sent automatically .

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.3.4.5. Reading Open-ended Multiple Data Blocks(CMD18+Auto CMD12)

To read open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks from the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18 command(Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, send CMD18 command to read data to device, when data transfer is complete, CMD12 will be sent automatically.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD18 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.6. Writing Pre-defined Multiple Data Blocks(CMD23+CMD25)

To write pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks, setting SMHC_CMDARG to 0x3 to ensure the block number to be operated, writing 0x80000157 to SMHC_CMD to send CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25 command(Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, send CMD25 command to write data to device.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step8: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.3.4.7. Reading Pre-defined Multiple Data Blocks(CMD23+CMD18)

To read pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks, setting SMHC_CMDARG to 0x3 to ensure the block number to be operated, writing 0x80000157 to SMHC_CMD to send CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, send CMD18 command to read data from device to DRAM/SRAM.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD18 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.5. Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2	0x04022000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_DBGC	0x0050	Current Debug Control Register
SMHC_CSDC	0x0054	CRC Status Detect Control Registers
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_IDMAC	0x0080	IDMAC Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	IDMAC Status Register
SMHC_IDIE	0x008C	IDMAC Interrupt Enable Register
SMHC_THLD	0x0100	Card Threshold Control Register
SMHC_SFC	0x0104	Sample FIFO Control Register
SMHC_A23A	0x0108	Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_EXT_CMD	0x0138	Extended Command Register
SMHC_EXT_RESP	0x013C	Extended Response Register
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_HS400_DL	0x014C	HS400 Delay Control Register
SMHC_FIFO	0x0200	Read/Write FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.6. Register Description

5.3.6.1. 0x0000 SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit is used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit is used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

5.3.6.2. 0x0004 SMHC Clock Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SMHC_CLKDIV**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM is in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

5.3.6.3. 0x0008 SMHC Timeout Register(Default Value:0xFFFF_FF40)

Offset: 0x0008			**Register Name: SMHC_TMOUT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data,data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18), a next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host writes data, the value is no effect.
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

5.3.6.4. 0x000C SMHC Bus Width Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

5.3.6.5. 0x0010 SMHC Block Size Register(Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

5.3.6.6. 0x0014 SMHC Byte Count Register(Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.6.7. 0x0018 SMHC Command Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge When software sets this bit along in mandatory boot operation, the controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send *Stop* or *Abort* command to stop current data transfer in

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the **SMHC_RESP1** will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1: Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without response 1: Command with response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

5.3.6.8. 0x001C SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SMHC_CMDARG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.6.9. 0x0020 SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

5.3.6.10. 0x0024 SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

5.3.6.11. 0x0028 SMHC Response 2 Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

5.3.6.12. 0x002C SMHC Response 3 Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

5.3.6.13. 0x0030 SMHC Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

5.3.6.14. 0x0034 SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			**Register Name: SMHC_MINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	M_CARD_REMOVAL_INT Card Removed

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30	R	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/Busy Clear When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

5.3.6.15. 0x0038 SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/Busy Clear When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host does not find start bit on data0. This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

5.3.6.16. 0x003C SMHC Status Register(Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card Data Busy Inverted version of DATA[0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data[3] Status Level of DATA[3], checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO did not reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO RX Water Level Flag 0: FIFO did not reach receive trigger level 1: FIFO reached receive trigger level

5.3.6.17. 0x0040 SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040			**Register Name: SMHC_FIFOTH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved It should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) FIFO_DEPTH = 256, FIFO_SIZE = 256 * 32 = 1K

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Recommended: MSize = 16, TX_TL = 240, RX_TL = 15 (for SMHC2) MSize = 8, TX_TL = 248, RX_TL = 7 (for SMHC0,SMHC1)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15, for SMHC2) 7 (means greater than 7, for SMHC0,SMHC1)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: No trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240, for SMHC2) 248(means less than or equal to 248, for SMHC0,SMHC1)

5.3.6.18. 0x0044 SMHC Function Select Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller resets to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

5.3.6.19. 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.6.20. 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.6.21. 0x0054 SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode Others: Reserved

5.3.6.22. 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A Auto CMD12 Argument SD_A12A set the argument of command 12 automatically send by controller.

5.3.6.23. 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear the input phase of command lines and data lines during update clock operation. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Clear the input phase of data lines before receive CRC status. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Clear the input phase of data lines before transfer data. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Clear the input phase of data lines before receive data. 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command rx phase before send command. 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0(only for SD2 hs400 mode)
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAMPLE_EN 0: Disable hs400 new sample method 1: Enable hs400 new sample method

5.3.6.24. 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

5.3.6.25. 0x0080 SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make IDMAC refetch descriptor again and do the transfer normally.
30:11	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable When set, the IDMAC is enabled.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

5.3.6.26. 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List Contains the base address of the First Descriptor. It is a word(4 Byte) address.

5.3.6.27. 0x0088 SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	IDMAC_ERR_STA Error Bits Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved The bit is read-only.
9	R/W1C	0x0	ABN_INT_SUM(AIS) Abnormal Interrupt Summary Logical OR of the following:

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: Descriptor Unavailable Bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM(NIS) Normal Interrupt Summary Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt Indicates that data transmission is finished for a descriptor.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Writing a '1' clears this bit.

5.3.6.28. 0x008C SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt Summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

5.3.6.29. 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_WR_THLD Card Read/Write Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable(HS400) 0: Card write threshold disabled 1: Card write threshold enabled

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy clear interrupt disabled 1: Busy clear interrupt enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card read threshold disabled 1: Card read threshold enabled Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO.

5.3.6.30. 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be changed between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation. The value increases one in this field is linked to one cycle(two cycles in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

5.3.6.31. 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.6.32. 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

5.3.6.33. 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When setting this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST is set, this field will be cleared.

5.3.6.34. 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.6.35. 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4/HS400 mode 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR8 mode, 0^0 at DDR4/HS400 mode
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4/HS400 mode 1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4/HS400 mode
15:0	/	/	/

5.3.6.36. 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW.
6	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data line. It can be determined according to the value of SAMP_DL, the cycle of card clock and the input timing requirement of the device.

5.3.6.37. 0x0148 SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

5.3.6.38. 0x014C SMHC HS400 New Timing Delay Control Register(Default Value: 0x0000_8000)

Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	HS400_DL_CAL_START HS400 Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	HS400_DL_CAL_DONE HS400 Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in HS400_DL.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

13:12	/	/	/
11:8	R	0x8	HS400_DL HS400 Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC clock nearly. This bit is valid only when HS400_DL_CAL_DONE is set.
7	R/W	0x0	HS400_DL_SW_EN Sample Delay Software Enable
6	/	/	/
3:0	R/W	0x0	HS400_DL_SW HS400 Delay Software

5.3.6.39. 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 6 Video Output Interfaces....422
6.1. TCON_LCD....422
6.1.1. Overview....422
6.1.2. Block Diagram....422
6.1.3. Operations and Functional Descriptions....423
6.1.4. Programming Guidelines....433
6.1.5. Register List....439
6.1.6. Register Description....440
6.2. DSI....465
6.2.1. Overview....465
6.2.2. Block Diagram....466
6.2.3. Operations and Functional Descriptions....467
6.2.4. Programming Guidelines....474
6.2.5. Register List....475
6.2.6. Registers Description....477

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 6- 1. TCON_LCD Block Diagram 422
Figure 6- 2. HV Interface Vertical Timing 426
Figure 6- 3. HV Interface Horizontal Timing 427
Figure 6- 4. i8080 Interface Timing 429
Figure 6- 5. LVDS Single Link JEDIA Mode Interface Timing 430
Figure 6- 6. LVDS Single Link NS Mode Interface Timing 430
Figure 6- 7. LVDS Dual Link NS Mode Interface Timing 431
Figure 6- 8. CMAP Module 433
Figure 6- 9. FRM Module 433
Figure 6- 10. HV Mode Initial Process 434
Figure 6- 11. LVDS Mode Configuration Process 436
Figure 6- 12. i8080 Mode Initial Process 438
Figure 6- 13. MIPI DSI Video Mode Data Timing 439
Figure 6- 14. MIPI DSI System Block Diagram 466
Figure 6- 15. MIPI DSI Internal Unit 466
Figure 6- 16. DPHY Block Diagram 467
Figure 6- 17. MIPI DSI Clock System 468
Figure 6- 18. DPHY SOT and EOT Timing 472
Figure 6- 19. DPHY Escape Mode Timing 473
Figure 6- 20. Switching Between HS and LP Timing 473
Figure 6- 21. Video Mode Initial Sequence 474
Figure 6- 22. Command Mode Initial Sequence 475

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 6- 1. LCD External Signals 423
Table 6- 2. HV Panel Signals 425
Table 6- 3. BT656 Panel Signals 427
Table 6- 4. EAV and SAV Sequence 428
Table 6- 5. CPU Panel Signals 428
Table 6- 6. LVDS Panel Signals 429
Table 6- 7. TCON_LCD Clock Sources 431
Table 6- 8. RGB Gamma Correction 432
Table 6- 9. MIPI DSI External Signals 467
Table 6- 10. MIPI DSI Controller Clock Sources 468
Table 6- 11. MIPI D-PHY Clock Source 468
Table 6- 12. Escape Entry Codes 469
Table 6- 13. Data Types for Processor-sourced Packets 469
Table 6- 14. Complete Set of Peripheral-to-Processor Data Types 470
Table 6- 15. Error Report Bit Definitions 471
Table 6- 16. D-PHY Lane State 471
Table 6- 17. Entry Command 472

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 6 Video Output Interfaces

6.1. TCON_LCD

6.1.1. Overview

The TCON_LCD (Timing Controller_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- RGB interface with DE/SYNC mode, up to 1280x720@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- LVDS interface with dual link, up to 1920 x 1200@60fps
- LVDS interface with single link, up to 1366 x 768@60fps
- i8080 interface, up to 800 x 480@60fps
- BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

6.1.2. Block Diagram

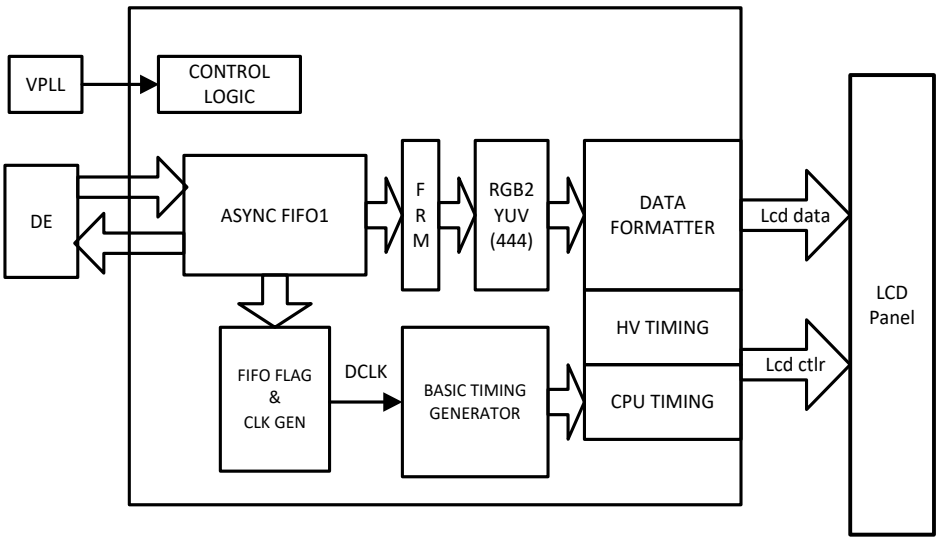


Figure 6- 1. TCON_LCD Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.3. Operations and Functional Descriptions

6.1.3.1. External Signals

The LCD external signals are used to connect to panel interface. The panel interface has various types.

Table 6- 1. LCD External Signals

External Signal	Description	Type
LCD0_D[7:2],LCD0_D[15:10],LCD0_D[23:18]	LCD data bit	O
LCD0_CLK	LCD clock signal	O
LCD0_DE	LCD data enable	O
LCD0_HSYNC	LCD horizontal sync	O
LCD0_VSYNC	LCD vertical sync	O

6.1.3.1.1. Control Signal and Data Port Mapping

	SYNC RGB					CPU cmd	CPU 18bit	CPU 16bit								CPU 8bit					CPU 9bit	
I/O	Parallel RGB	Serial RGB			CCIR656		256K	256K							65K	256K			65K		256K	
		1st	2nd	3rd				1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd
IO0	VSYNC					CS																
IO1	HSYNC					RD																
IO2	DCLK					WR																
IO3	DE					RS																
D23	R7			CKN		D23	R5	R5	B5	G5	R5		R5	B5	R4							
D22	R6			CKP		D22	R4	R4	B4	G4	R4		R4	B4	R3							
D21	R5					D21	R3	R3	B3	G3	R3		R3	B3	R2							
D20	R4					D20	R2	R2	B2	G2	R2		R2	B2	R1							
D19	R3					D19	R1	R1	B1	G1	R1		R1	B1	R0							
D18	R2					D18	R0	R0	B0	G0	R0		R0	B0	G5							
D17	R1					D17																
D16	R0					D16																
D15	G7					D15	G5								G4							
D14	G6					D14	G4								G3							
D13	G5					D13	G3															
D12	G4	D17	D27	D37	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2
D11	G3	D16	D26	D36	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1
D10	G2	D15	D25	D35	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0
D9	G1					D9																
D8	G0					D8																
D7	B7	D14	D24	D34	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5
D6	B6	D13	D23	D33	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

D5	B5	D12	D22	D32	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3
D4	B4	D11	D21	D31	D1	D4	B2								B1				G4	B1	G5	B2
D3	B3	D10	D20	D30	D0	D3	B1								B0				G3	B0	G4	B1
D2	B2					D2	B0														G3	B0
D1	B1					D1																
D0	B0					D0																

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

LCD I/O	**Parallel RGB**	
	RGB565	**RGB666**
LCD0_D23	R4	R5
LCD0_D22	R3	R4
LCD0_D21	R2	R3
LCD0_D20	R1	R2
LCD0_D19	R0	R1
LCD0_D18	-	R0
LCD0_D15	G5	G5
LCD0_D14	G4	G4
LCD0_D13	G3	G3
LCD0_D12	G2	G2
LCD0_D11	G1	G1
LCD0_D10	G0	G0
LCD0_D7	B4	B5
LCD0_D6	B3	B4
LCD0_D5	B2	B3
LCD0_D4	B1	B2
LCD0_D3	B0	B1
LCD0_D2	-	B0

The multiplex relationship between LCD I/O and LVDS is shown as follows.

LCD0_DE	LVDS1_D3N
LCD0_CLK	LVDS1_D3P
LCD0_D23	LVDS1_CKN
LCD0_D22	LVDS1_CKP
LCD0_D21	LVDS1_D2N
LCD0_D20	LVDS1_D2P
LCD0_D19	LVDS1_D1N
LCD0_D18	LVDS1_D1P
LCD0_D15	LVDS1_D0N
LCD0_D14	LVDS1_D0P
LCD0_D13	LVDS0_D3N
LCD0_D12	LVDS0_D3P

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

LCD0_D11	LVDS0_CKN
LCD0_D10	LVDS0_CKP
LCD0_D7	LVDS0_D2N
LCD0_D6	LVDS0_D2P
LCD0_D5	LVDS0_D1N
LCD0_D4	LVDS0_D1P
LCD0_D3	LVDS0_D0N
LCD0_D2	LVDS0_D0P

6.1.3.1.2. HV Interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 application.

Table 6- 2. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

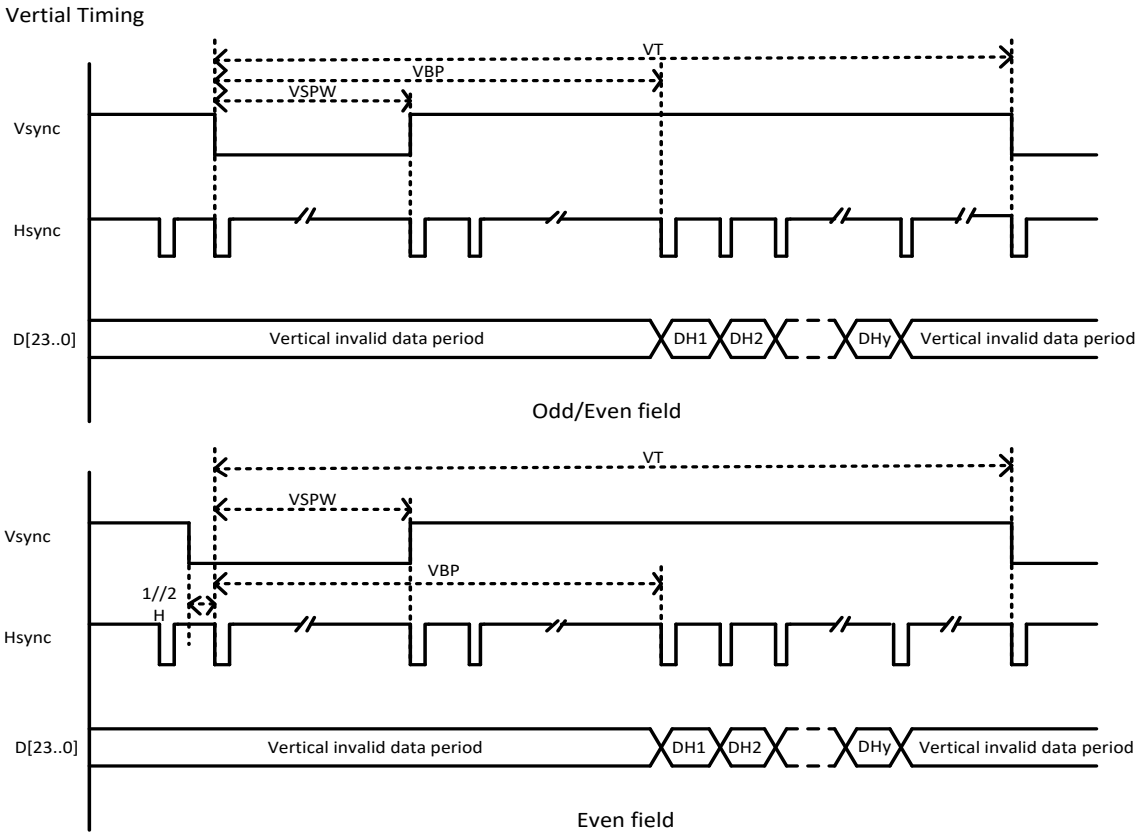


Figure 6- 2. HV Interface Vertical Timing

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

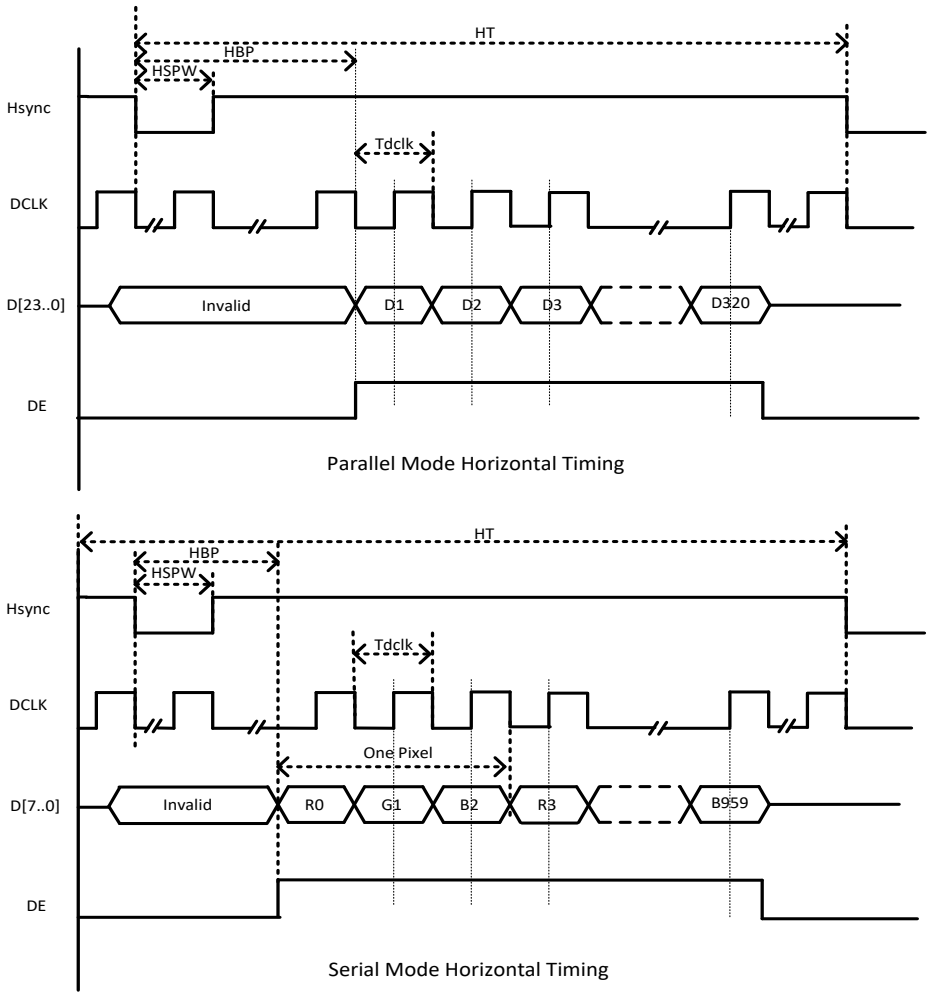


Figure 6- 3. HV Interface Horizontal Timing

6.1.3.1.3. BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 6- 3. BT656 Panel Signals

Signal	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

Where ⊕ represents the exclusive-OR function

The 4 byte SAV/EAV sequence is as follows.

Table 6- 4. EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9(MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

6.1.3.1.4. i8080 Interface

i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. CPU control signals are active low.

Table 6- 5. CPU Panel Signals

Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180° delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

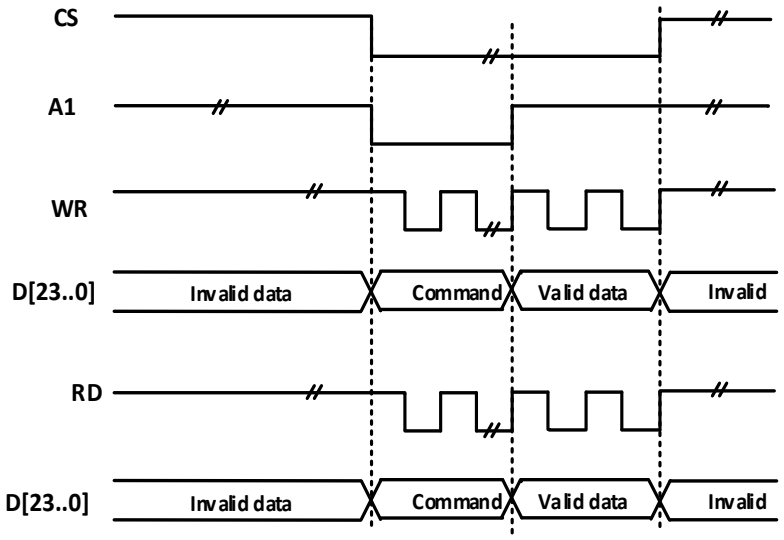


Figure 6- 4. i8080 Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

6.1.3.1.5. LVDS Interface

Table 6- 6. LVDS Panel Signals

External Signal	Description	Type
CKP	The positive port of clock	O
CKN	The negative port of clock	O
D0P	The positive port of data channel 0	O
D0N	The negative port of data channel 0	O
D1P	The positive port of data channel 1	O
D1N	The negative port of data channel 1	O
D2P	The positive port of data channel 2	O
D2N	The negative port of data channel 2	O
D3P	The positive port of data channel 3	O
D3N	The negative port of data channel 3	O

The following figures show the timing of LVDS interface.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

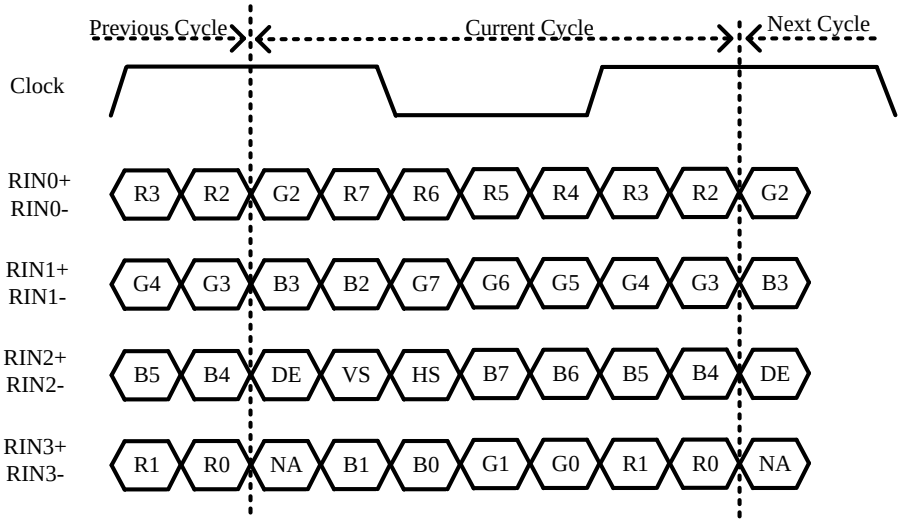


Figure 6- 5. LVDS Single Link JEDIA Mode Interface Timing

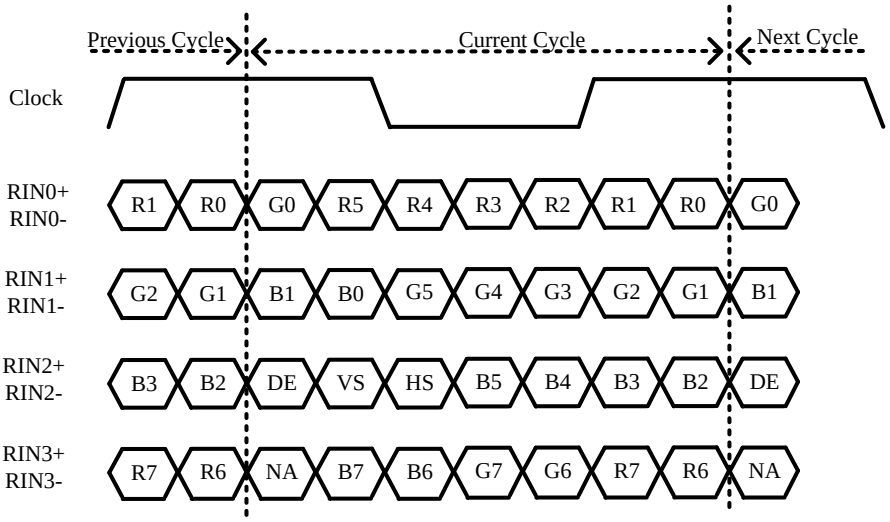


Figure 6- 6. LVDS Single Link NS Mode Interface Timing

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

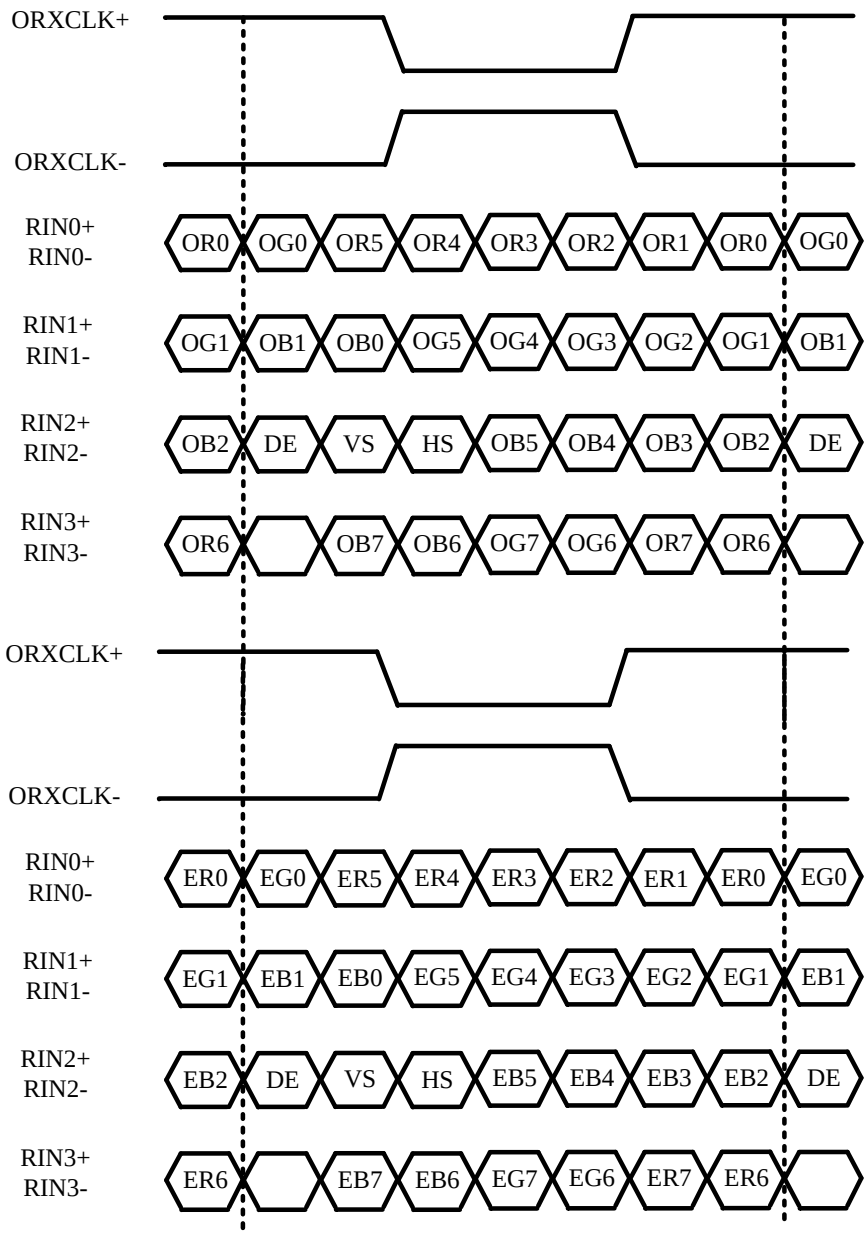


Figure 6- 7. LVDS Dual Link NS Mode Interface Timing

6.1.3.2. Clock Sources

The following table describes the clock sources of TCON_LCD. Table 6-7 describes the clock sources of TCON_LCD.

Table 6- 7. TCON_LCD Clock Sources

Clock Sources	Description
PLL_VIDEO0(4X)	Video PLL Clock, and the default value is 1188 MHz
PLL_VIDEO1(4X)	Video PLL Clock, and the default value is 1188 MHz
PLL_VIDEO2(4X)	Video PLL Clock, and the default value is 1188 MHz
PLL_VIDEO3(4X)	Video PLL Clock, and the default value is 1188 MHz

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PLL_PERI0(2X)	PERI0 PLL Clock, and the default value is 1.2 GHz

6.1.3.3. RGB Gamma Correction

Function: This module correct the RGB input data of DE.

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 6- 8. RGB Gamma Correction

Offset	Value
0x400	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

6.1.3.4. CEU Module

This module enhances color data from DE.

R' = Rr*R + Rg*G + Rb*B + Rc

G' = Gr*R + Gg*G + Gb*B + Gc

B' = Br*R + Bg*G + Bb*B + Bc

NOTE

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

Rc, Gc, Bc s19 (-16384, 16384)

R, G, B u8 [0-255]

R' has the range of [Rmin ,Rmax]

G' has the range of [Rmin ,Rmax]

B' has the range of [Rmin ,Rmax]

6.1.3.5. CMAP Module

Function: This module map color data from DE.

Every 4 input pixels are as a unit. A unit is divided into 12 bytes. The output byte can select one of those 12 bytes. Note that even line and odd line can be different, and the output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

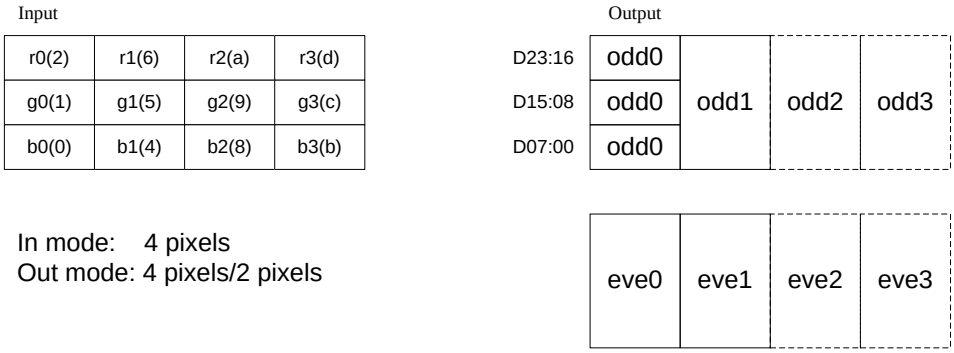


Figure 6- 8. CMAP Module

6.1.3.6. FRM Module

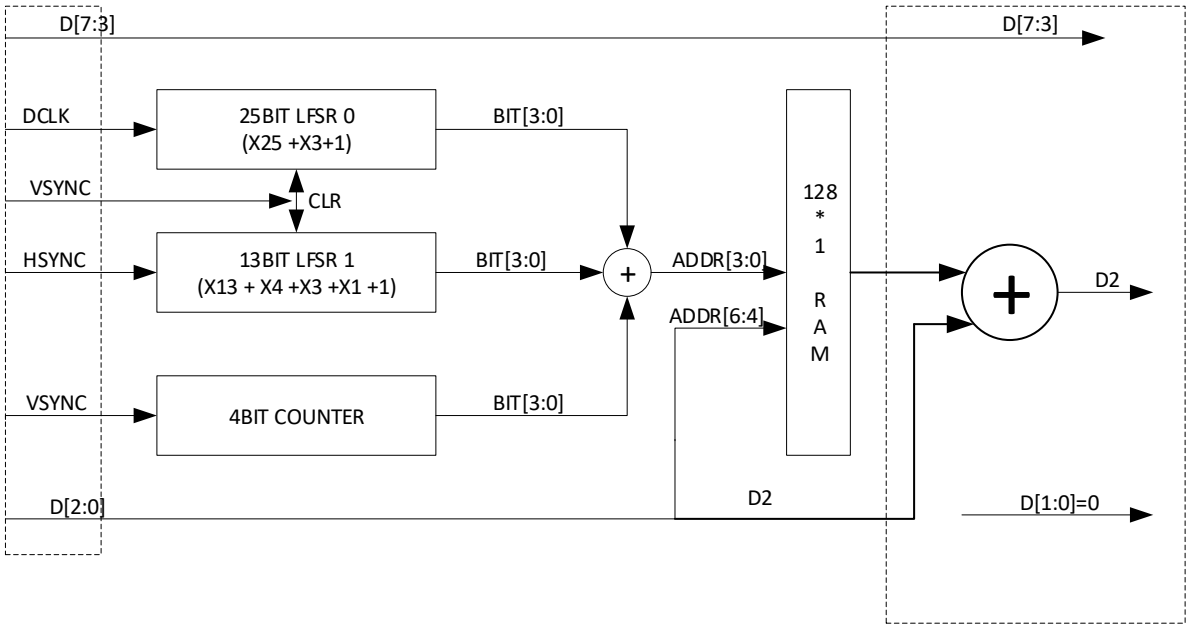


Figure 6- 9. FRM Module

6.1.4. Programming Guidelines

6.1.4.1. HV Mode Configuration Process

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

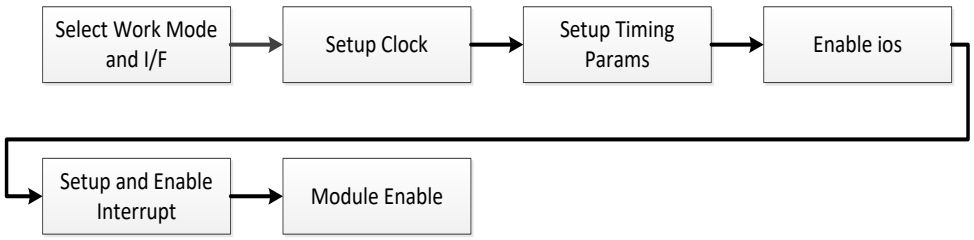


Figure 6- 10. HV Mode Initial Process

(1) Parallel RGB

Step1: **Select HV interface type**

Configure LCD_CTL_REG[LCD_IF](reg0x40) to 0 to select HV(Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE](reg0x58) to 0 to select 24bit/1cycle parallel mode.

```
lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);
lcd_dev[sel]->lcd_ctl.src_sel = src;      //src = DE/color/grayscale/...
lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24-bit/1cycle parallel mode;
```

Step2: **Clock configuration**

NOTE

- **In parallel RGB mode, the displayed pixel clock(pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.**
- **When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL(reg0x88) selects dclk0~2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.**

Configure corresponding frequency by setting PLL_VIDEO0/1/2/3 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV].If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

```
lcd_dev[sel]->lcd_dclk.dclk_en = en;
lcd_dev[sel]->lcd_dclk.dclk_div = div;
```

Step3: **Set sequence parameters**

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG in reg0x48~0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASE2_REG.VT needs be set to the twice of the actual value.

```
lcd_dev[sel]->lcd_basic0.x = x-1;
lcd_dev[sel]->lcd_basic0.y = y-1;
lcd_dev[sel]->lcd_basic1.ht = ht-1;
lcd_dev[sel]->lcd_basic1.hbp = hbp-1;
lcd_dev[sel]->lcd_basic2.vt = vt*2;
lcd_dev[sel]->lcd_basic2.vbp = vbp-1;
lcd_dev[sel]->lcd_basic3.hspw = hspw-1;
lcd_dev[sel]->lcd_basic3.vspw = vspw-1;
```

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step4: **Open IO output**

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG(reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0~3_INV(reg0x88).

Step5: **Set and open interrupt function**

The LCD_GINT0_REG(reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG(reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step6: **Open module enable**

Enable LCD_CTL_REG.LCD_EN(reg0x40) and LCD_GCTL_REG.LCD_EN(reg0x00).

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

(2) Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step1: **Select HV interface type**

Set LCD_CTL_REG.LCD_IF(reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE(reg0x58) to select 8bit/3cycle RGB serial mode(RGB888), 8bit/4cycle Dummy RGB mode(DRGB) or 8bit/4cycle RGB Dummy mode(RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

Step2、**Step3**: In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASE2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.4.2. LVDS Mode Configuration Process

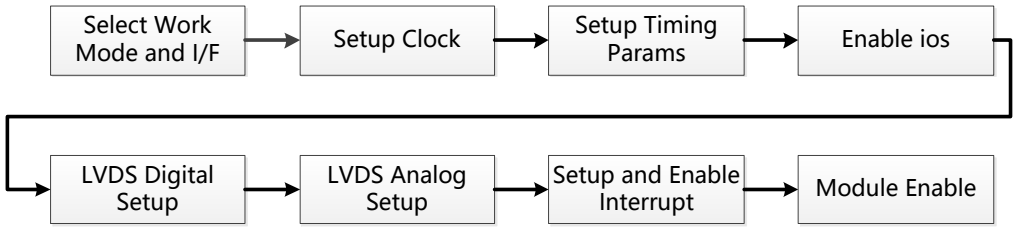


Figure 6- 11. LVDS Mode Configuration Process

The LVDS interface configuration process is similar to the parallel mode of HV mode, and adds the digital/analog configuration of LVDS interface.

Step1: **Same as in step1 of parallel mode**

Step2: **Clock configuration**

NOTE

In parallel mode, the displayed pixel clock(pixel_CLK) is required to be consistent with the DCLK, pixel_clk=Ht*Vt*frame rate.

- Configure LCD_DCLK_REG.LCD_DCLK_DIV(reg0x44) to 7 after DCLK is determined;
- Configure the PLL clock in CCU based on proportional relationship;
- Release the LVDS reset of TCON_LCD_BGR_REG;
- Other configurations remain unchanged.

  lcd_dev[sel]->lcd_dclk.dclk_en = en;

  lcd_dev[sel]->lcd_dclk.dclk_div = 7;

Step3: **Same as in step3 of parallel mode**

Step4: **Same as in step4 of parallel mode**

Step5: **LVDS digital logic configuration**

Includes clock source select of module, LVDS link number, data mode and bit width configuration.

- Configure LCD_LVDS_IF_REG.LCD_LVDS_CLK_SEL(reg0x84) to set LCD CLK;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_LINK to set the required LVDS port number;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_MODE to set JEDIA and NS mode;
- Configure LCD_LVDS_IF_REG.LCD_LVDS_BITWIDTH to select 24-bit or 18-bit width;
- Lastly configure LCD_LVDS_IF_REG.LCD_LVDS_EN to start LVDS mode.

  lcd_dev[sel]->lcd_lvds_ctl.lvds_link = link_num-1;

  lcd_dev[sel]->lcd_lvds_ctl.lvds_mode = mode;

  lcd_dev[sel]->lcd_lvds_ctl.lvds_bitwidth = bitwidth;

  lcd_dev[sel]->lcd_lvds_ctl.lvds_clk_sel = clk_src;

  lcd_dev[sel]->lcd_lvds_ctl.lvds_en = 1;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

NOTE

If configuring the same source data output mode of dual link, except the reg0x84 register of TCON_LCD0 needs be configured, the LCD_LVDS_IF_REG.LCD_LVDS_CLK_SEL, LCD_LVDS_IF_REG.LCD_LVDS_LINK, LCD_LVDS_IF_REG.LCD_LVDS_MODE, and LCD_LVDS_IF_REG.LCD_LVDS_BITWIDTH of the reg0x244 register need be configured.

Step6: **LVDS controller configuration**

NOTE

The TCON LCD0 PHY0 is controlled by COMBO_PHY_REG(reg0x1110, reg0x1114). The TCON LCD0 PHY1 is controlled by LCD_LVDS0_ANA_REG(reg0x220).

For PHY0:

- Configure the reg_verf1p6(differential mode voltage) in reg0x1114 to 4;
- Configure the reg_vref0p8 reg0x1114(common mode voltage) in reg0x1114 to 3;
- Start en_cp, en_mipi, en_lvds, and en_comboldo in reg0x1110, in turn.

For PHY1:

The LVDS analog configuration process is to start clock and data channel, and set the common mode and differential mode voltage, and start module power.

- Configure LVDS_HPREN_DRVC and LVDS_HPREN_DRV. When LVDS signal is 18-bit, LVDS_HPREN_DRV=0x7; when LVDS signal is 24-bit, LVDS_HPREN_DRV=0xF;
- Configure LVDS0_REG_C(differential mode voltage) to 4;
- Configure LVDS0_REG_V(common mode voltage) to 3;
- Lastly, start module voltage, and enable EN_LVDS and EN_24M.

NOTE

When the same source data output of dual link needs be configured, then the LVDS_DUAL_CHANNEL_SRC_SEL needs be configured to 1.

```
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_drvd = 0x7; //18bit=0x7, 24bit=0xf
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_drvc = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.diff_level = diff;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.com_level = com;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.dual_src = link_src;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_24M = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_lvds = 1;
lcd_dev[sel]->lcd_lvds_ana_ctl[lvds_num].bits.en_mb = 1;
```

Step7: **Same as in step5 of parallel mode**

Step8: **Same as in step6 of parallel mode**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.4.3. i8080 Mode Configuration Process

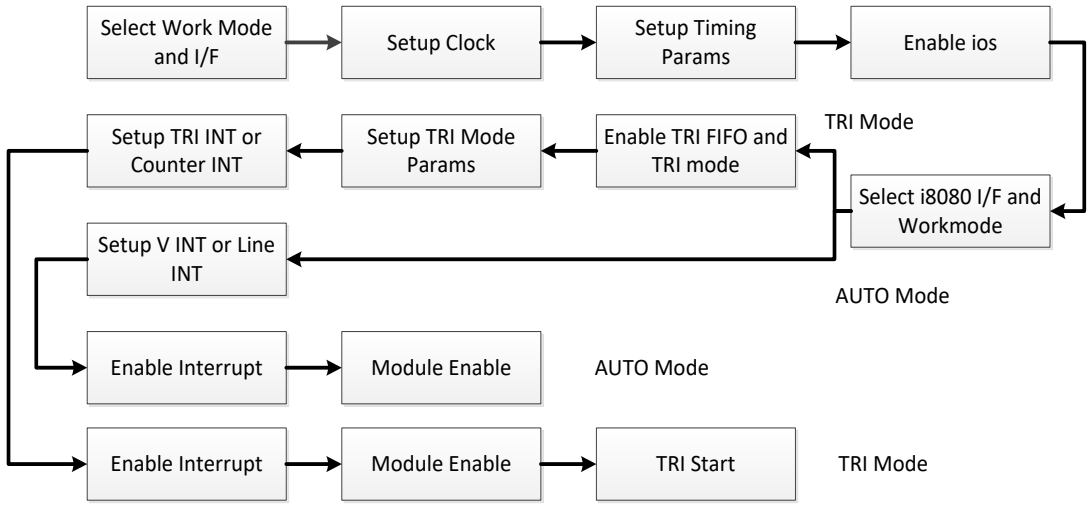


Figure 6- 12. i8080 Mode Initial Process

Step1: Select i8080 interface type.

Step2: The step is the same as HV mode, but pulse adjustment function is invalid.

Step3: The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.

Step4: The step is the same as HV mode.

Step5: Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------**TRI mode**----------

Step6: Open TRI FIFO switch, and TRI mode function.

Step7: Set parameters of TRI mode, including block size, block space and block number.

NOTE

When output interface is parallel mode, then the setting value of block space parameter is not less than 20.
When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.
When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.
When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

Step8: Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.

Step9: Open interrupt total switch.

Step10: Open interrupt total enable.

Step11: Operate tri start operation(the bit1 of LCD_CPU_IF_REG is set to"1").

----------**Auto mode**----------

Step6: Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step7: Open module total enable.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.4.4. MIPI DSI Notes

The requirements on MIPI DSI mode are as follows.

(1). When using MIPI DSI as display interface, the data clk of TCON needs be started firstly.

(2). When it is used with DSI video mode, the setting of block space needs to meet the following relationship.

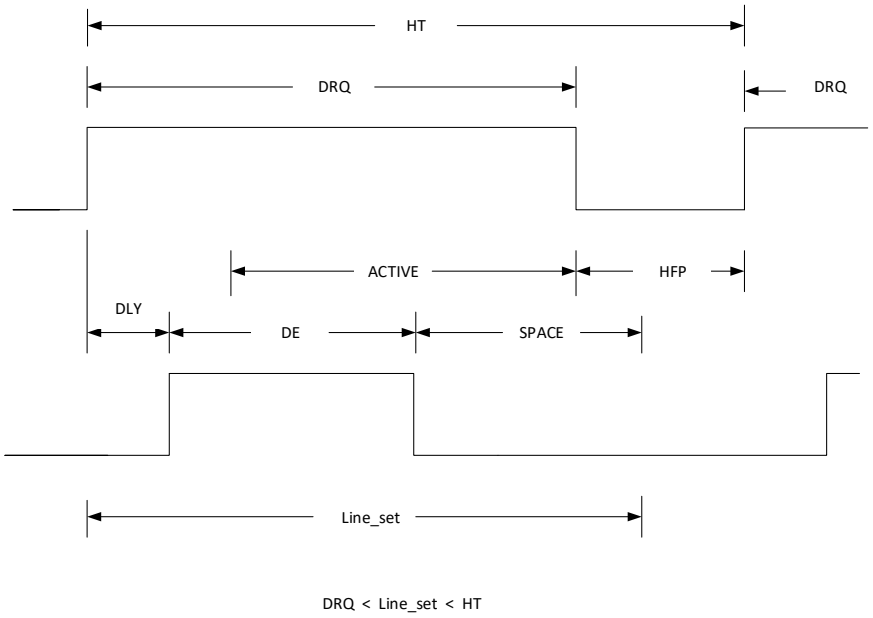


Figure 6- 13. MIPI DSI Video Mode Data Timing

6.1.5. Register List

Module Name	Base Address
TCON_LCD0	0x06511000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04	LCD FRM Seed Register(N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x002C+N*0x04	LCD FRM Table Register(N=0,1,2,3)
LCD_3D_FIFO_REG	0x003C	LCD 3D FIFO Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_LVDS_IF_REG	0x0084	LCD LVDS Configure Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04	LCD CEU Coefficient Register0(N=0~10)
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10	LCD CEU Coefficient Register1(N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04	LCD CEU Coefficient Register2(N=0,1,2)
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_LVDS0_ANA_REG	0x0220	LCD LVDS Analog Register 0
LCD_FSYNC_GEN_DLY_REG	0x0240	Fsync Active Time Register
LCD_GAMMA_TABLE_REG	0x0400-0x07FF	LCD Gamma Table Register

6.1.6. Register Description

6.1.6.1. 0x0000 LCD Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	LCD_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.
29:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.2. 0x0004 LCD Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN 0: Disable 1: Enable Enable the trigger finish interrupt.
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN 0: Disable 1: Enable Enable the trigger counter interrupt.
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 matched the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finished. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reached this value. Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when sync by DSI but not finish. Write 0 to clear it.
8:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.3. 0x0008 LCD Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger(including inactive lines) Setting it for the specified line of trigger0. **Note: SY0 is writable only when LINE_TRG0 is disabled.**
15:0	/	/	/

6.1.6.4. 0x0010 LCD FRM Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN 0:Disable 1:Enable Enable the dither function.
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R 0: 6-bit frm output 1: 5-bit frm output The R component output bits are in dither function.
5	R/W	0x0	LCD_FRM_MODE_G 0: 6-bit frm output 1: 5-bit frm output The G component output bits are in dither function.
4	R/W	0x0	LCD_FRM_MODE_B 0: 6-bit frm output 1: 5-bit frm output The B component output bits are in dither function.
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST 00: FRM 01: half 5-/6-bit, half FRM 10: half 8-bit, half FRM 11: half 8-bit, half 5-/6-bit Set the test mode of dither function.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.5. 0x0014+N*0x04 LCD FRM Seed Register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04(N=0~5)			Register Name: LCD_FRM_SEED_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Set the seed used in dither function. **Note: Avoid setting it to 0**

6.1.6.6. 0x002C+N*0x04 LCD FRM Table Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0~3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7F7F7777

6.1.6.7. 0x003C LCD 3D FIFO Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN 0: Disable 1: Enable Enable the 3rd fifo bist test function.
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1 Only valid when 3D_FIFO_SETTING is set as 2.
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Bypass 01: Used as normal FIFO 10: Used as 3D interlace FIFO 11: Reserved

6.1.6.8. 0x0040 LCD Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable It executes at the beginning of the first blank line of LCD timing.
30:26	/	/	/
25:24	R/W	0x0	LCD_IF 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved Set the interface type of LCD controller.
23	R/W	0x0	LCD_RB_SWAP 0: Default 1: Swap RED and BLUE data at FIFO1 Enable the function to swap red data and blue data in FIFO1.
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 **Note: 1 holding time must more than 1 DCLK.**
20	R/W	0x0	LCD_INTERLACE_EN 0:Disable 1:Enable This flag is valid only when LCD_EN == 1
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DELAY The unit of delay is T_{line}. Valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			111: Gridding Check

6.1.6.9. 0x0044 LCD Data Clock Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others:Reserved
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk / DCLKDIV **Note: If dclk1&dclk2 used, DCLKDIV >=6. If dclk only, DCLKDIV >=1**

6.1.6.10. 0x0048 LCD Basic Timing Register0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	Y Panel height is Y+1

6.1.6.11. 0x004C LCD Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel: HT = X + BLANK Limitation:

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

6.1.6.12. 0x0050 LCD Basic Timing Register2(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

6.1.6.13. 0x0054 LCD Basic Timing Register3(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

6.1.6.14. 0x0058 LCD HV Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE 0000: 24-bit/1cycle parallel mode 1000: 8-bit/3 cycle RGB serial mode(RGB888) 1010: 8-bit/4 cycle Dummy RGB(DRGB)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1011: 8-bit/4 cycle RGB Dummy(RGBD) 1100: 8-bit/2 cycle YUV serial mode(CCIR656) Set the HV mode of LCD controller.
27:26	R/W	0x0	RGB888_ODD_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at odd lines of the panel (line 1, 3, 5, 7…)
25:24	R/W	0x0	RGB888_EVEN_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at even lines of the panel (line 2, 4, 6, 8…)
23:22	R/W	0x0	YUV_SM 00: YUYV 01: YVYU 10: UYVY 11: VYUY Serial YUV mode output sequence 2-pixel-pair of every scan line
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01: delay 2 line(CCIR PAL) 10: delay 3 line(CCIR NTSC) 11: reserved Set the delay line mode.
19	R/W	0x0	CCIR_CSC_DIS 0: Enable 1: Disable Only valid when HV mode is “1100”. Select ‘0’ LCD convert source from RGB to YUV
18:0	/	/	/

6.1.6.15. 0x0060 LCD CPU Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI Set the i8080 interface work mode.
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG Status of Write Operation 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG Status of Read Operation 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode If it is 1, all the valid data during this frame are written to panel. This bit is sampled by Vsync.
16	R/W	0x0	FLUSH Direct Transfer Mode If it is enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: Disable 1: Enable Entry addr is 0xFF8.
2	R/W	0x0	TRIGGER_FIFO_EN 0:Disable 1:Enable Enable the trigger FIFO.
1	R/W1S	0x0	TRIGGER_START Write ‘1’ to start a frame flush, writing ’0’ has no effect. This flag indicated frame flush is running. Software must write ‘1’ only when this flag is ‘0’.
0	R/W	0x0	TRIGGER_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Trigger mode disable 1: Trigger mode enable Enable trigger mode.

6.1.6.16. 0x0064 LCD CPU Panel Write Data Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus

6.1.6.17. 0x0068 LCD CPU Panel Read Data Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus

6.1.6.18. 0x006C LCD CPU Panel Read Data Register1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus

6.1.6.19. 0x0084 LCD LVDS Configure Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	LCD_LVDS_EN 0: Disable 1: Enable Enable lvds interface
30	R/W	0	LCD_LVDS_LINK 0: Single link 1: Dual link Select work single link mode or dual link mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

29	R/W	0x0	LCD_LVDS_EVEN_ODD_DIR 0: Normal 1: Reverse Set the order of even pixel and odd pixel.
28	R/W	0x0	LCD_LVDS_DIR 0: Normal 1: Reverse Set the lvds direction
27	R/W	0x0	LCD LVDS MODE 0: NS mode 1: JEIDA mode Set the LVDS data mode.
26	R/W	0x0	LCD_LVDS_BIT_WIDTH 0: 24-bit 1: 18-bit
25	R/W	0x0	LCD_LVDS_DEBUG_EN 0: Disable 1: Enable
24	R/W	0x0	LCD_LVDS_DEBUG_MODE 0: Mode0 random data 1: Mode1 output clock period=7/2 lvds clk period Set the output signal in debug mode.
23	R/W	0x0	LCD_LVDS_CORRECT_MODE 0: Mode0 1: Mode1 Set the lvds correct mode.
22:21	/	/	/
20	R/W	0x0	LCD_LVDS_CLK_SEL 0: Reserved 1: LCD CLK Select the clock source of lvds.
19:5	/	/	/
4	R/W	0x0	LCD_LVDS_CLOCK_POL 0: Reverse 1: Normal Set the clock polarity of lvds.
3:0	R/W	0x0	LCD_LVDS_DATA_POL 0: Reverse 1: Normal Set the data polarity of lvds.

6.1.6.20. 0x0088 LCD IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088	Register Name: LCD_IO_POL_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IO_OUTPUT_SEL 0: Normal output 1: Register output When it is set as '1', d[23:0], io0, io1,io3 sync to dclk.
30:28	R/W	0x0	DCLK_SEL 000: Used DCLK0(normal phase offset) 001: Used DCLK1(1/3 phase offset) 010: Used DCLK2(2/3 phase offset) 100: DCLK0/2 phase 0 101: DCLK0/2 phase 90 Others: Reserved Set the phase offset of clock and data in hv mode.
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

6.1.6.21. 0x008C LCD IO Control Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: Normal 1: Bits_invert Set the endian of data bits.
27	R/W	0x1	IO3_OUTPUT_TRI_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Disable 0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable LCD output port D[23:0] output enable, with independent bit control.

6.1.6.22. 0x00FC LCD Debug Register(Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the fifo is in underflow status.
30	/	/	/
29	R	0x1	LCD_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

6.1.6.23. 0x0100 LCD CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	R/W	0x0	CEU_EN 0: Bypass 1: Enable Enable CEU function.
30	R/W	0x0	BT656 F_MASK 0: Disable 1: Enable
29	R/W	0x0	BT656 F_MASK_VALUE 0/1
28:0	/	/	/

6.1.6.24. 0x0110+N*0x04 LCD CEU Coefficient Register0(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04(N=0~10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13-bit value, range of (-16,16)

6.1.6.25. 0x011C+N*0x10 LCD CEU Coefficient Add Register(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc N=2: Bc Signed 19-bit value, range of (-16384, 16384)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.26. 0x0140+N*0x04 LCD CEU Coefficient Range Register(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0~2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0,255]

6.1.6.27. 0x0160 LCD CPU Panel Trigger Register0(Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set to 20*pixel above.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

6.1.6.28. 0x0164 LCD CPU Panel Trigger Register1(Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

6.1.6.29. 0x0168 LCD CPU Panel Trigger Register2(Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0x0	TRANS_START_MODE 0: ecc_fifo+tri_fifo 1: tri_fifo

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Select the FIFOs used in CPU mode.
14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1 Set the sync mode in CPU interface.
12:0	R/W	0x0	TRANS_START_SET Usually set as the length of a line.

6.1.6.30. 0x016C LCD CPU Panel Trigger Register3(Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode When it is set as 2b'01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When it is set as 2b'10 or 2b'11, IO0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

6.1.6.31. 0x0170 LCD CPU Panel Trigger Register4(Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: Disable 1: Enable Enable the plug mode used in DSI command mode.
27:25	/	/	/
24	R/W	0x0	A1 Valid in first Block.
23:0	R/W	0x0	D23-D0 Valid in first Block.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.32. 0x0174 LCD CPU Panel Trigger Register5(Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	A1 Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

6.1.6.33. 0x0180 LCD Color Map Control Register(Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: LCD_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: Bypass 1: Enable Enable the color map function. This module only work when X is divided by 4.
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1 Set the pixel output format in color map function.

6.1.6.34. 0x0190 LCD Color Map Odd Line Register0(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

6.1.6.35. 0x0194 LCD Color Map Odd Line Register1(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

6.1.6.36. 0x0198 LCD Color Map Even Line Register0(Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 bit15-12: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.37. 0x019C LCD Color Map Even Line Register1(Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1110: in_r3 1111: Reserved Indicates the output order of components.

6.1.6.38. 0x01F0 LCD Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the safe mode.

6.1.6.39. 0x0220 LCD LVDS Analog Register 0(Default Value: 0x0000_0000)

Offset: 0x220			Register Name: LCD_LVDS0_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS_EN_MB Enable the bias circuit of the LVDS_ANA module. 0: Disable 1: Enable
30	R/W	0x0	Reserved
29	R/W	0x0	EN_LVDS Enable LVDS.
28	R/W	0x0	EN_24M Enable the 24M clock.
27:25	/	/	/
24	R/W	0x0	LVDS_HPREN_DRVC Enable clock channel drive 0: disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: enable
23:20	R/W	0x0	LVDS_HPREN_DRV Enable clock channel[3:0] drive 0: disable 1: enable
19:17	R/W	0x0	LVDS_REG_C Adjust current flowing through rload of rx to change the differential signals amplitude 000: 216 mV 001: 252 mV 010: 276 mV 011: 312 mV 100: 336 mV 101: 372 mV 110: 395 mV 111: 432 mV
16	R/W	0x0	LVDS_REG_DENC Choose data output or pll test clock output in LVDS_TX
15:12	R/W	0x0	LVDS_REG_DEN Choose data output or pll test clock output in LVDS_TX
11	/	/	/
10:8	R/W	0x0	LVDS_REG_R Adjust current flowing through rload of rx to change the common signals amplitude. 000: 0.925 V 001: 0.950 V 010: 0.975 V 011: 1.000 V 100: 1.025 V 101: 1.050 V 110: 1.075 V 111: 1.100 V
7:5	/	/	/
4	R/W	0x0	LVDS_REG_PLRC Lvds clock channel direction 0: Normal 1: Reverse
3:0	R/W	0x0	LVDS_REG_PLR Lvds data channel[3:0] direction 0: Normal 1: Reverse

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6.40. 0x0230 LCD Sync Control Register(Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	LCD_CONTROLLER_WORK_MODE 0:Single DSI mode 1:Dual DSI mode
7:5	/	/	/
4	R/W	0x0	LCD_CONTROLLER_SYNC_MASTER_SLAVE 0:Master 1:Slave **Note:Only use in Single DSI mode.**
3:1	/	/	/
0	R/W	0x0	LCD_CONTROLLER_SYNC_MODE 0:Sync in the first time 1:Sync every frame **Note:Only use in Single DSI mode.**

6.1.6.41. 0x0234 LCD Sync Position Register(Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_SYNC_PIXEL_NUM Set the pixel number of master LCD controller which is used to trigger the slave LCD controller to start working. This value is the number of pixels between the trigger point and the end of the line. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**
15:12	/	/	/
11:0	R/W	0x0	LCD_SYNC_LINE_NUM Set the line number of master LCD controller which is used to trigger the slave LCD controller to start working. It is only set in master LCD controller. It is not necessarily to set in slave LCD controller. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**

6.1.6.42. 0x0238 LCD Slave Stop Position Register(Default Value: 0x0000_0000)

Offset: 0x0238	Register Name:LCD_SLAVE_STOP_POS_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
7:0	R/W	0x0	STOP_VAL Set the stop position of the slave LCD. This value is the number of pixels between the stop position and the end of the HFP. Stop_pos = HFP - Stop_val. 0<Stop_pos<HFP-2. **Note:Only use in Single DSI mode.**

6.1.6.43. 0x0400~0x07FF LCD Gamma Table Register(Default Value: 0x0000_0000)

Offset: 0x0400~0x07FF			Register Name: LCD_GAMMA_TABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x00	Red Component
15:8	R/W	0x00	Green Component
7:0	R/W	0x00	Blue Component

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2. DSI

6.2.1. Overview

The Display Serial Interface (DSI) is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.01 and a D-PHY module which is compliance with MIPI DPHY specification V1.00.

DSI Host Features:

- Compliance with MIPI DSI v1.01
- Supports up to 4 lanes
- Maximum 1920 x 1200@60fps performance for MIPI DSI
- Supports non-burst mode with sync pulse/sync event, burst mode and command mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous lane clock mode and non-continuous lane clock mode
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Hardware checksum capabilities

D-PHY Features:

- Compliance with D-PHY v1.00
- Supports up to 4 lanes, and lane speed up to 2 Gbps per lane in forward direction
- Aggregate throughput up to 8 Gbps with 4 data lanes
- Bidirectional communication in low power mode through data lane 0
- Supports low power Escape mode and Ultra Low Power state
- Supports multiplex with GPIO, GPIO can work in 3.3 V or 1.8 V power supply

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.2. Block Diagram

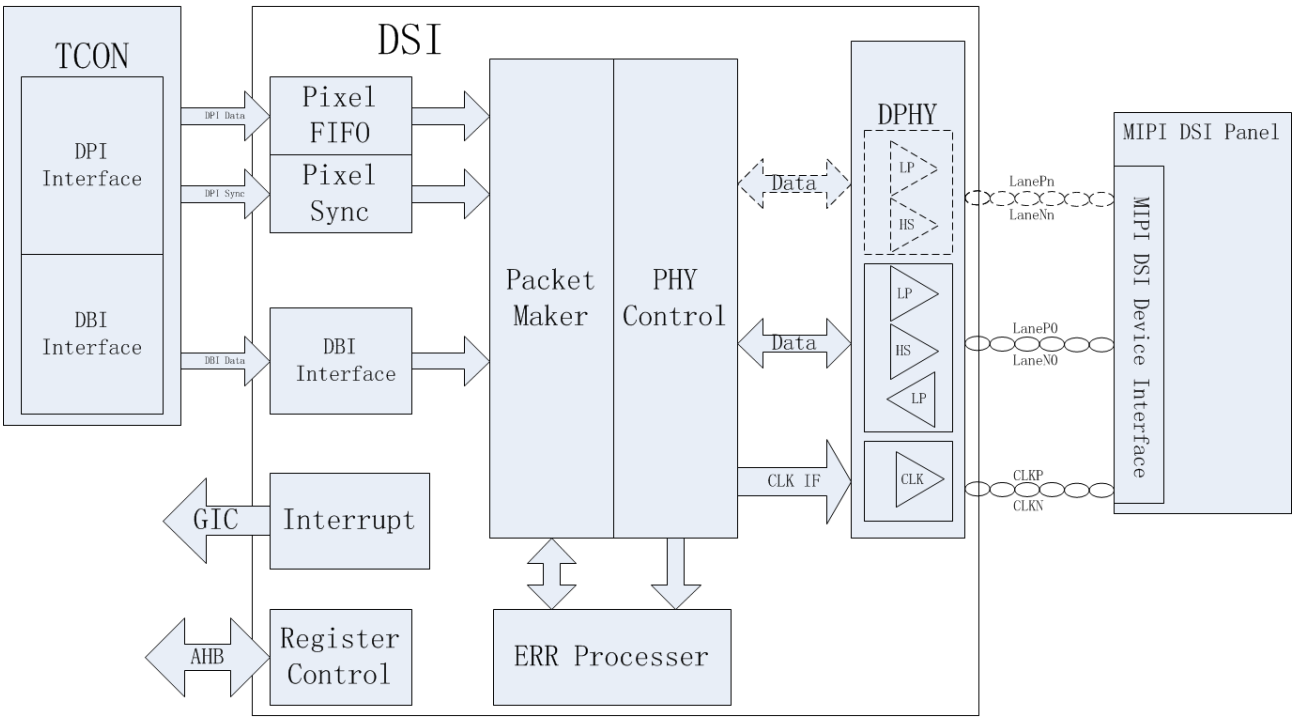


Figure 6- 14. MIPI DSI System Block Diagram

TCON is connected with DSI Controller through DPI and DBI. Packet Maker transforms pixel data of TCON into data packets based on a designated mode(video mode with sync pulse/video mode with sync event/burst mode/command mode). PHY Control distributes data packets to every lane, and starts filling for alignment. After data packets arrive at DPHY, the data packets start to serialize, then they are sent into sink end. The ERR processor monitors the whole process, if there is a mistake, the corresponding state position is set to “1”.

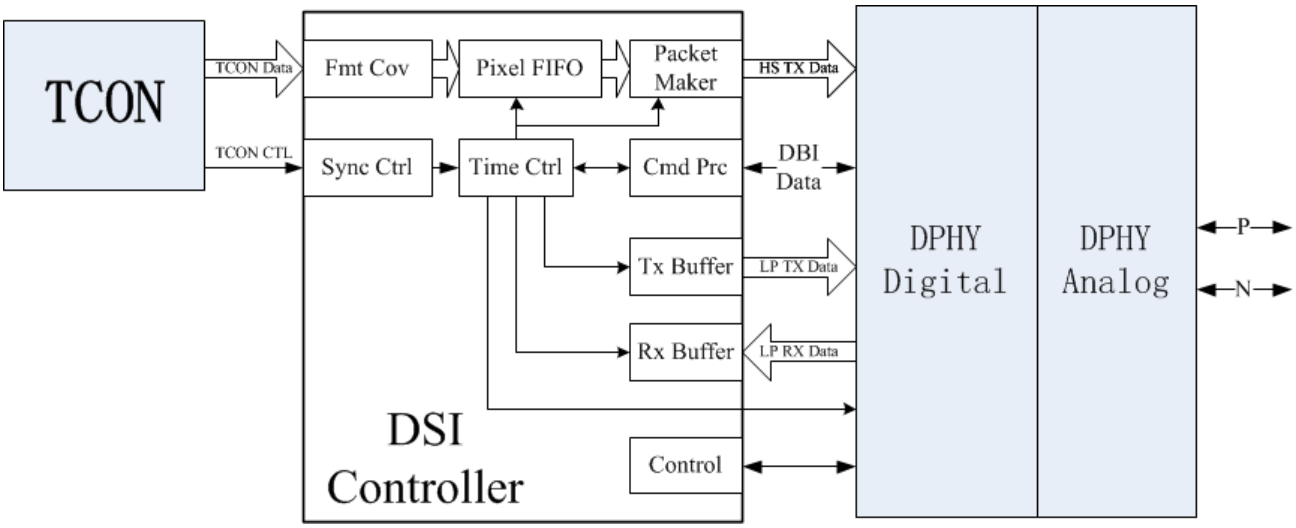


Figure 6- 15. MIPI DSI Internal Unit

TCON synchronous signals come into DSI Controller, and input into Time Ctrl. According to TCON synchronous signals,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

the Time Ctrl controls and drives the operation of every sub module.

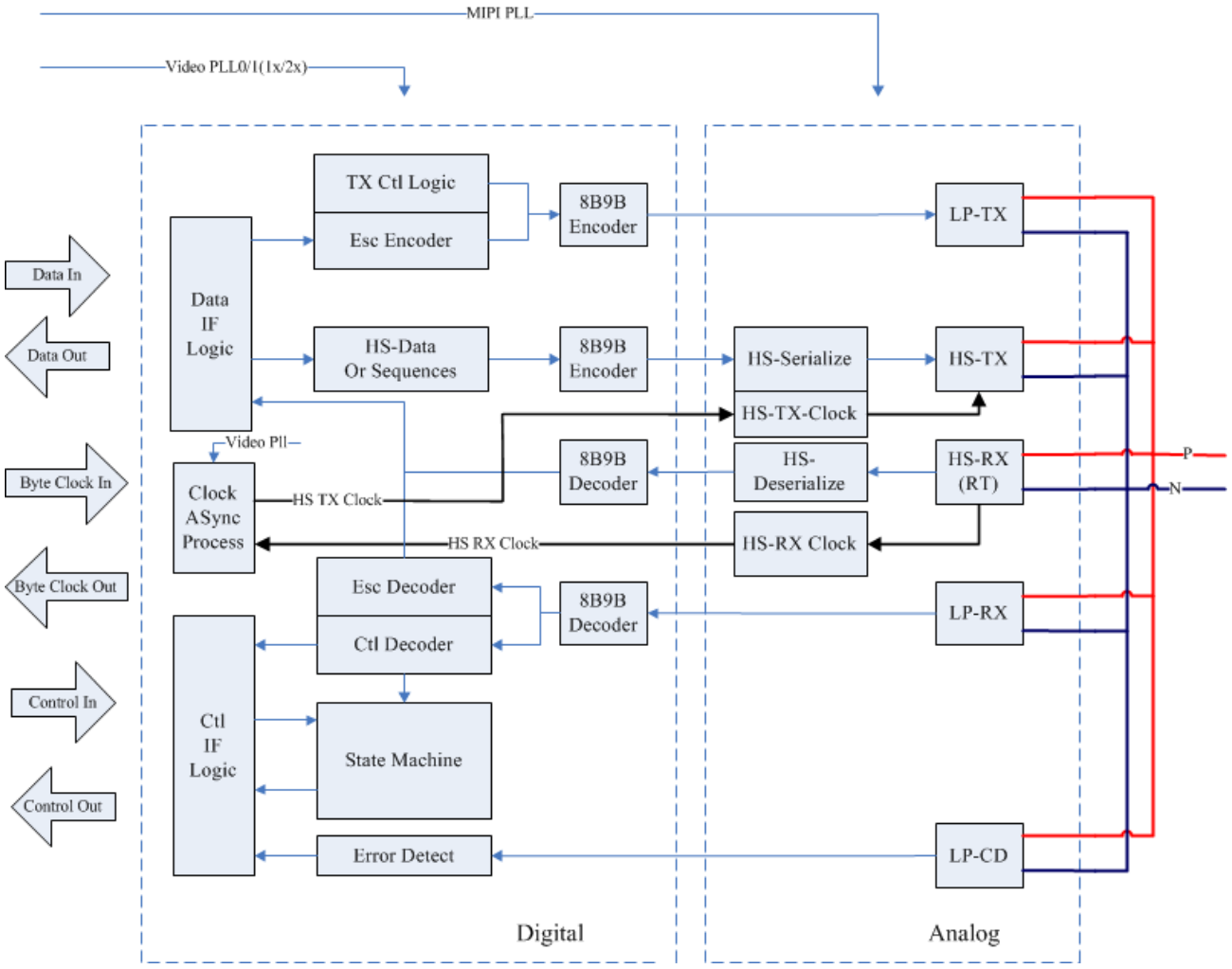


Figure 6- 16. DPHY Block Diagram

Serialization and deserialization of high speed data are operated in the analog part of DPHY. The digital and analog part of DPHY use two different clocks, so the transmit process and receive process of high speed data are asynchronous. The work clock of digital part is Byte Clock, usually set at about 150 MHz, which are lower than clocks of analog part. In order to provide the reliability of transmission, the DPHY supports 9-bit encoding mode, but it needs extra bandwidth to transmit additional bits.

6.2.3. Operations and Functional Descriptions

6.2.3.1. External Signals

The following table describes the external signals of MIPI DSI.

Table 6- 9. MIPI DSI External Signals

Signal	Description	Type
DSI_DP0	The positive port of lane0	AI/O

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DSI_DM0	The negative port of lane0	AI/O
DSI_DP1	The positive port of lane1	AO
DSI_DM1	The negative port of lane1	AO
DSI_DP2	The positive port of lane2	AO
DSI_DM2	The negative port of lane2	AO
DSI_DP3	The positive port of lane3	AO
DSI_DM3	The negative port of lane3	AO
DSI_CKP	The positive port of clock lane	AO
DSI_CKM	The negative port of clock lane	AO

6.2.3.2. Clock Sources

The following tables describe the clock sources of MIPI DSI. Table 6-10 describes the clock sources of MIPI DSI Controller and Table 6-11 describes the clock source of D-PHY.

Table 6- 10. MIPI DSI Controller Clock Sources

Clock Sources	Description
Local Clock	The clock for DSI Host configuration,which is about 150 MHz.

Table 6- 11. MIPI D-PHY Clock Source

Clock Sources	Description
D-PHY Clock	The clock for D-PHY.

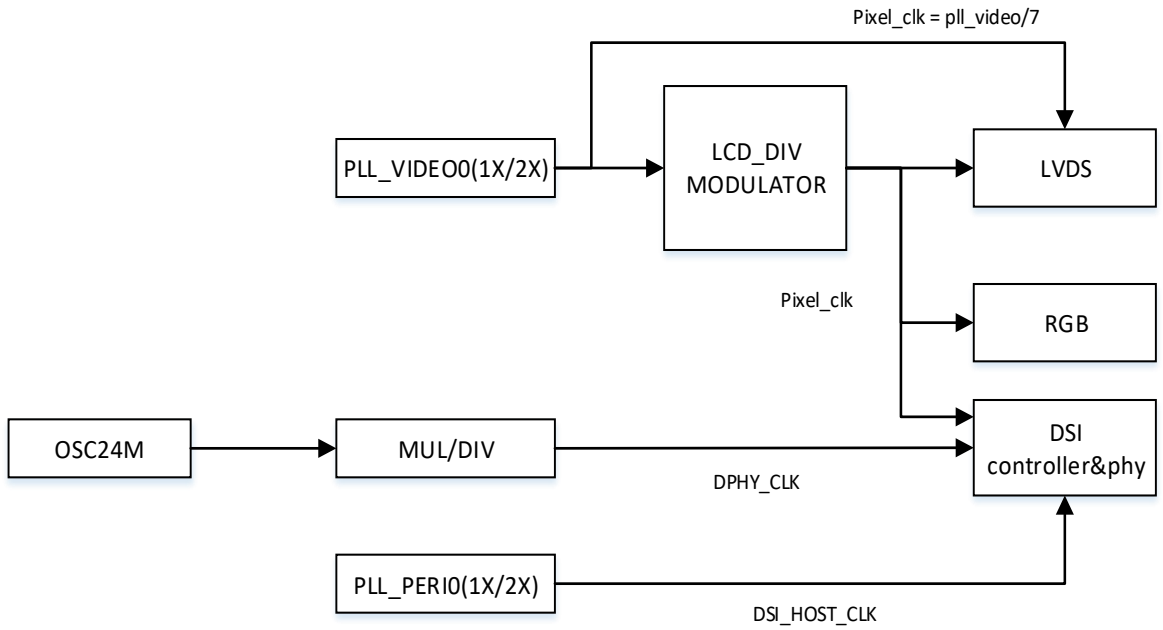


Figure 6- 17. MIPI DSI Clock System

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The DPHY CLK is the lane bit clock in high speed mode, which obtained by OSC24M frequency doubling and frequency division. The DPHY CLK is controlled by DPHY_PLL_REF0(reg0x1104), HS_phy_clk=24MHz*n/(p+1)/(m0+1), p is not 0; after the frequency configuration completes, start cp36_en,ldo_en,en_lvs,pll_en, and enable COMBOPHY PLL.

```
dphy_dev_40[sel]->dphy_pll_reg0.bits.n = n;       //HS_clk:24MHz*n/(p+1)/(m0+1);
dphy_dev_40[sel]->dphy_pll_reg0.bits.p = div_p;
dphy_dev_40[sel]->dphy_pll_reg0.bits.m0 = div_m0;
dphy_dev_40[sel]->dphy_pll_reg0.bits.m1 = div_m1;
```

6.2.3.3. MIPI DSI Protocol Escape Entry

The following table shows the escape entry codes in MIPI DSI.

Table 6- 12. Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	Mode	11100001
Ultra-Low Power State	Mode	00011110
Undefined-1	Mode	10011111
Undefined-2	Mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

6.2.3.4. MIPI DSI Date Type

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown below.

Table 6- 13. Data Types for Processor-sourced Packets

Data Type(hex)	Data Type(binary)	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE, all unspecified codes are reserved	

The following table presents the complete set of peripheral-to-processor Data Types.

Table 6- 14. Complete Set of Peripheral-to-Processor Data Types

Data Type(hex)	Data Type(binary)	Description	Packet Size
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge and Error Report	Short
03h – 07h	00 0011 – 00 0111	Reserved	
08h	00 1000	End of Transmission packet (EoTp)	Short
09h – 10h	00 1001 – 01 0000	Reserved	
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
13h – 19h	01 0011 – 01 1001	Reserved	
1Ah	01 1010	Generic Long READ Response	Long
1Bh	01 1011	Reserved	
1Ch	01 1100	DCS Long READ Response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	
21h	10 0001	DCS Short READ Response, 1 byte returned	Short

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Data Type(hex)	Data Type(binary)	Description	Packet Size
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	

The following table shows the bit assignment for all error reporting.

Table 6- 15. Error Report Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
Bit	Description
14	Reserved
15	DSI Protocol Violation

6.2.3.5. D-PHY Lane State

The following table shows all the lane states of D-PHY in MIPI DSI standard.

Table 6- 16. D-PHY Lane State

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.3.6. D-PHY Lane Sequence

The sequence in data lane:

SOT sequence: LP-11,LP-01,LP-00,HS Sync-sequence ('00011101')

EOT sequence: Diff HS-0 or HS-1, LP-11

Escape mode request: LP-11, LP-10, LP-00,LP-01,LP-00, Escape Entry Command

The following table shows the supported entry command.

Table 6- 17. Entry Command

Escape Mode Action	Command Type	Entry Command Pattern
Ultra-Low Power State	mode	00011110
Reset-Trigger [Remote Application]	Trigger	01100010

The sequence in clock lane:

Clock Lane only supports ULPS, an Escape mode entry code is not required.

During Data and Clock ULPS state, the lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

6.2.3.7. D-PHY Timing

SOT and EOT:

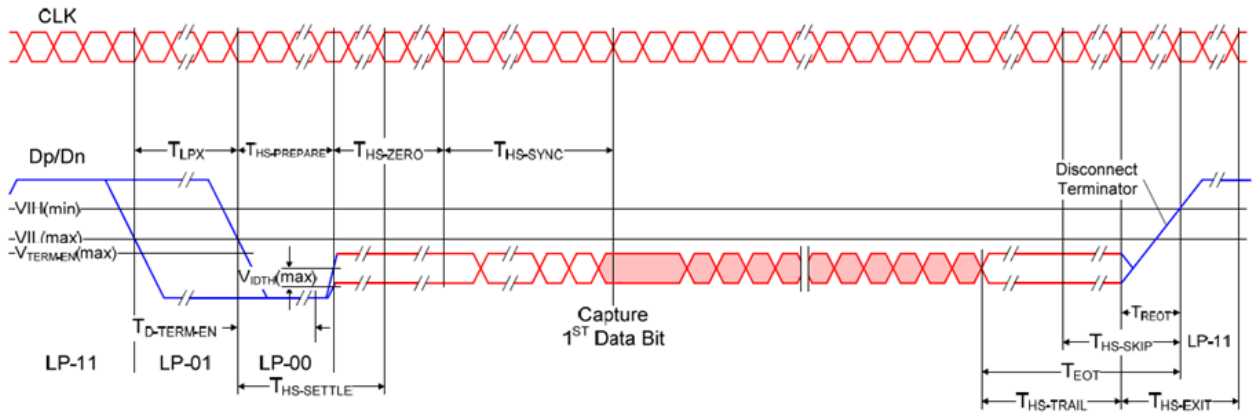


Figure 6- 18. DPHY SOT and EOT Timing

Escape mode timing:

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

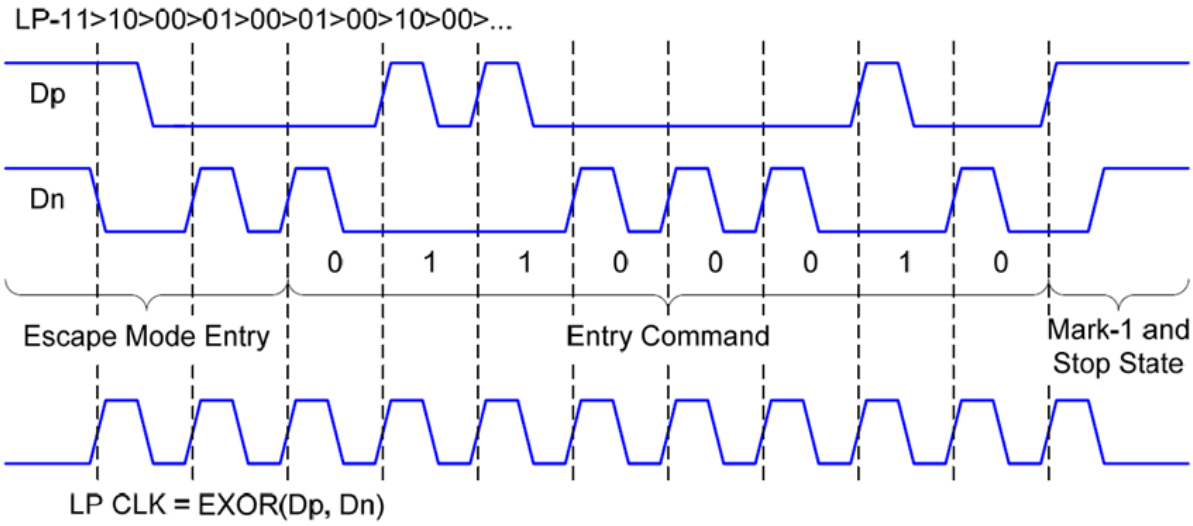


Figure 6- 19. DPHY Escape Mode Timing

Ultra-Low Power State is exited by means of a Mark-1 state with a length T_{WAKEUP} followed by a Stop state.

Clock switching between HS and LP:

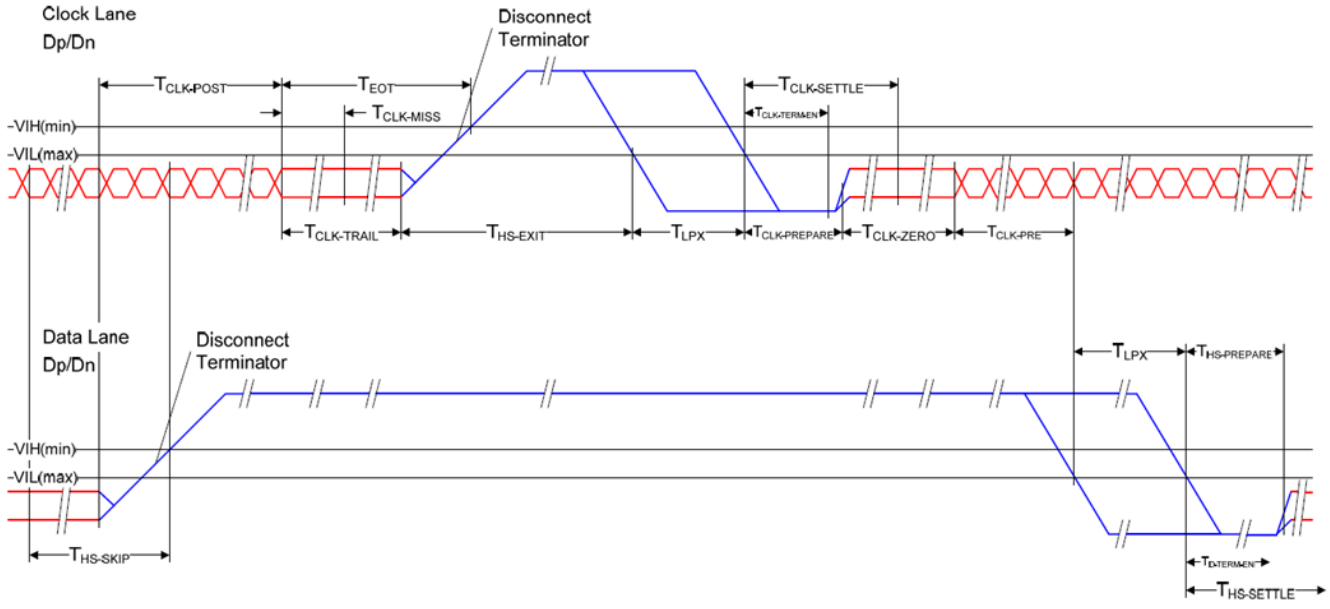


Figure 6- 20. Switching Between HS and LP Timing

6.2.3.8. D-PHY Error Behavior

(1) SoT Error

The Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error. The synchronization

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

may be usable, but confidence in the payload data is lower. If this situation occurs, an SoT Error is indicated.

(2) SoT Sync Error

If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected, a SoT Sync Error is indicated.

(3) Escape Mode Entry Command Error

If the receiving Lane Module does not recognize the received Entry Command for Escape mode, an Escape mode Entry Command Error is indicated.

(4) False Control Error

If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence, a False Control Error is indicated. This error is also indicated if a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).

6.2.4. Programming Guidelines

6.2.4.1. Video Mode Initial Sequence

The following diagram shows the initial sequence for video mode.

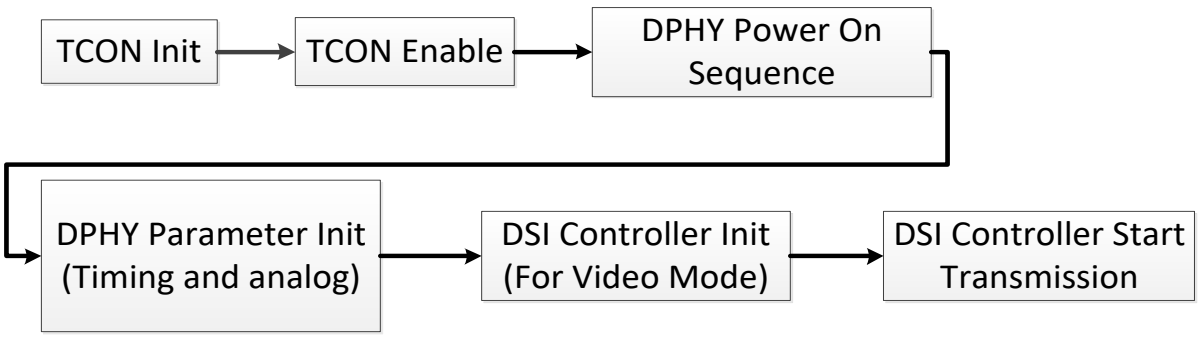


Figure 6- 21. Video Mode Initial Sequence

6.2.4.2. Command Mode Initial Sequence

The following diagram shows the initial sequence for command mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

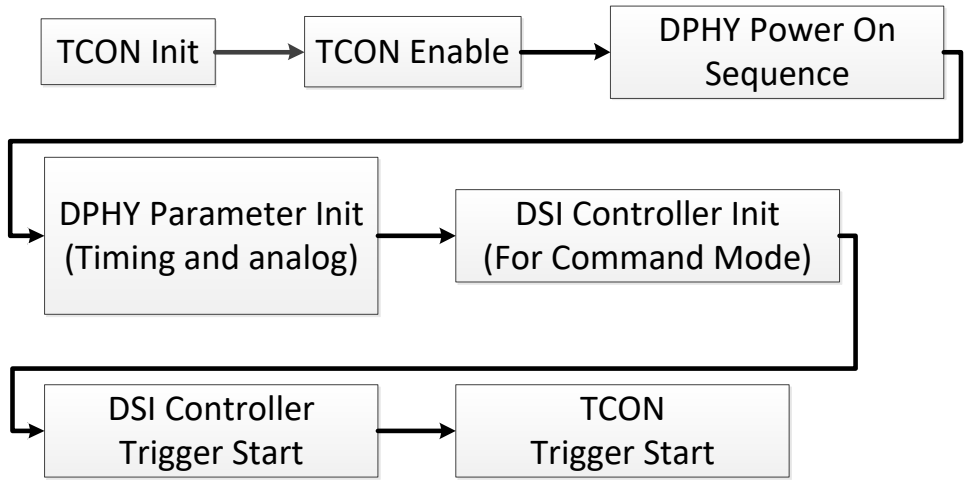


Figure 6- 22. Command Mode Initial Sequence

6.2.5. Register List

Module Name	Base Address
COMBO_PHY_TX_DSI	0x06504000
COMBO_PHY_TX_GPIO_DSI	0x06504400

Register Name	Offset	Description
DSI_CTL_REG	0x0000	DSI Control Register
DSI_GINT0_REG	0x0004	DSI Global Interrupt Register0
DSI_GINT1_REG	0x0008	DSI Global Interrupt Register1
DSI_BASIC_CTL_REG	0x000C	DSI Basic Control Register
DSI_BASIC_CTL0_REG	0x0010	DSI Basic Control Register0
DSI_BASIC_CTL1_REG	0x0014	DSI Basic Control Register1
DSI_BASIC_SIZE0_REG	0x0018	DSI Basic Timing Register0
DSI_BASIC_SIZE1_REG	0x001C	DSI Basic Timing Register1
DSI_BASIC_INST0_REG	0x0020+N*0x04	DSI Basic Instruction Register0 (N=0,1,2,3,4,5,6,7)
DSI_BASIC_INST1_REG	0x0040	DSI Basic Instruction Register1
DSI_BASIC_INST2_REG	0x0044	DSI Basic Instruction Register2
DSI_BASIC_INST3_REG	0x0048	DSI Basic Instruction Register3
DSI_BASIC_INST4_REG	0x004C	DSI Basic Instruction Register4
DSI_BASIC_INST5_REG	0x0050	DSI Basic Instruction Register5
DSI_BASIC_INST6_REG	0x0054	DSI Basic Instruction Register6
DSI_BASIC_TRAN0_REG	0x0060	DSI Basic Transmission Register0
DSI_BASIC_TRAN4_REG	0x0078	DSI Basic Transmission Register4
DSI_BASIC_TRAN5_REG	0x007C	DSI Basic Transmission Register5
DSI_PIXEL_CTL0_REG	0x0080	DSI Pixel Control Register0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DSI_PIXEL_PH_REG	0x0090	DSI Pixel Packet Header Register
DSI_PIXEL_PD_REG	0x0094	DSI Pixel Packet Data Register
DSI_PIXEL_PF0_REG	0x0098	DSI Pixel Packet Footer Register0
DSI_PIXEL_PF1_REG	0x009C	DSI Pixel Packet Footer Register1
DSI_SYNC_HSS_REG	0x00B0	DSI H Sync Start Register
DSI_SYNC_HSE_REG	0x00B4	DSI H Sync End Register
DSI_SYNC_VSS_REG	0x00B8	DSI V Sync Start Register
DSI_SYNC_VSE_REG	0x00BC	DSI V Sync End Register
DSI_BLK_HSA0_REG	0x00C0	DSI Blanking H Sync Active Register0
DSI_BLK_HSA1_REG	0x00C4	DSI Blanking H Sync Active Register1
DSI_BLK_HBP0_REG	0x00C8	DSI Blanking H Back Porch Register0
DSI_BLK_HBP1_REG	0x00CC	DSI Blanking H Back Porch Register0
DSI_BLK_HFP0_REG	0x00D0	DSI Blanking H Front Porch Register0
DSI_BLK_HFP1_REG	0x00D4	DSI Blanking H Front Porch Register1
DSI_BLK_HBLK0_REG	0x00E0	DSI H Blanking Register0
DSI_BLK_HBLK1_REG	0x00E4	DSI H Blanking Register1
DSI_BLK_VBLK0_REG	0x00E8	DSI V Blanking Register0
DSI_BLK_VBLK1_REG	0x00EC	DSI V Blanking Register1
DSI_BURST_LINE_REG	0x00F0	DSI Burst Line Register
DSI_BURST_DRQ_REG	0x00F4	DSI Burst DRQ Register
DSI_DEBUG_REG	0x00FC	DSI Debug Register
DSI_BASIC_INST10_REG	0x0120+N*0x04(N=0,1,2,3,4,5,6)	DSI Basic INST10 Register
DSI_BASIC_INST11_REG	0x0140	DSI Basic INST11 Register
DSI_BASIC_INST13_REG	0x0148	DSI Basic INST13 Register
DSI_SAFE_PERIOD_REG	0x01F0	DSI Safe Period Register
DSI_CMD_CTL_REG	0x0200	DSI Command Control Register
DSI_CMD_RX_REG	0x0240+N*0x04	DSI Command RX Register (N=0,1,2,3,4,5,6,7)
DSI_CMD_TX_REG	0x0300+N*0x04	DSI Command TX Register (N=0,1,2,…,63)
DSI_DEBUG0_REG	0x02E0	DSI Debug Register0
DSI_DEBUG1_REG	0x02E4	DSI Debug Register1
DSI_INST_DEBUG_REG	0x02EC	DSI INST Debug Register
DSI_DEBUG2_REG	0x02F0	DSI Debug Register2
DSI_DEBUG3_REG	0x02F4	DSI Debug Register3
DSI_DEBUG4_REG	0x02F8	DSI Debug Register4
DSI_FIFO_BIST_REG	0x0FF8	DSI FIFO Bist Register
The following addresses need add offset 0x4000.		
DPHY_CTL_REG	0x1000	DPHY Control Register
DPHY_TX_CTL_REG	0x1004	DPHY TX Control Register
DPHY_TX_TIME0_REG	0x1010	DPHY TX Timing Parameter 0 Register
DPHY_TX_TIME1_REG	0x1014	DPHY TX Timing Parameter 1 Register
DPHY_TX_TIME2_REG	0x1018	DPHY TX Timing Parameter 2 Register
DPHY_TX_TIME3_REG	0x101C	DPHY TX Timing Parameter 3 Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DPHY_TX_TIME4_REG	0x1020	DPHY TX Timing Parameter 4 Register
DPHY_RX_TIME0_REG	0x1030	DPHY RX Timing Parameter 0 Register
DPHY_RX_TIME1_REG	0x1034	DPHY RX Timing Parameter 1 Register
DPHY_RX_TIME3_REG	0x1040	DPHY RX Timing Parameter 3 Register
DPHY_ANA0_REG	0x104C	DPHY Analog 0 Register
DPHY_ANA1_REG	0x1050	DPHY Analog 1 Register
DPHY_ANA2_REG	0x1054	DPHY Analog 2 Register
DPHY_ANA3_REG	0x1058	DPHY Analog 3 Register
DPHY_ANA4_REG	0x105C	DPHY Analog 4 Register
DPHY_INT_EN0_REG	0x1060	DPHY Interrupt Enable 0 Register
DPHY_INT_EN1_REG	0x1064	DPHY Interrupt Enable 1 Register
DPHY_INT_EN2_REG	0x1068	DPHY Interrupt Enable 2 Register
DPHY_INT_PD0_REG	0x1070	DPHY Interrupt Pending 0 Register
DPHY_INT_PD1_REG	0x1074	DPHY Interrupt Pending 1 Register
DPHY_DBG0_REG	0x10E0	DPHY Debug 0 Register
DPHY_DBG1_REG	0x10E4	DPHY Debug 1 Register
DPHY_DBG2_REG	0x10E8	DPHY Debug 2 Register
DPHY_DBG3_REG	0x10EC	DPHY Debug 3 Register
DPHY_DBG4_REG	0x10F0	DPHY Debug 4 Register
DPHY_TX_SKEW_REG0	0x10F8	DPHY TX Skew Register0
DPHY_TX_SKEW_REG1	0x10FC	DPHY TX Skew Register1
DPHY_TX_SKEW_REG2	0x1100	DPHY TX Skew Register2
DPHY_PLL_REG0	0x1104	DPHY PLL Register0
DPHY_PLL_REG1	0x1108	DPHY PLL Register1
COMBO_PHY_REG0	0x1110	Combo PHY Register0
COMBO_PHY_REG1	0x1114	Combo PHY Register1

6.2.6. Registers Description

6.2.6.1. 0x0000 DSI Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: DSI_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DSI_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.

6.2.6.2. 0x0004 DSI Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004	**Register Name: DSI_GINT0_REG**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	PDE_PEDGE_IN_DRQ_ERR In video mode: Drq is the signal that dsi request data from tcon. Pde is the data valid signal that tcon send data to dsi. If during an active time of Drq signal,there is no rising edge of Pde or there are more than 1 rising edge of Pde appeared, it indicates that an error occurs, this bit will be set to 1.
26	R	0x0	PDE_PEDGE_IN_DRQ_TOO_MANY If during an active time of Drq signal, there is more than 1 rising edge appeared, it indicates that an timing error occurs, this bit will be set to 1.
25	R	0x0	PDE_NEDGE_IN_DRQ_ERR Drq is the signal that dsi request data from tcon. Pde is the data valid signal that tcon send data to dsi. If during an active time of Drq signal, there is no falling edge of Pde or there are more than 1 rising edge of Pde appeared, it indicates that an error occurs, this bit will be set to 1.
24	R	0x0	PDE_NEDGE_IN_DRQ_TOO_MANY If during an active time of Drq signal,there are more than 1 falling edge appeared, it indicates that an timing error occurs, this bit will be set to 1.
23:21	/	/	/
20	R	0x0	BURST_LP_OVERLAP When enabled HS transmission, if the LP driver source is still working, an error occurs, this bit will be set to 1.
19	R	0x0	LINE_INT_FLAG The flag of line interrupt.
18	R	0x0	VB_INT_FLAG The flag of Vb interrupt.
17	R	0x0	INSTRU_STEP_FLAG When finished 1 instruction, this bit will be set to 1.
16	R	0x0	INTSTRU_END_FLAG When finished all instructions, this bit will be set to 1.
15:4	/	/	/
3	R/W	0x0	LINE_INT_EN 0: Disable 1: Enable Enable Line interrupt.
2	R/W	0x0	VB_INT_EN 0: Disable 1: Enable Enable Vb interrupt.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	INSTRU_STEP_EN 0: Disable 1: Enable Enable instructions step interrupt.
0	R/W	0x0	INSTRU_END_EN 0: Disable 1: Enable Enable instructions end interrupt.

6.2.6.3. 0x0008 DSI Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DSI_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_INT_NUM Set the trigger line of line interrupt.

6.2.6.4. 0x000C DSI Basic Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: DSI_BASIC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
23:16	R/W	0x0	BRDY_SET When using 4 lanes, set the delay time for module to deal with the data arrangement in data sub_package.
15:9	/	/	/
8	R/W	0x0	DSI_Start_Mode 0: Tri_Auto 1: Tri_By_TCON Note that this bit is used for video mode and burst mode.
7:4	R/W	0x0	TRAIL_INV 0000: Disable 0001: Enable Others:Reserved Enable trail inversion to deal with 4 lanes bytes aligning.
3	R/W	0x0	TRAIL_FILL 0: Disable 1: Enable fill 2bytes as trail Enable trail padding to deal with 4 lanes bytes aligning.
2	R/W	0x0	HBP_DIS 0: Normal mode 1: HBP disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Disable HBP packets.
1	R/W	0x0	HSA_HSE_DIS 0: Normal mode 1: HSA and HSE disable Disable HSA packets and HSE packets.
0	R/W	0x0	VIDEO_MODE_BURST 0: Normal mode 1: Burst mode Enable video burst mode. When in burst mode, enter LP11 each line.

6.2.6.5. 0x0010 DSI Basic Control Register0(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: DSI_BASIC_CTL0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	HS_EOTP_EN 0: Disable 1: Enable Enable Eotp packet at the end of every HS transmission. Format: "08h" "0fh" "0fh" "01h"
17	R/W	0x0	CRC_EN 0: Disable 1: Enable Enable the CRC function.
16	R/W	0x0	ECC_EN 0: Disable 1: Enable Enable the ECC function.
15:13	/	/	/
12	R/W	0x0	FIFO_GATING 0: Disable 1: Enable Gating data from TCON, note that TCON data is gating in frame unit.
11	/	/	/
10	R/W	0x0	FIFO_MANUAL_RESET Write 1 to reset all correlation FIFO, writing 0 has no effect.
9:6	/	/	/
5:4	R/W	0x0	SRC_SEL 00: TCON data 01: Test data 1x: Reserved Select the data source of DSI.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:1	/	/	/
0	R/W	0x0	INSTRU_EN 0: Disable 1: Enable When instruction enable, dsi process from instruction0.

6.2.6.6. 0x0014 DSI Basic Control Register1(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DSI_BASIC_CTL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	TRI_DELAY It is used to set the delay of transmitting data from DSI in passive mode. That is, first delay to make the relevant FIFO have data, then transmit data to external device to avoid fifo empty.
15:12	/	/	/
11:4	R/W	0x0	VIDEO_START_DELAY Delay by lines,only valid in video mode. The field is used in active mode. When DSI starts, DSI will delay by a certain number of rows before requesting data from TCON. The number of delayed row is decided by VIDEO_START_DELAY. Ensure that the number of delayed row is less than porch area.
3	/	/	/
2	R/W	0x0	VIDEO_PRECISION_MODE_ALIGN 0: Cut mode 1: Fill mode In precision mode(set in VIDEO_FRAME_MODE), if the data length is not the integer times of lanes number, we should choose cut mode.
1	R/W	0x0	VIDEO_FRAME_MODE 0: Normal mode 1: Precision mode Set 0 to start new frame by instruction, and set 1 to start new frame by counter.
0	R/W	0x0	DSI_MODE 0: Command mode 1: Video mode In video mode, enable timing define in basic size.

6.2.6.7. 0x0018 DSI Basic Timing Register0(Default Value: 0x000A_0000)

Offset: 0x0018			Register Name: DSI_BASIC_SIZE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

27:16	R/W	0xa	VIDEO_VBP Set the Vertical Blanking Porch length.
15:12	/	/	/
11:0	R/W	0x0	VIDEO_VSA Set the Vertical Sync Area length.

6.2.6.8. 0x001C DSI Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DSI_BASIC_SIZE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VIDEO_VT Set the Vertical Total length.
15:12	/	/	/
11:0	R/W	0x0	VIDEO_VACT Set the Vertical Active Area Length.

6.2.6.9. 0x0020+N*0x04 DSI Basic Instruction Register0(Default Value: 0x0000_0000)

Offset: 0x0020+N*0x04(N=0,1,2,3,4,5,6,7)			Register Name: DSI_BASIC_INST0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	INSTRU_MODE 000: Stop(LP-11) 001: BTA(Bus Turn Around) 010: HS(High Speed mode) 011: Escape Mode 100: HS Exit(only use in clk lane) 101: Nop Others: reserved Set the instruction type.
27:24	R/W	0x0	ESCAPE_ENRTY 000: LPDT 001: ULPS 010: Undef-1 011: Undef-2 100: Trigger-Reset 101: Undef-3 110: Undef-4 111: Undef-5 Others: reserved Set the Escape entry code,valid in Escape.
23:20	R/W	0x0	TRANS_PACKET

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			000: Pixel Packet 001: Command Packet 010: Pixel + Sync + Blk Packet Others: reserved Valid in HS or Escape LPDT.
19:16	R/W	0x0	TRANS_START_CONDITION 000: Immediate, used in cmd_tx 001: Trans FIFO ready TRANS_FIFO_NUM, used in command mode 010: TCON Hsync delay DSI_DELAY_CYCLE,used in video mode 011: DSI HT end, DSI new line start,used in video mode Others: reserved Valid in HS or Escape LPDT.
15:5	/	/	/
4:0	R/W	0x0	LANE_SEL Bit4: clk lane selected Bit3: data3 lane selected Bit2: data2 lane selected Bit1: data1 lane selected Bit0: data0 lane selected 0: Disable 1: Enable Instruction is valid on selected lane.

6.2.6.10. 0x0040 DSI Basic Instruction Register1(Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: DSI_BASIC_INST1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LOOP_SEL Bit31-28: Instruction7 Bit27-24: Instruction6 Bit23-20: Instruction5 Bit19-16: Instruction4 Bit15-12: Instruction3 Bit11-08: Instruction2 Bit07-04: Instruction1 Bit03-00: Instruction0 000: only one times 010: (LOOP_N0+1) times 011: (LOOP_N1+1) times Others: reserved Note LOOP_N0, LOOP_N1 is defined in DSI_BASIC_INST2_REG.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.11. 0x0044 DSI Basic Instruction Register2(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: DSI_BASIC_INST2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LOOP_N1 Set the instructions loop time in blanking area.
15:12	/	/	/
11:0	R/W	0x0	LOOP_N0 Set the instructions loop time in blanking area.

6.2.6.12. 0x0048 DSI Basic Instruction Register3(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: DSI_BASIC_INST3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	INST7_JUMP_SEL
27:24	R/W	0x0	INST6_JUMP_SEL
23:20	R/W	0x0	INST5_JUMP_SEL
19:16	R/W	0x0	INST4_JUMP_SEL
15:12	R/W	0x0	INST3_JUMP_SEL
11:8	R/W	0x0	INST2_JUMP_SEL
7:4	R/W	0x0	INST1_JUMP_SEL
3:0	R/W	0x0	INST0_JUMP_SEL Bit31-28: Instruction7 Bit27-24: Instruction6 Bit23-20: Instruction5 Bit19-16: Instruction4 Bit15-12: Instruction3 Bit11-08: Instruction2 Bit07-04: Instruction1 Bit03-00: Instruction0 0000: Jump Instruction0 0001: Jump Instruction1 0010: Jump Instruction2 0011: Jump Instruction3 0100: Jump Instruction4 0101: Jump Instruction5 0110: Jump Instruction6 0111: Jump Instruction7 1000: Jump Instruction8 1001: Jump Instruction9 1010: Jump Instruction10 1011: Jump Instruction11

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1100: Jump Instruction12 1101: Jump Instruction13 1110: Jump Instruction14 1111: Jump End Others: reserved Set the instruction order.

6.2.6.13. 0x004C DSI Basic Instruction Register4(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: DSI_BASIC_INST4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	JUMP_CFG0_EN 0:Disable instructions jump function 1:Enable instructions jump function
27:24	/	/	/
23:20	R/W	0x0	JUMP_CFG0_TO Set the instruction which will be jumped after finishing the instructions loop.
19:16	R/W	0x0	JUMP_CFG0_POINT Set the entry instruction of the instructions loop.
15:0	R/W	0x0	JUMP_CFG0_NUM Set the loop time of the instructions loop.

6.2.6.14. 0x0050 DSI Basic Instruction Register5(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DSI_BASIC_INST5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	JUMP_CFG1_EN 0:Disable instructions jump function 1:Enable instructions jump function
27:24	/	/	/
23:20	R/W	0x0	JUMP_CFG1_TO Set the instruction which will be jumped after finishing the instructions loop.
19:16	R/W	0x0	JUMP_CFG1_POINT Set the entry instruction of the instructions loop.
15:0	R/W	0x0	JUMP_CFG1_NUM Set the loop time of the instructions loop.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.15. 0x0054 DSI Basic Instruction Register6(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: DSI_BASIC_INST6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LOOP_N1_SHADOW In video burst mode, replace LOOP_N1 in active area.
15:12	/	/	/
11:0	R/W	0x0	LOOP_N0_SHADOW In video burst mode, replace LOOP_N0 in active area.

6.2.6.16. 0x0060 DSI Basic Transmission Register0(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: DSI_BASIC_TRAN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	TRANS_START_SET In video mode, hs tx by timing start. In command mode, hs tx when fifo reach this numbers.

6.2.6.17. 0x0078 DSI Basic Transmission Register4(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: DSI_BASIC_TRAN4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	HS_ZERO_REDUCE_SET Setting a value to reduce HS Zero time.Delay time to info D-PHY into HS. TRANS_START_SET- HS_ZERO_REDUCE_SET = DSI_HS_ZERO_TIME. Total hs zero time = DSI_HS_ZERO_TIME + DPHY_HS_ZERO_TIME. It should be HS_ZERO_REDUCE_SET < (TRANS_START_SET-30). Note that HS_ZERO_REDUCE_SET should be 7 hsbyte clk earlier than TRANS_START_SET, and this value is refer to lp clk. If hs=300M, lp=150M, (1/300)x8x7 ÷ (1/150)=28

6.2.6.18. 0x007C DSI Basic Transmission Register5(Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: DSI_BASIC_TRAN5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DRQ_MODE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Request tcon data at new line start 1: Request tcon data reference to Drq_set Set the DRQ request condition.
27:10	/	/	/
9:0	R/W	0x0	DRQ_SET Request tcon data reference setting, this bit is only valid when DRQ_MODE='1'.

6.2.6.19. 0x0080 DSI Pixel Control Register0(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: DSI_PIXEL_CTL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PD_PLUG_DIS Disable PD plug before pixel bytes.
15:5	/	/	/
4	R/W	0x0	PIXEL_ENDIAN 0: LSB first 1: MSB first Set the endian of the pixel data.
3:0	R/W	0x0	PIXEL_FORMAT Command mode 0000: 24-bit (rgb888) 0001: 18-bit (rgb666) 0010: 16-bit (rgb565) Video mode 1000: 24-bit(rgb888) 1001: 18-bit(rgb666L) 1010: 18-bit (rgb666) 1011: 16-bit(rgb565) Others: reserved Set the pixel format.

6.2.6.20. 0x0090 DSI Pixel Packet Header Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: DSI_PIXEL_PH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Only valid when DSI ECC is disable.
23:8	R/W	0x0	WC WC is byte numbers of PD in a pixel packet.
7:6	R/W	0x0	VC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Virtual Channel.
5:0	R/W	0x0	DT Video mode 24-bit, set as "3eh" Video mode L18-bit, set as "2eh" Video mode 18-bit, set as "1eh" Video mode 16-bit, set as "0eh" Command mode, set as "39h"

6.2.6.21. 0x0094 DSI Pixel Packet Data Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: DSI_PIXEL_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	PD_TRANN Used in transmissions except 1st one, set as "3Ch", only valid when PD_PLUG_DIS is set to '0'.
15:8	/	/	/
7:0	R/W	0x0	PD_TRAN0 Used in 1st transmission, set as "2Ch", only valid when PD_PLUG_DIS is set to '0'.

6.2.6.22. 0x0098 DSI Pixel Packet Footer Register0(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: DSI_PIXEL_PF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	CRC_FORCE CRC force to this value, this value is only valid when CRC is disabled.

6.2.6.23. 0x009C DSI Pixel Packet Footer Register1(Default Value: 0xFFFF_FFFF)

Offset: 0x009C			Register Name: DSI_PIXEL_PF1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0xffff	CRC_INIT_LINEN CRC initial to this value in transmissions except 1st one,only valid when CRC is enabled.
15:0	R/W	0xffff	CRC_INIT_LINE0 CRC initial to this value in 1st transmission every frame, only valid when CRC is enabled.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.24. 0x00B0 DSI H Sync Start Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: DSI_SYNC_HSS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "12h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT HSS, set as "21h".

6.2.6.25. 0x00B4 DSI H Sync End Register(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: DSI_SYNC_HSE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "01h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT HSE, set as "31h".

6.2.6.26. 0x00B8 DSI V Sync Start Register(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: DSI_SYNC_VSS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "07h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5:0	R/W	0x0	DT VSS, set as "01h".

6.2.6.27. 0x00BC DSI V Sync End Register(Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: DSI_SYNC_VSE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "14h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT VSE, set as "11h".

6.2.6.28. 0x00C0 DSI Blanking H Sync Active Register0(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: DSI_BLK_HSA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HSA_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of HSA packets.

6.2.6.29. 0x00C4 DSI Blanking H Sync Active Register1(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DSI_BLK_HSA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HSA_PF Set the packet footer value of HSA packets.
15:8	/	/	/
7:0	R/W	0x0	HSA_PD Set the packet value of HSA packets.

6.2.6.30. 0x00C8 DSI Blanking H Back Porch Register0(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: DSI_BLK_HBP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	HBP_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of HBP packets.

6.2.6.31. 0x00CC DSI Blanking H Back Porch Register0(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: DSI_BLK_HBP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HBP_PF Set the packet footer value of HBP packets.
15:8	/	/	/
7:0	R/W	0x0	HBP_PD Set the packet value of HBP packets.

6.2.6.32. 0x00D0 DSI Blanking H Front Porch Register0(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: DSI_BLK_HFP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HFP_PH Note that bit[23:8] is WC, define byte numbers of PD in a blank packet. Set the packet header value of HFP packets.

6.2.6.33. 0x00D4 DSI Blanking H Front Porch Register1(Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: DSI_BLK_HFP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HFP_PF Set the packet footer value of HFP packets.
15:8	/	/	/
7:0	R/W	0x0	HFP_PD Set the packet value of HFP packets.

6.2.6.34. 0x00E0 DSI H Blanking Register0(Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: DSI_BLK_HBLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HBLK_PH Note that bit[23:8] is WC, define byte numbers of PD in a blank packet. Set the packet header value of HBLK packets.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.35. 0x00E4 DSI H Blanking Register1(Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: DSI_HBLK_BLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HBLK_PF Set the packet footer value of HBLK packets.
15:8	/	/	/
7:0	R/W	0x0	HBLK_PD Set the packet value of HBLK packets.

6.2.6.36. 0x00E8 DSI V Blanking Register0(Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: DSI_BLK_VBLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VBLK_PH Note that bit[23:8] is WC, define byte numbers of PD in a blank packet. Set the packet header value of VBLK packets.

6.2.6.37. 0x00EC DSI V Blanking Register1(Default Value: 0x0000_0000)

Offset: 0x00EC			Register Name: DSI_BLK_VBLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	VBLK_PF Set the packet footer value of VBLK packets.
15:8	/	/	/
7:0	R/W	0x0	VBLK_PD Set the packet value of VBLK packets.

6.2.6.38. 0x00F0 DSI Burst Line Register(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: DSI_BRUST_LINE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	LINE_SYNCPOINT In video burst mode, set the start time of the first HS data transmission. It is set as 30 by default .
15:0	R/W	0x0	LINE_NUM In video burst mode, set the total time of each line whose unit the cycle of symbol.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.39. 0x00F4 DSI Burst DRQ Register(Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: DSI_BRUST_DRQ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	DRQ_EDGE1 In video burst mode, DRQ_EDGE0 and DRQ_EDGE1 is used to control the create time of dsi_drq. There is a timer working during burst mode. If DRQ_EDGE1 < timer value < DRQ_EDGE0, the dsi_drq will be set 1.
15:0	R/W	0x0	DRQ_EDGE0 In video burst mode,DRQ_EDGE0 and DRQ_EDGE1 is used to control the create time of dsi_drq. There is a timer working during burst mode.If DRQ_EDGE1 < timer value < DRQ_EDGE0, the dsi_drq will be set 1.

6.2.6.40. 0x00FC DSI Debug Register(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: DSI_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DSI_FIFO_UNDER_FLOW It will be set 1 when the DSI FIFO is underflow.
30:0	/	/	/

6.2.6.41. 0x0120+N*0x04 DSI Basic INST10 Register(Default Value: 0x0000_0000)

Offset: 0x0120+N*0x04(N=0,1,2,3,4,5,6)			Register Name: DSI_BASIC_INST10_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0	Instru_Mode 0000: Stop(LP-11) 0001: TBA 0010: HS-NM 0011: Escape 0100: HS Exit(only use in clk lane) 0101: Nop Others: reserved
27:24	R/W	0	Escape_Enrty 0000: LPDT 0001: ULPS 0010: Undef-1 0011: Undef-2 0100: Trigger-Reset 0101: Undef-3 0110: Undef-4 0111: Undef-5

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Others: reserved valid in Escape.
23:20	R/W	0	Trans_Packet 0000: Pixel Packet 0001: Command Packet 0010: Pixel + Sync + Blk Packet Others: reserved Valid in HS or Escape LPDT.
19:16	R/W	0	Trans_Start_Condition 0000: Immediate, used in cmd_tx 0001: Trans FIFO ready Trans_FIFO_Num, used in command mode 0010: TCON hsync delay DSI_Delay_Cycle,used in video mode 0011: DSI HT end, DSI new line start,used in video mode Others: reserved Valid in HS or Escape LPDT.
15:5	/	/	/
4:0	R/W	0	Lane_Sel Bit4: clk lane selected Bit3: data3 lane selected Bit2: data2 lane selected Bit1: data1 lane selected Bit0: data0 lane selected 0: disable 1: enable Instruction is valid on selected lane.

6.2.6.42. 0x0140 DSI Basic INST11 Register(Default Value: 0x0000_0000)

Offset: 0x0140			**Register Name: DSI_BASIC_INST11_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LOOP_SEL Bit31-28: Instruction15 Bit27-24: Instruction14 Bit23-20: Instruction13 Bit19-16: Instruction12 Bit15-12: Instruction11 Bit11-08: Instruction10 Bit07-04: Instruction9 Bit03-00: Instruction8 0: only one times 2: (Loop_N0+1) times 3: (Loop_N1+1) times Others: reserved Note Loop_N0, Loop_N1 is defined in DSI_BASIC_INST2_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.43. 0x0148 DSI Basic INST13 Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: DSI_BASIC_INST13_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	INST14_JUMP_SEL
23:20	R/W	0x0	INST13_JUMP_SEL
19:16	R/W	0x0	INST12_JUMP_SEL
15:12	R/W	0x0	INST11_JUMP_SEL
11:8	R/W	0x0	INST10_JUMP_SEL
7:4	R/W	0x0	INST9_JUMP_SEL
3:0	R/W	0x0	INST8_JUMP_SEL Bit31-28: Instruction7 Bit27-24: Instruction6 Bit23-20: Instruction5 Bit19-16: Instruction4 Bit15-12: Instruction3 Bit11-08: Instruction2 Bit07-04: Instruction1 Bit03-00: Instruction0 0000: Jump Instruction0 0001: Jump Instruction1 0010: Jump Instruction2 0011: Jump Instruction3 0100: Jump Instruction4 0101: Jump Instruction5 0110: Jump Instruction6 0111: Jump Instruction7 1000: Jump Instruction8 1001: Jump Instruction9 1010: Jump Instruction10 1011: Jump Instruction11 1100: Jump Instruction12 1101: Jump Instruction13 1110: Jump Instruction14 1111: Jump End Others: reserved Set the instruction order.

6.2.6.44. 0x01F0 DSI Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0	Register Name: DSI_SAFE_PERIOD_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, DSI controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, DSI controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line

6.2.6.45. 0x0200 DSI Command Control Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: DSI_CMD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
26	R/W	0x0	RX_OVERFLOW 1: rx data is overflow register buffer Note: Write'1' to clear this bit. Writing '0' has no effect.
25	R/W	0x0	RX_FLAG 1: rx has happened Note: Write'1' to clear this bit. Writing '0' has no effect.
24	R	0x0	RX_STATUS 0: rx is finish 1: rx is pending
20:16	R	0x0	RX_SIZE (RX_SIZE+1) is number of bytes in the last rx.
15:9	/	/	/
9	R/W	0x0	TX_FLAG 1: tx has happened Note: Write '1' to clear this bit. Writing '0' has no effect.
8	R	0x0	TX_STATUS 0: tx is finish 1: tx is pending
7:0	R/W	0x0	TX_SIZE (TX_SIZE+1) is number of bytes ready to tx

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.46. 0x0240+N*0x04 DSI Command RX Register(Default Value: 0x0000_0000)

Offset: 0x0240+N*0x04(N=0,1,2,3,4,5,6,7)			Register Name: DSI_CMD_RX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DATA Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data from rx, only in LPDT Only read when RX_Flag is setting. no way to clear this fifo.

6.2.6.47. 0x0300+N*0x04 DSI Command TX Register(Default Value: 0x0000_0000)

Offset: 0x0300+N*0x04(N=0,1,2…64)			Register Name: DSI_CMD_TX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data for tx, transmission in HS and LPDT, defined by INST_REG.

6.2.6.48. 0x02E0 DSI Debug Register0(Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: DSI_DEBUG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R	0x0	VIDEO_CURR_LINE The real time current line.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.49. 0x02E4 DSI Debug Register1(Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: DSI_DEBUG1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	VIDEO_CURR_LP2HS The current number of LP to HS in real time.

6.2.6.50. 0x02EC DSI INST Debug Register(Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: DSI_INST_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	INSTRU14_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
13	R/W	0x0	INSTRU13_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
12	R/W	0x0	INSTRU12_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
11	R/W	0x0	INSTRU11_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
10	R/W	0x0	INSTRU10_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
9	R/W	0x0	INSTRU9_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
8	R/W	0x0	INSTRU8_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
7	R/W	0x0	INSTRU7_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
6	R/W	0x0	INSTRU6_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
5	R/W	0x0	INSTRU5_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
4	R/W	0x0	INSTRU4_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
3	R/W	0x0	INSTRU3_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
2	R/W	0x0	INSTRU2_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
1	R/W	0x0	INSTRU1_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.
0	R/W	0x0	INSTRU0_UNKNOW_FLAG Write '1' to clear this bit. Writing '0' has no effect.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.51. 0x02F0 DSI Debug Register2(Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: DSI_DEBUG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
23:20	R	0x0	CURR_INSTRU_NUM Instruction number process now.
19:4	R	0x0	CURR_LOOP_NUM The loop number of instructions loop.
3:2	/	/	/
1	R/W	0x0	TRANS_FAST_FLAG When in active region, transmit FIFO is empty, this bit is set. Write '1' to clear this bit.
0	R/W	0x0	TRANS_LOW_FLAG Before trans FIFO reset, trans FIFO is not empty, this bit is set. Write '1' to clear this bit.

6.2.6.52. 0x02F4 DSI Debug Register3(Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: DSI_DEBUG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	CURR_FIFO_NUM Byte numbers in trans FIFO now.
15:0	/	/	/

6.2.6.53. 0x02F8 DSI Debug Register4(Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: DSI_DEBUG4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DSI_FIFO_BIST_EN 0: Disable 1: Enable Entry address is 0xFF8.
27:24	/	/	/
23:0	R/W	0x0	TEST_DATA Cooperated with SRC_SEL in DSI_BASIC_CTL0_REG, instead of the data from TCON.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.54. 0x1000 DPHY Control Register(Default Value: 0x0000_0000)

Offset:0x1000			Register Name: DPHY_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	LANE_NUM 000: 1 data lane 001: 2 data lane 010: 3 data lane 011: 4 data lane Note: This bits determine lane number used for transmission.
3:1	/	/	/
0	R/W	0x0	MODULE_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.

6.2.6.55. 0x1004 DPHY TX Control Register(Default Value: 0x0000_0000)

Offset:0x1004			Register Name: DPHY_TX_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	ULPSTX_ENTER 0: Direct (enter LP-00 after ULPS command) 1: Indirect (enter MARK-I after ULPS command then LP-00)
28	R/W	0x0	HSTX_CLK_CONT 0: Disable 1: Enable When this bit is enabled, clk lane continue in HS mode. When this bit is disable, clk lane anto enter LP mode.
27:26	/	/	/
25	R/W	0x0	HSTX_CLK_EXIT 0: No effect 1: Force clock lane exit from HS
24	R/W	0x0	HSTX_DATA_EXIT 0: No effect 1: Force all data lanes exit from HS
23:21	/	/	/
20	R/W	0x0	ULPSTX_CLK_EXIT 0: No effect 1: Force Clock lane exit from ULPS
19	R/W	0x0	ULPSTX_DATA3_EXIT 0: No effect

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Force data lane 3 exit from ULPS
18	R/W	0x0	ULPSTX_DATA2_EXIT 0: No effect 1: Force data lane 2 exit from ULPS
17	R/W	0x0	ULPSTX_DATA1_EXIT 0: No effect 1: Force data lane 1 exit from ULPS
16	R/W	0x0	ULPSTX_DATA0_EXIT 0: No effect 1: Force data lane 0 exit from ULPS
15:13	/	/	/
12	R/W	0x0	FORCE_LP11 0: No effect 1: Force module work in LP11
11	R/W	0x0	HSTX_8B9B_EN 0: 8B9B Encoding disable 1: 8B9B Encoding enable
10	R/W	0x0	LPTX_8B9B_EN 0: 8B9B Encoding disable 1: 8B9B Encoding enable
9	R/W	0x0	HSTX_ENDIAN 0: LSB first 1: MSB first
8	R/W	0x0	LPTX_ENDIAN 0: LSB first 1: MSB first
7:5	/	/	/
4	R/W	0x0	TX_CLK_FORCE Write 1 to force into tx default state(lp00) Writing 0 has no effect.
3	R/W	0x0	TX_D3_FORCE Write 1 to force into tx default state(lp00) Writing 0 has no effect.
2	R/W	0x0	TX_D2_FORCE Write 1 to force into tx default state(lp00) Writing 0 has no effect.
1	R/W	0x0	TX_D1_FORCE Write 1 to force into tx default state(lp00) Writing 0 has no effect.
0	R/W	0x0	TX_D0_FORCE Write 1 to force into tx default state(lp00) Writing 0 has no effect.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.56. 0x1010 DPHY TX Timing Parameter 0 Register(Default Value: 0x0000_0000)

Offset:0x1010			Register Name: DPHY_TX_TIME0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	HS_TRAIL_SET HS trail = (HS_TRAIL_SET + 2) * Tbyteclk + (2~3)*Tclk - (3~4)*Tclkd8.
23:16	R/W	0x0	HS_PRE_SET The setting of hs prepare time: Begin with LP00, end after (HS_PRE_SET + 4)*Tclk.
15:8	/	/	/
7:0	R/W	0x0	LPX_TM_SET LP pulse = (LPX_TM_SET + 1)*Tclk.

6.2.6.57. 0x1014 DPHY TX Timing Parameter 1 Register(Default Value: 0x0000_0000)

Offset:0x1014			Register Name: DPHY_TX_TIME1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	CK_POST_SET CK_Post_set can not be 0,after the falling edge of entx,keep it for (CK_POST_SET + 2)* Tclk and then turn off the clk.
23:16	R/W	0x0	CK_PRE_SET Clk pre = ((CK_PRE_SET + 2)+ (0 ~ LPX_TM_SET))* Tclk
15:8	R/W	0x0	CK_ZERO_SET CK_Zero_set can not be 0,when entxc is set 1, after (CK_ZERO_SET + 2)* Tclk, the enckq will be set as 1.
7:0	R/W	0x0	CK_PREP_SET Clk prepare = (CK_PREP_SET + 3) * clk

6.2.6.58. 0x1018 DPHY TX Timing Parameter 2 Register(Default Value: 0x0000_0000)

Offset:0x1018			Register Name: DPHY_TX_TIME2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	HS_DLY_MODE The setting of HS zero time depending on HS_DLYMODE: when HS_DLYMODE=0, HS_ZERO_TIME > 20*Tbyteclk When HS_DLYMODE=1,HS_ZERO_TIME = (HS_DLY_SET + 4)*Tclk - 2*(LPX_TM_SET + 1)*Tclk + (20~23)*Tbyteclk - (HS_PRE_SET + 4)*Tclk
27:24	/	/	/
23:8	R/W	0x0	HS_DLY_SET

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Use this value to prolong the time before LP switch to HS,cut down the length of HS-Zero.
7:0	R/W	0x0	CK_TRAIL_SET CK_TRAIL_SET clk tail =(CK_TRAIL_SET + 2)* Tclk

6.2.6.59. 0x101C DPHY TX Timing Parameter 3 Register(Default Value: 0x0000_0000)

Offset:0x101C			Register Name: DPHY_TX_TIME3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	LPTX_ULPS_EXIT_SET ULPS exit Cycles.

6.2.6.60. 0x1030 DPHY RX Timing Parameter 0 Register(Default Value: 0x0000_0000)

Offset:0x1030			Register Name: DPHY_RX_TIME0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	HSRX_SYNC_ERR_TO When HS SOT is not detected until reaching the hs sync error timeout counter, the SOT_ERR should be flagged. Only valid for data lane.
23:16	R/W	0x0	HSRX_CLK_MISS When clock lane is detected no clock until hs rx clock miss counter, the receiver disconnect the terminal resister. Only valid for clock lane.
15:8	R/W	0x0	LPRX_TO The timeout counter for receiver in LP mode.
7:6	/	/	/
5	R/W	0x0	HSRX_SYNC_ERR_TO_EN 0: Disable 1: Enable HSRX_SYNC_ERR_TO counter
4	R/W	0x0	HSRX_CLK_MISS_EN 0: Disable 1: Enable HSRX_CLK_MISS counter
3:2	/	/	/
1	R/W	0x0	FREQ_CNT_EN 0:Disable 1:Enable When enabled, the FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Clock.
0	R/W	0x0	LPRX_TO_EN LP RX timeout enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.2.6.61. 0x1034 DPHY RX Timing Parameter 1 Register(Default Value: 0x0000_0000)

Offset:0x1034			Register Name: DPHY_RX_TIME1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	RX_DLY The time that DPhy process hs fifo data and pull off data valid signal to protocal after DPhy has detected the lane state from HS to LP. It should be more than 8 byte clock cycle time.
19:0	R/W	0x0	LPRX_ULPS_WP When recerivers detects MARK-I for ULPS Wakeup Cycles, the corresponding ULPS WP is pending. (Valid for clock lane and all data lane).

6.2.6.62. 0x1040 DPHY RX Timing Parameter 3 Register(Default Value: 0x0000_0000)

Offset:0x1040			Register Name: DPHY_RX_TIME3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	LPRST_DLY The added delayed time that reset the hs-fifo after the DPhy has detected the HS-to-LP.
15:0	R	0x0	FREQ_CNT The value of FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Cock.

6.2.6.63. 0x104C DPHY Analog 0 Register(Default Value: 0x0000_0044)

Offset:0x104C			Register Name: DPHY_ANA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	dsi_reg_preemph0 Data lane0 hstx preemphasis tuning.
19:16	R/W	0x0	dsi_reg_preemph1 Data lane1 hstx preemphasis tuning.
15:12	R/W	0x0	dsi_reg_preemph2 Data lane2 hstx preemphasis tuning.
11:8	R/W	0x0	dsi_reg_preemph3 Data lane3 hstx preemphasis tuning.
7	/	/	/
6:4	R/W	0x4	dsi_reg_lptx_setc LPtx current bias tuning.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	/	/	/
2:0	R/W	0x4	dsi_reg_lptx_setr LPtx output resistance tuning.

6.2.6.64. 0x1050 DPHY Analog 1 Register(Default Value: 0x0000_0000)

Offset:0x1050			Register Name: DPHY_ANA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	envtt_mode Hstx vtt enable.
30:27	/	/	/
26	R/W	0x0	dsi_en_phback_lock Back sync clk lock enable.
25	R/W	0x0	dsi_en_phback_sync Back sync clk enable.
24	R/W	0x0	dsi_en_soft_phsel Resister control enable for phase back clk.
23:22	R/W	0x0	dsi_reg_soft_phsel Resister tuning for phase back clk.
21:20	R/W	0x0	dsi_reg_phsync_set Set to digital clock phase for parallel data.
19:16	R/W	0x0	dsi_en_clkpatd Hstx clk pattern enable for data lane0 to lane3.
15	/	/	/
14:11	R/W	0x0	dsi_en_vtt_test Hstx vtt test enable for data lane0 to lane3.
10	R/W	0x0	dsi_en_vtt_testc Hstx vtt test enable for clk lane.
9:6	R/W	0x0	dsi_reg_hstx_plr Data lane0 to lane3 polar reverse.
5	R/W	0x0	dsi_reg_hstxck_plr Clk lane polar reverse.
4:1	R/W	0x0	dsi_en_vlptx_test Data lane0 to lane3 LPtx analog point test enable.
0	R/W	0x0	dsi_en_vlptx_testc Clk lane LPtx analog point test enable.

6.2.6.65. 0x1054 DPHY Analog 2 Register(Default Value: 0x0100_0F20)

Offset:0x1054			Register Name: DPHY_ANA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

27:24	R/W	0x1	EN_P2S Enable signal for HS p2s module in Data Lane<3:0>
23:12	/	/	/
11:8	R/W	0xF	EN_TXTERM Enable signal for HStx termination in Data Lane<3:0>
7:6	/	/	/
5	R/W	0x1	EN_TXTREMC Enable signal for HStx termination in Clock Lane
4	R/W	0x0	EN_CLK Enable signal for ref clock is active to MIPI. It can not be controlled by CPU. Set as "1"
3:2	/	/	/
1	R/W	0x0	EN_IREF Enable signal for current bias is active Set as "1"
0	R/W	0x0	ANA_CPU_EN Enable all register with cpu, when disable, those bits are control by circuit automatic

6.2.6.66. 0x1058 DPHY Analog 3 Register(Default Value: 0xF800_0000)

Offset:0x1058			**Register Name: DPHY_ANA3_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	EN_VDRVLDO_ON Enable Signal for HS TX LDO in Data Lane<3:0> Set as "1111" when hstx
27	R/W	0x1	EN_VDRVLDO_ONC Enable Signal for HS TX LDO in Clock Lane Set as "1" when hstx
26	R/W	0x0	EN_DIV2 Enable Signal for input clock divided by 2. Set as "1"
25	R/W	0x0	EN_LVCK Enable Signal for clock power LDO is active DSI set as "1"; CSI set as "0"
24	R/W	0x0	EN_LV Enable Signal for data power LDO is active Set as "1"
23	R/W	0x0	EN_ULPSC Data Lane<3:0> LP contention detect threshold tuning.
22:19	R/W	0x0	EN_ULPS CLK Lane LP contention detect threshold tuning.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

18	R/W	0x0	EN_VREF Enable signal for reference power LDO is active Set as "1"
17:15	/	/	/
14	R/W	0x0	EN_LPCDC Enable signal for LP cd module is active in Clock Lane
13	R/W	0x0	EN_LPTXC Enable signal for LP tx module is active in Clock Lane
12	R/W	0x0	EN_LPRXC Enable signal for LP rx module is active in Clock Lane
11:8	R/W	0x0	EN_LPCD Enable signal for LP cd module is active in Data Lane<3:0>
7:4	R/W	0x0	EN_LPRX Enable signal for LP rx module is active in Data Lane<3:0>
3:0	R/W	0x0	EN_LPTX Enable signal for LP tx module is active in Data Lane<3:0>

6.2.6.67. 0x105C DPHY Analog 4 Register(Default Value: 0x0000_0000)

Offset:0x105C			Register Name: DPHY_ANA4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	dsi_en_mipi Mipi dsi enable.
30	R/W	0x0	dsi_en_comtest Common test enable.
29:28	R/W	0x0	dsi_reg_comtest Common test select.
27	/	/	/
26:24	R/W	0x0	dsi_reg_ib Input bias current tuning.
23	/	/	/
22:20	R/W	0x0	dsi_reg_vres_set Res calibration reference voltage tuning.
19	/	/	/
18:16	R/W	0x0	dsi_reg_vtt_set Hstx reference voltage tuning.
15	/	/	/
14:12	R/W	0x0	dsi_reg_vlptx_set LPtx reference voltage tuning.
11	/	/	/
10:8	R/W	0x0	dsi_reg_vlv_set LDO voltage tuning for core power.
7	R/W	0x0	dsi_en_rescal

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Resistance calibration enable.
6	R/W	0x0	dsi_on_rescal Resistance calibration on.
5	R/W	0x0	dsi_en_soft_rcal Software Resistance calibration enable.
4:0	R/W	0x0	dsi_reg_soft_rcal Software Resistance calibration tuning.

6.2.6.68. 0x1060 DPHY Interrupt Enable 0 Register(Default Value: 0x0000_0000)

Offset:0x1060			Register Name: DPHY_INT_EN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CD_LP1_ERR_D3_INT Contention Detection detects LP1 error interrupt
30	R/W	0x0	CD_LP0_ERR_D3_INT Contention Detection detects LP0 error interrupt
29	R/W	0x0	CD_LP1_ERR_D2_INT Contention Detection detects LP1 error interrupt
28	R/W	0x0	CD_LP0_ERR_D2_INT Contention Detection detects LP0 error interrupt
27	R/W	0x0	CD_LP1_ERR_D1_INT Contention Detection detects LP1 error interrupt
26	R/W	0x0	CD_LP0_ERR_D1_INT Contention Detection detects LP0 error interrupt
25	R/W	0x0	CD_LP1_ERR_D0_INT Contention Detection detects LP1 error interrupt
24	R/W	0x0	CD_LP0_ERR_D0_INT Contention Detection detects LP0 error interrupt
23	R/W	0x0	CD_LP1_ERR_CLK_INT Contention Detection detects LP1 error interrupt
22	R/W	0x0	CD_LP0_ERR_CLK_INT Contention Detection detects LP0 error interrupt
21:16	/	/	/
15	R/W	0x0	RX_ALG_ERR_D3_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
14	R/W	0x0	RX_ALG_ERR_D2_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
13	R/W	0x0	RX_ALG_ERR_D1_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
12	R/W	0x0	RX_ALG_ERR_D0_INT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W	0x0	SOT_SYNC_ERR_D3_INT DPHY RX can not detected SOT sequence at Data Lane 0 interrupt.
10	R/W	0x0	SOT_SYNC_ERR_D2_INT DPHY RX can not detected SOT sequence at Data Lane 0 interrupt.
9	R/W	0x0	SOT_SYNC_ERR_D1_INT DPHY RX can not detected SOT sequence at Data Lane 0 interrupt.
8	R/W	0x0	SOT_SYNC_ERR_D0_INT DPHY RX can not detected SOT sequence at Data Lane 0 interrupt.
7	R/W	0x0	SOT_ERR_D3_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
6	R/W	0x0	SOT_ERR_D2_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
5	R/W	0x0	SOT_ERR_D1_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
4	R/W	0x0	SOT_ERR_D0_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
3	R/W	0x0	SOT_D3_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 3 interrupt.
2	R/W	0x0	SOT_D2_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 2 interrupt.
1	R/W	0x0	SOT_D1_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 1 interrupt.
0	R/W	0x0	SOT_D0_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 0 interrupt.

6.2.6.69. 0x1064 DPHY Interrupt Enable 1 Register(Default Value: 0x0000_0000)

Offset:0x1064			Register Name: DPHY_INT_EN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	R/W	0x0	FALSE_CTL_D3_INT A false control occurs at Data Lane 3 interrupt.
30	R/W	0x0	FALSE_CTL_D2_INT A false control occurs at Data Lane 2 interrupt.
29	R/W	0x0	FALSE_CTL_D1_INT A false control occurs at Data Lane 1 interrupt.
28	R/W	0x0	FALSE_CTL_D0_INT A false control occurs at Data Lane 0 interrupt.
27	R/W	0x0	ESC_CMD_ERR_D3_INT DPHY RX received can not recognize the Escape Entry Command at Data Lane 3 interrupt.
26	R/W	0x0	ESC_CMD_ERR_D2_INT DPHY RX received can not recognize the Escape Entry Command at Data Lane 2 interrupt.
25	R/W	0x0	ESC_CMD_ERR_D1_INT DPHY RX received can not recognize the Escape Entry Command at Data Lane 1 interrupt.
24	R/W	0x0	ESC_CMD_ERR_D0_INT DPHY RX received can not recognize the Escape Entry Command at Data Lane 0 interrupt.
23	R/W	0x0	RST_D3_INT DPHY RX detected Reset Trigger sequence at Data Lane 3 interrupt.
22	R/W	0x0	RST_D2_INT DPHY RX detected Reset Trigger sequence at Data Lane 2 interrupt.
21	R/W	0x0	RST_D1_INT DPHY RX detected Reset Trigger sequence at Data Lane 1 interrupt.
20	R/W	0x0	RST_D0_INT DPHY RX detected Reset Trigger sequence at Data Lane 0 interrupt.
19	R/W	0x0	UNDEF5_D0_INT DPHY RX received undefined 5 sequence at Data Lane 0 interrupt.
18	R/W	0x0	UNDEF4_D0_INT DPHY RX received undefined 4 sequence at Data Lane 0 interrupt.
17	R/W	0x0	UNDEF3_D0_INT DPHY RX received undefined 3 sequence at Data Lane 0 interrupt.
16	R/W	0x0	UNDEF2_D0_INT DPHY RX received undefined 2 sequence at Data Lane 0 interrupt.
15	R/W	0x0	UNDEF1_D0_INT DPHY RX received undefined 1 sequence at Data Lane 0 interrupt.
14	R/W	0x0	TX_TRND_ERR_D0_INT DPHY TX turn around error at Data Lane 0 interrupt.
13	R/W	0x0	RX_TRND_D0_INT DPHY RX received turn around sequence at Data Lane 0 interrupt.
12	R/W	0x0	LPDT_D0_INT DPHY RX complete LPDT transfer at Data Lane 0 interrupt.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:10	/	/	/
9	R/W	0x0	ULPS_WP_CLK_INT DPHY RX detected ULPS wakeup at Clock Lane interrupt.
8	R/W	0x0	ULPS_CLK_INT DPHY RX detected ULPS sequence at Clock Lane interrupt.
7	R/W	0x0	ULPS_WP_D3_INT DPHY RX detected ULPS wakeup at Data Lane 3 interrupt.
6	R/W	0x0	ULPS_WP_D2_INT DPHY RX detected ULPS wakeup at Data Lane 2 interrupt.
5	R/W	0x0	ULPS_WP_D1_INT DPHY RX detected ULPS wakeup at Data Lane 1 interrupt.
4	R/W	0x0	ULPS_WP_D0_INT DPHY RX detected ULPS wakeup at Data Lane 0 interrupt.
3	R/W	0x0	ULPS_D3_INT DPHY RX detected ULPS sequence at Data Lane 3 interrupt.
2	R/W	0x0	ULPS_D2_INT DPHY RX detected ULPS sequence at Data Lane 2 interrupt.
1	R/W	0x0	ULPS_D1_INT DPHY RX detected ULPS sequence at Data Lane 1 interrupt.
0	R/W	0x0	ULPS_D0_INT DPHY RX detected ULPS sequence at Data Lane 0 interrupt.

6.2.6.70. 0x1070 DPHY Interrupt Pending 0 Register(Default Value: 0x0000_0000)

Offset:0x1070			**Register Name: DPHY_INT_PD0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CD_LP1_ERR_D3_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
30	R/W	0x0	CD_LP0_ERR_D3_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
29	R/W	0x0	CD_LP1_ERR_D2_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
28	R/W	0x0	CD_LP0_ERR_D2_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
27	R/W	0x0	CD_LP1_ERR_D0_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
26	R/W	0x0	CD_LP0_ERR_D0_PD Contention Detection detects LP0 error interrupt pending. Write "1" to

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			clear.
25	R/W	0x0	CD_LP1_ERR_D1_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
24	R/W	0x0	CD_LP0_ERR_D1_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
23	R/W	0x0	CD_LP1_ERR_CLK_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
22	R/W	0x0	CD_LP0_ERR_CLK_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
21:16	/	/	/
15	R/W	0x0	RX_ALG_ERR_D3_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
14	R/W	0x0	RX_ALG_ERR_D2_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
13	R/W	0x0	RX_ALG_ERR_D1_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
12	R/W	0x0	RX_ALG_ERR_D0_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W	0x0	SOT_SYNC_ERR_D3_PD Asserted if DPHY RX cant not detected SOT sequence at Data Lane 3. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
10	R/W	0x0	SOT_SYNC_ERR_D2_PD Asserted if DPHY RX cant not detected SOT sequence at Data Lane 2. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
9	R/W	0x0	SOT_SYNC_ERR_D1_PD Asserted if DPHY RX cant not detected SOT sequence at Data Lane 1. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
8	R/W	0x0	SOT_SYNC_ERR_D0_PD Asserted if DPHY RX cant not detected SOT sequence at Data Lane 0. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
7	R/W	0x0	SOT_ERR_D3_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 3. The confidence in the payload data is lower. Write "1" to clear.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6	R/W	0x0	SOT_ERR_D2_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 2. The confidence in the payload data is lower. Write "1" to clear.
5	R/W	0x0	SOT_ERR_D1_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 1. The confidence in the payload data is lower. Write "1" to clear.
4	R/W	0x0	SOT_ERR_D0_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 0. The confidence in the payload data is lower. Write "1" to clear.
3	R/W	0x0	SOT_D3_PD Asserted if DPHY RX detected SOT sequence at Data Lane 3.Write "1" to clear.
2	R/W	0x0	SOT_D2_PD Asserted if DPHY RX detected SOT sequence at Data Lane 2.Write "1" to clear.
1	R/W	0x0	SOT_D1_PD Asserted if DPHY RX detected SOT sequence at Data Lane 1.Write "1" to clear.
0	R/W	0x0	SOT_D0_PD Asserted if DPHY RX detected SOT sequence at Data Lane 0.Write "1" to clear.

6.2.6.71. 0x1074 DPHY Interrupt Pending 1 Register(Default Value: 0x0000_0000)

Offset:0x1074			Register Name: DPHY_INT_PD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FALSE_CTL_D3_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
30	R/W	0x0	FALSE_CTL_D2_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
29	R/W	0x0	FALSE_CTL_D1_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
28	R/W	0x0	FALSE_CTL_D0_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
27	R/W	0x0	ESC_CMD_ERR_D3_PD Asserted if DPHY RX received can not recognize the Escape Entry

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Command at Data Lane 3. Write "1" to clear.
26	R/W	0x0	ESC_CMD_ERR_D2_PD Asserted if DPHY RX received can not recognize the Escape Entry Command at Data Lane 2. Write "1" to clear.
25	R/W	0x0	ESC_CMD_ERR_D1_PD Asserted if DPHY RX received can not recognize the Escape Entry Command at Data Lane 1. Write "1" to clear.
24	R/W	0x0	ESC_CMD_ERR_D0_PD Asserted if DPHY RX received can not recognize the Escape Entry Command at Data Lane 0. Write "1" to clear.
23	R/W	0x0	RST_D3_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 3.Write "1" to clear.
22	R/W	0x0	RST_D2_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 2.Write "1" to clear.
21	R/W	0x0	RST_D1_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 1.Write "1" to clear.
20	R/W	0x0	RST_D0_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 0.Write "1" to clear.
19	R/W	0x0	UNDEF5_D0_PD Asserted if DPHY RX received undefined 5 sequence at Data Lane 0. Write "1" to clear. "10100000"
18	R/W	0x0	UNDEF4_D0_PD Asserted if DPHY RX received undefined 4 sequence at Data Lane 0. Write "1" to clear. "00100001"
17	R/W	0x0	UNDEF3_D0_PD Asserted if DPHY RX received undefined 3 sequence at Data Lane 0. Write "1" to clear. "01011101"
16	R/W	0x0	UNDEF2_D0_PD Asserted if DPHY RX received undefined 2 sequence at Data Lane 0 . Write "1" to clear. "11011110"
15	R/W	0x0	UNDEF1_D0_PD Asserted if DPHY RX received undefined 1 sequence at Data Lane 0. Write "1" to clear. "10011111"
14	R/W	0x0	TX_TRND_ERR_D0_PD Asserted if DPHY TX turn around error at Data Lane 0. Write "1" to clear.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

13	R/W	0x0	RX_TRND_D0_PD Asserted if DPHY RX received turn around sequence at Data Lane 0. Write "1" to clear.
12	R/W	0x0	LPDT_D0_PD Asserted if DPHY RX complete LPDT transfer at Data Lane 0 .Write "1" to clear. "11100001"
11:10	/	/	/
9	R/W	0x0	ULPS_WP_CLK_PD Asserted if DPHY RX detected ULPS wakeup at Clock Lane. Write "1" to clear.
8	R/W	0x0	ULPS_CLK_PD Asserted if DPHY RX detected ULPS sequence at Clock Lane. Write "1" to clear.
7	R/W	0x0	ULPS_WP_D3_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 3. Write "1" to clear.
6	R/W	0x0	ULPS_WP_D2_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 2. Write "1" to clear.
5	R/W	0x0	ULPS_WP_D1_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 1. Write "1" to clear.
4	R/W	0x0	ULPS_WP_D0_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 0. Write "1" to clear.
3	R/W	0x0	ULPS_D3_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 3. Write "1" to clear.
2	R/W	0x0	ULPS_D2_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 2. Write "1" to clear.
1	R/W	0x0	ULPS_D1_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 1. Write "1" to clear.
0	R/W	0x0	ULPS_D0_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 0. Write "1" to clear. "00011110"

6.2.6.72. 0x10E0 DPHY Debug 0 Register(Default Value: 0x0000_0000)

Offset: 0x10E0	Register Name: DPHY_DBG0_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	DIRECTION 0:No lane switch into HS transmission 1:At least one lane switch into HS transmission
27:26	/	/	/
25	R	0x0	Soft_rcal_cmpo Resistance calibration comparator output.
24	R	0x0	Soft_rcal_flag Resistance calibration completion flag.
23:19	R	0x0	Soft_rcal_value Resistance calibration bit return to system.
18:16	R	0x0	LPTX_STA_CLK 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
15	/	/	/
14:12	R	0x0	LPTX_STA_D3 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
11	/	/	/
10:8	R	0x0	LPTX_STA_D2 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
7	/	/	/
6:4	R	0x0	LPTX_STA_D1 000: STP_ST 001: HSRQ_ST

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
3	/	/	/
2:0	R	0x0	LPTX_STA_D0 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST

6.2.6.73. 0x10E4 DPHY Debug 1 Register(Default Value: 0x0000_0000)

Offset: 0x10E4			Register Name: DPHY_DBG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	LPTX_SET_CK Clock Lane output state 00: LP-00 01: LP-01 10: LP-10 11: LP-11
11:10	R/W	0x0	LPTX_SET_D3 Data Lane 3 output state 00: LP-00 01: LP-01 10: LP-10 11: LP-11
9:8	R/W	0x0	LPTX_SET_D2 Data Lane 2 output state 00: LP-00 01: LP-01 10: LP-10 11: LP-11
7:6	R/W	0x0	LPTX_SET_D1 Data Lane 1 output state 00: LP-00 01: LP-01

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: LP-10 11: LP-11
5:4	R/W	0x0	LPTX_SET_D0 Data Lane 0 output state 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3:2	/	/	/
1	R/W	0x0	HSTX_DBG_EN 0: normal mode 1: debug mode
0	R/W	0x0	LPTX_DBG_EN 0: normal mode 1: debug mode

6.2.6.74. 0x10E8 DPHY Debug 2 Register(Default Value: 0x0000_0000)

Offset: 0x10E8			Register Name: DPHY_DBG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HSTX_Data Bit31-24: D3_DATA Bit23-16: D2_DATA Bit15-08: D1_DATA Bit07-00: D0_DATA

6.2.6.75. 0x10EC DPHY Debug 3 Register(Default Value: 0x0000_0000)

Offset:0x10EC			Register Name: DPHY_DBG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R	0x0	LPRX_STA_CLK 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S
15:12	R	0x0	LPRX_STA_D3 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S
11:8	R	0x0	LPRX_STA_D2 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S
7:4	R	0x0	LPRX_STA_D1 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S
3:0	R	0x0	LPRX_STA_D0 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010: UDF1S 1011: UDF2S 1100: UDF3S 1101: UDF4S 1110: UDF5S

6.2.6.76. 0x10F0 DPHY Debug 4 Register(Default Value: 0x0000_0000)

Offset:0x10F0			Register Name: DPHY_DBG4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	LPCD_PHY_CLK 00: LP-00 01: LP-01 10: LP-10 11: LP-11
23:22	R	0x0	LPCD_PHY_D3 00: LP-00 01: LP-01 10: LP-10 11: LP-11
21:20	R	0x0	LPCD_PHY_D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19:18	R	0x0	LPCD_PHY_D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
17:16	R	0x0	LPCD_PHY_D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11
15:10	/	/	/
9:8	R	0x0	LPRX_PHY_CLK 00: LP-00 01: LP-01 10: LP-10 11: LP-11
7:6	R	0x0	LPRX_PHY_D3 00: LP-00 01: LP-01 10: LP-10 11: LP-11
5:4	R	0x0	LPRX_PHY_D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3:2	R	0x0	LPRX_PHY_D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
1:0	R	0x0	LPRX_PHY_D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11

6.2.6.77. 0x10F4 DPHY Debug 5 Register(Default Value: 0x0000_0000)

Offset:0x10F4			Register Name: DPHY_DBG5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HSRX_DATA Bit31-24: LANE_D3 Bit23-16: LANE_D2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Bit15-08: LANE_D1 Bit07-00: LANE_D0

6.2.6.78. 0x10F8 DPHY TX Skew Register0(Default Value: 0x0000_0000)

Offset:0x10F8			Register Name: DPHY_TX_SKEW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	SKEWCAL_zero_set The time length of HS-Zero in Skew Calibration mode Its unit is byteclk.
23:16	R/W	0x0	SKEWCAL_trail_set The time length of HS-Trail in Skew Calibration mode Its unit is byteclk.
15:8	R/W	0x0	reg_skewcal Clock Pattern Content : 8'b0101_0101/8'b1010_1010
7:0	R/W	0x0	reg_skewcal_sync Skewcal sync Pattern Content : 8'b1111_1111

6.2.6.79. 0x10FC DPHY TX Skew Register1(Default Value: 0x0000_0000)

Offset:0x10FC			Register Name: DPHY_TX_SKEW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	SKEWCAL_sync_set The time length of SkewCal-Sync. Its unit is byteclk.
23:16	R/W	0x0	SKEWCAL_pedic_set The time length of Periodic mode SkewCal Its unit is byteclk.
15:0	R/W	0x0	SKEWCAL_init_set The time length of Initial mode SkewCal Its unit is byteclk.

6.2.6.80. 0x1100 DPHY TX Skew Register2(Default Value: 0x0000_0000)

Offset:0x1100			Register Name: DPHY_TX_SKEW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
10	R/W	0x0	en_skewcal_init
9	R/W	0x0	en_skewcal_perdic
8	R/W	0x0	skewcal_trail_inv
7:0	R/W	0x0	SKEWCAL_PREPARE_LP00 The time length of LP-00.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Its unit is byteclk.

6.2.6.81. 0x1104 DPHY PLL Register0(Default Value: 0x00F0_3283)

Offset:0x1104			Register Name: DPHY_PLL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
23	R/W	0x1	cp36_en enable signal of cp for 3.3V voltage
22	R/W	0x1	ldo_en enable signal of 0.9V LDO for V &dV
21	R/W	0x1	en_lvs enable gating for l2h level_shift
20	R/W	0x1	pll_en enable_signal for PLL
19:16	R/W	0x0	p<3:0> pre divider = p+1;
15:8	R/W	0x32	n<7:0> feedback divider = n, except 0;
7	R/W	0x1	ndet n detection
6	R/W	0x0	tdiv
5:4	R/W	0x0	m0<1:0> post divider0= 1/2/4
3:0	R/W	0x3	m1<3:0> post divider1= m1+1

6.2.6.82. 0x1108 DPHY PLL Register1(Default Value: 0x0000_0481)

Offset:0x1108			Register Name: DPHY_PLL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x0	unlock_mdsel 00: 21-29 clock cycles 01: 22-28 clock cycles
13	R/W	0x0	lockmdsel 0: 24-26 clock cycles 1: 23-27 clock cycles
12	R/W	0x0	lockdet_en 0: disable 1: enable
11:9	R/W	0x2	vseta<2:0> ref voltage regulation for LDO V 0.8,0.85,0.9,0.95,1.0,1.05,1.1,1.15

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8:6	R/W	0x2	vsetd<2:0> ref voltage regulation for LDO dV 0.8,0.85,0.9,0.95,1.0,1.05,1.1,1.15
5	R/W	0x0	lpf_sw charge pump current regulation
4:3	R/W	0x0	icp_sel<1:0> Charge pump current sel & regulate icpsel<1>: current regulate; icpsel<0>: 0 for ibias current; 1 for self-bias current;
2:1	R/W	0x0	atest_sel<1:0> 00: dv 01: v 10: icp 11: vc_od
0	R/W	0x1	test_en test enable for ck_test & ana_test

6.2.6.83. 0x1110 COMBO PHY Register0(Default Value: 0x0000_0000)

Offset:0x1110			Register Name: COMBO_PHY_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	en_test_comboldo comboldo ldo test enable
4	R/W	0x0	en_test_0p8 0p8 ldo test enable
3	R/W	0x0	en_mipi mipi phy enable
2	R/W	0x0	en_lvds lvds phy enable
1	R/W	0x0	en_comboldo comboldo enable
0	R/W	0x0	en_cp charge pump enable

6.2.6.84. 0x1114 COMBO PHY Register1(Default Value: 0x0000_0000)

Offset:0x1114			Register Name: COMBO_PHY_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
6:4	R/W	0x0	reg_vref1p6 vref1p6 tuning
3	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2:0	R/W	0x0	reg_vref0p8 vref0p8 tuning

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 7 ISP 528
7.1. Overview 528
7.2. Block Diagram 529
7.3. Module Functions 529
7.3.1. TDM 529
7.3.2. Crop 529
7.3.3. BLC 530
7.3.4. Digital Gain 530
7.3.5. DPC 530
7.3.6. Crosstalk Correction 530
7.3.7. GCA 530
7.3.8. 2D De-noise 530
7.3.9. WB 530
7.3.10. LSC 530
7.3.11. Bayer Interpolation 531
7.3.12. Sharpen 531
7.3.13. LCA 531
7.3.14. Color Matrix 531
7.3.15. CNR 531
7.3.16. SATU 531
7.3.17. DRC 531
7.3.18. Gamma 532
7.3.19. RGB2YCrCb 532
7.3.20. CEM 532

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 7- 1. ISP Block Diagram 529

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 7 ISP

7.1. Overview

The ISP module supports online/offline image process for RAW sensor. The main functions are as follows.

- Time Division Multiplexing(TDM)
- Crop
- Black level correction(BLC)
- Linearity correction
- Digital gain
- Defect pixel correction(DPC)
- Crosstalk correction
- Global chromatic aberration correction(GCA)
- 2D denoise fileter
- White balance(WB)
- Lens shading correction(LSC)
- Bayer interpolation
- Local chromatic aberration correction(LCA)
- Sharpening
- Color matrix
- Chrominance noise reduction(CNR)
- Saturation adjust
- RGB Dynamic range compression(DRC)
- RGB Gamma correction
- RGB2YCbCr
- Color enhance management
- 3A statistic output
- Anti-flick detection statistics
- Histogram statistics

The processing capability of the ISP module is as follows.

- Supports 8/10/12 bits RAW data input
- supports one sensor in online mode, or two sensors in offline mode
- Supports maximum 16x fps difference among two input cameras
- Online mode: maximum picture resolution of 3264 x 3264, maximum frame rate of 8M@30fps
- Offline mode: maximum picture resolution of 4224 x 4224, maximum frame rate of 13M@10fps
- Minimum picture resolution of 256 x 128
- Minimum horizontal blanking region of 96 pixels

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Minimum vertical blanking region of 40 lines

7.2. Block Diagram

The block diagram of the ISP module is as follows.

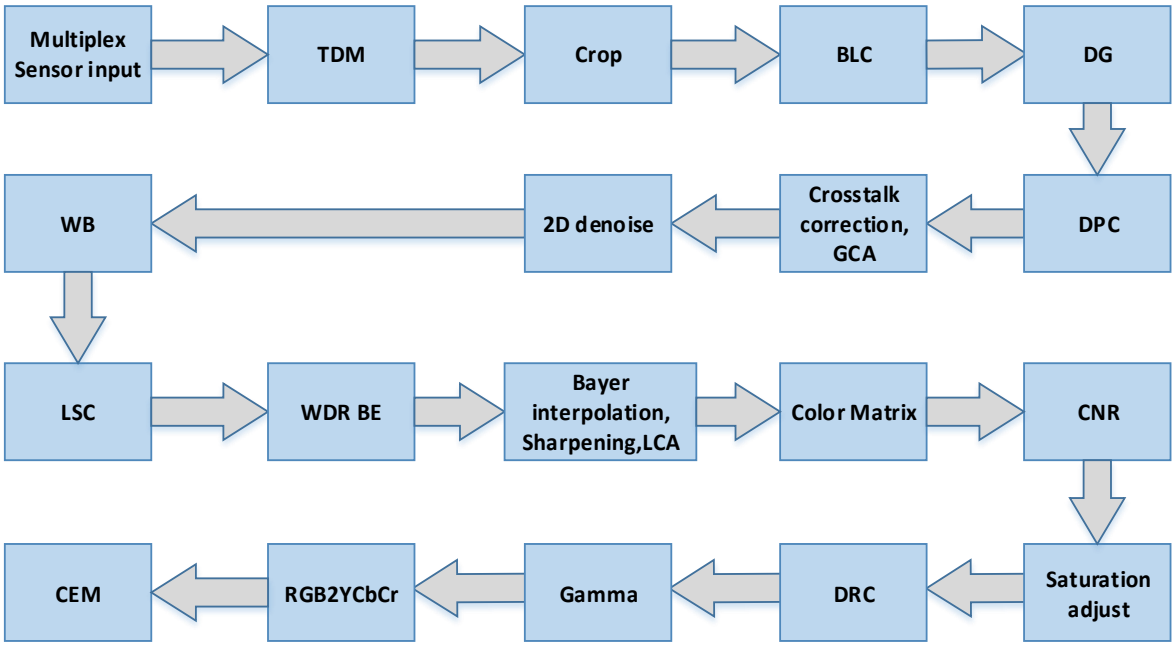


Figure 7- 1. ISP Block Diagram

7.3. Module Functions

7.3.1. TDM

The TDM module can support two input cameras simultaneously.

7.3.2. Crop

The Crop module can crop the input picture, and often be used to change the aspect ratio of the input picture or extract the region of interest for a picture.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.3.3. BLC

The BLC module adds respectively offset for four Bayer color channels(R,Gr,Gb,and B), to perform optical black correction. The precision of the offset is S13. The module is usually used for wide dynamic sensor.

7.3.4. Digital Gain

The Digital Gain module provides the digital gain, and supports U16Q10-precision.

7.3.5. DPC

The DPC module is used to correct defect pixels in Bayer field. It supports correct the type of defective pixel: Singlet dead pixel; doublet dead pixel in 5x5 kernel; and other cluster of defect pixel.

7.3.6. Crosstalk Correction

The Crosstalk Correction module is used to remove abnormal picture question when Gr and Gb imbalance. Usually, the module is used when sensor CRA unmatches lens CRA.

7.3.7. GCA

The GCA module is used to correction of Lateral Chromatic Aberration, which is one of the common optical defects of camera lens.

7.3.8. 2D De-noise

The 2D De-noise module restrains sensor noises in the Bayer field to improve picture quality.

7.3.9. WB

The WB Correction module adds respectively gain for four channels(R, Gr ,Gb, and B) to implement white balance correction. The precision of the gain is U12Q8.

7.3.10. LSC

The LSC module implements lens shading correction. It supports two way of mesh(MSC) and radio(RSC), which interpolate the shading correction coefficient by the radio distance and pixel block statistics.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.3.11. Bayer Interpolation

The module interpolates Bayer field pixel to RGB field while holding clear picture edge and restraining pseudo color.

7.3.12. Sharpen

The Sharpen module implements picture edge sharpening to improve picture edge information, while picture contour is much clearer.

7.3.13. LCA

The LCA module is used to correction of Axial Chromatic Aberration, which is one of the common optical defects of camera lens.

7.3.14. Color Matrix

The Color Matrix module applies a 3x3 color gain matrix and a 3x1 offset matrix on the input R/G/B pixels to restore image color. The precision of each value in gain matrix is S12Q8 and the precision of each value in offset matrix is S13.

$$\begin{pmatrix} R_out \\ G_out \\ B_out \end{pmatrix} = \begin{pmatrix} g_{rr} & g_{gr} & g_{br} \\ g_{rg} & g_{gg} & g_{bg} \\ g_{rb} & g_{gb} & g_{bb} \end{pmatrix} \times \begin{pmatrix} R_in \\ G_in \\ B_in \end{pmatrix} + \begin{pmatrix} offset_R \\ offset_G \\ offset_B \end{pmatrix}$$

7.3.15. CNR

The CNR module is used to reduce chroma noise in RGB domain.

7.3.16. SATU

Saturation adjust module is used to adjust the saturation of image.

7.3.17. DRC

The DRC module performs a gamma correction for each color in the RGB color space.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.3.18. Gamma

The Gamma module applies gamma correction for each color channel(R,G,and B) through looking-up table. Each gamma table has 256 entries and the precision is U12.

7.3.19. RGB2YCrCb

The RGB2YCrCb module convert RGB color space to YCbCr color space by using a 3x3 squre matrix with an added offset. Each gain range is U10Q10 precision.

7.3.20. CEM

The CEM module adjusts hue and saturation of picture in YUV field, and enhances or restrains specific colors such as blue sky, plant and complexion based on user preference.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 8 Video Input Interfaces....536
8.1. CSIC....536
8.1.1. Overview....536
8.1.2. Block Diagram....536
8.1.3. Operations and Functional Descriptions....537
8.1.4. Register List....539
8.1.5. CCU Register Description....543
8.1.6. CSIC Top Register Description....545
8.1.7. Parser Register Description....564
8.1.8. CSIC DMA Register Description....580

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 8- 1. CSIC Block Diagram 536
Figure 8- 2. RAW-10 Format 538
Figure 8- 3. RAW-12 Format 538
Figure 8- 4. Y of YUV-10 Format 538
Figure 8- 5. UV Combined of YUV-10 Format 538
Figure 8- 6. RGB888 Format 538
Figure 8- 7. PRGB888 Format 539
Figure 8- 8. RGB565 Format 539

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 8- 1. CSIC External Signals 537
Table 8- 2. CSIC FIFO Distribution 537

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 8 Video Input Interfaces

8.1. CSIC

8.1.1. Overview

The CMOS Sensor Interface Controller(CSIC) is an image or video input control module which can receive image or video data via camera interface(MIPI). The controller can transfer valid data to embedded ISP or store the data in memory directly.

The CSIC includes the following features:

- Supports 2 serial interfaces(one for MIPI 4-lane, the other for MIPI 2-lane)
- Supports image crop function
- Supports MIPI Version 1.0
- Up to 1.0Gbps/Lane
- Maximum video capture resolution for serial interface up to 8M@30fps(online mode) or 13M@10fps(offline mode) or 4*1080p@25fps(de-interleaver conversion chip)

8.1.2. Block Diagram

Figure 8-1 shows a function block diagram of the CSIC. The CSIC consists of Input Parser, ISP, VIPP and DMA Control. In addition, the controller has 2 Input Parsers, 1 ISP, 4 VIPPs and 4 DMAs.

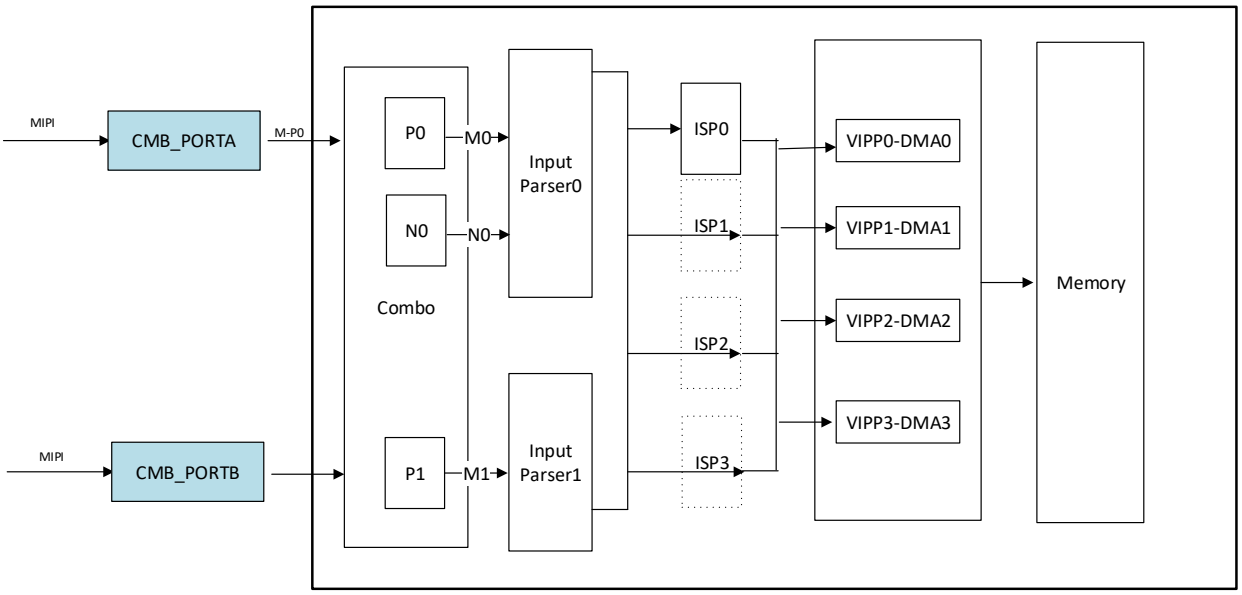


Figure 8- 1. CSIC Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

Table 8- 1. CSIC External Signals

Signal	Description	Type
MCSIA_CKN	MIPI CSI controller A clock negative signal	AI
MCSIA_CKP	MIPI CSI controller A clock positive signal	AI
MCSIA_D0N	MIPI CSI controller A data0 negative signal	AI
MCSIA_D0P	MIPI CSI controller A data0 positive signal	AI
MCSIA_D1N	MIPI CSI controller A data1 negative signal	AI
MCSIA_D1P	MIPI CSI controller A data1 positive signal	AI
MCSIA_D2N	MIPI CSI controller A data2 negative signal	AI
MCSIA_D2P	MIPI CSI controller A data2 positive signal	AI
MCSIA_D3N	MIPI CSI controller A data3 negative signal	AI
MCSIA_D3P	MIPI CSI controller A data3 positive signal	AI
MCSIB_CKN	MIPI CSI controller B clock negative signal	AI
MCSIB_CKP	MIPI CSI controller B clock positive signal	AI
MCSIB_D0N	MIPI CSI controller B data0 negative signal	AI
MCSIB_D0P	MIPI CSI controller B data0 positive signal	AI
MCSIB_D1N	MIPI CSI controller B data1 negative signal	AI
MCSIB_D1P	MIPI CSI controller B data1 positive signal	AI
VCC_MCSI	MIPI CSI power supply	P
MIPI_MCLK0	MIPI CSI controller A master clock	O
MIPI_MCLK1	MIPI CSI controller B master clock	O
CSI_SM_VS	MIPI CSI slave mode vertical SYNC	O

8.1.3.2. Typical Application

The CSIC has 2 input ports and 4 DMA, which means it can support 2 port input and 4 video streams output to memory simultaneously at most. This makes the applications very flexible.

The CSIC supports following input case:

- 2 serial inputs(1 four-lane and 1 two-lane)

8.1.3.3. CSIC FIFO Distribution

Table 8- 2. CSIC FIFO Distribution

Interface	MIPI Interface

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Input format	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB/PRGB
CH0_FIFO0	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-

8.1.3.4. Pixel Format Arrangement

RAW-10:

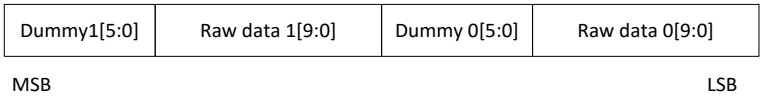


Figure 8- 2. RAW-10 Format

RAW-12:

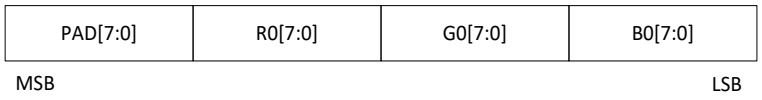


Figure 8- 3. RAW-12 Format

YUV-10:

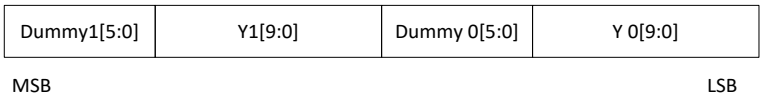


Figure 8- 4. Y of YUV-10 Format

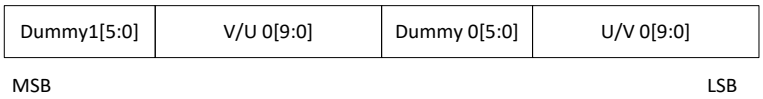


Figure 8- 5. UV Combined of YUV-10 Format

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

Figure 8- 6. RGB888 Format

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PRGB888:

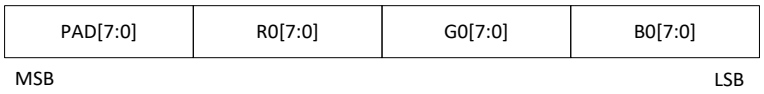


Figure 8- 7. PRGB888 Format

RGB565:

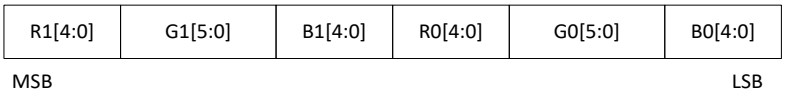


Figure 8- 8. RGB565 Format

8.1.3.5. Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.
For YUV422 format, pixel unit is a YU/YV combination.
For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer and RAW format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is 2 bytes of RGB565 package.
For RGB888, pixel unit is 3 bytes of RGB combination.

8.1.3.6. Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.
If horizontal flip is enabled, one or more pixels will be took as a unit:
For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.
For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.
For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

8.1.4. Register List

Module Name	Base Address
CSIC_BASE	0x02000000
CSIC_CCU	0x02000000

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_TOP	0x02000800
CSIC_PARSER0	0x02001000
CSIC_PARSER1	0x02002000
CSIC_DMA0	0x02009000
CSIC_DMA1	0x02009200
CSIC_DMA2	0x02009400
CSIC_DMA3	0x02009600
CSIC_COMBO	0x0200A000
CSIC_ISP0	0x02100000
CSIC_ISP1	0x02102000
CSIC_TDM	0x02108000
CSIC_VIPP0	0x02110000
CSIC_VIPP1	0x02110400
CSIC_VIPP2	0x02110800
CSIC_VIPP3	0x02110C00

CCU register list:

Register Name	Offset	Register Description
CCU_CLK_MODE_REG	0x0000	CCU Clock Mode Register
CCU_PARSER_CLK_EN_REG	0x0004	CCU Parser Clock Enable Register
CCU_ISP_CLK_EN_REG	0x0008	CCU ISP Clock Enable Register
CCU_POST0_CLK_EN_REG	0x000C	CCU Post0 Clock Enable Register

CSIC TOP register list:

Register Name	Offset	Register Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004c	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge Buffer Maxuse Counter Register
CSIC_ISP1_BRG_BUF_MAXUSE_CNT_REG	0x007C	CSIC ISP1 Bridge Buffer Maxuse Counter Register
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
CSIC_ISP1_BRG_INT_EN_REG	0x0088	CSIC ISP1 Bridge Interrupt Enable Register
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
CSIC_ISP1_BRG_INT_PD_REG	0x0090	CSIC ISP1 Bridge Interrupt Pending Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_BIST_CS_REG	0x00DC	CSIC BIST CS Register
CSIC_BIST_CONTROL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_REG	0x00E4	CSIC BIST Start Register
CSIC_BIST_END_REG	0x00E8	CSIC BIST End Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature list Register

PARSER0/1 register list:

Register Name	**Offset**	**Register Description**
PRS_EN_REG	0x0000	Parser Enable Register
PRS_MCSIC_IF_CFG_REG	0x0008	Parser MCSIC Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register
PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA1_REG	0x0034	Parser Channel_0 Input Parameter1 Register
PRS_C0_INPUT_PARA2_REG	0x0038	Parser Channel_0 Input Parameter2 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
PRS_CH0_LINE_TIME_REG	0x0048	Parser Channel_0 Line Time Register
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PRS_C1_INPUT_PARA1_REG	0x0134	Parser Channel_1 Input Parameter1 Register
PRS_C1_INPUT_PARA2_REG	0x0138	Parser Channel_1 Input Parameter2 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
PRS_CH1_LINE_TIME_REG	0x0148	Parser Channel_1 Line Time Register
PRS_C2_INFMT_REG	0x0224	Parser Channel_2 Input Format Register
PRS_C2_OUTPUT_HSIZE_REG	0x0228	Parser Channel_2 Output Horizontal Size Register
PRS_C2_OUTPUT_VSIZE_REG	0x022C	Parser Channel_2 Output Vertical Size Register
PRS_C2_INPUT_PARA0_REG	0x0230	Parser Channel_2 Input Parameter0 Register
PRS_C2_INPUT_PARA1_REG	0x0234	Parser Channel_2 Input Parameter1 Register
PRS_C2_INPUT_PARA2_REG	0x0238	Parser Channel_2 Input Parameter2 Register
PRS_C2_INPUT_PARA3_REG	0x023C	Parser Channel_2 Input Parameter3 Register
PRS_C2_INT_EN_REG	0x0240	Parser Channel_2 Interrupt Enable Register
PRS_C2_INT_STA_REG	0x0244	Parser Channel_2 Interrupt Status Register
PRS_CH2_LINE_TIME_REG	0x0248	Parser Channel_2 Line Time Register
PRS_C3_INFMT_REG	0x0324	Parser Channel_3 Input Format Register
PRS_C3_OUTPUT_HSIZE_REG	0x0328	Parser Channel_3 Output Horizontal Size Register
PRS_C3_OUTPUT_VSIZE_REG	0x032C	Parser Channel_3 Output Vertical Size Register
PRS_C3_INPUT_PARA0_REG	0x0330	Parser Channel_3 Input Parameter0 Register
PRS_C3_INPUT_PARA1_REG	0x0334	Parser Channel_3 Input Parameter1 Register
PRS_C3_INPUT_PARA2_REG	0x0338	Parser Channel_3 Input Parameter2 Register
PRS_C3_INPUT_PARA3_REG	0x033C	Parser Channel_3 Input Parameter3 Register
PRS_C3_INT_EN_REG	0x0340	Parser Channel_3 Interrupt Enable Register
PRS_C3_INT_STA_REG	0x0344	Parser Channel_3 Interrupt Status Register
PRS_CH3_LINE_TIME_REG	0x0348	Parser Channel_3 Line Time Register
PRS_CSIC_SYNC_EN_REG	0x0520	Parser CSIC SYNC Enable Register
PRS_CSIC_SYNC_CFG_REG	0x0524	Parser CSIC SYNC CFG Register
PRS_CSIC_SYNC_WAIT_N_REG	0x0528	Parser CSIC SYNC WAIT N Register
PRS_CSIC_SYNC_WAIT_M_REG	0x052C	Parser CSIC SYNC WAIT M Register

DMA0/1/2/3 register list:

CSIC_DMA_EN_REG	0x0000	CSIC DMA Enable Register
CSIC_DMA_CFG_REG	0x0004	CSIC DMA Configuration Register
CSIC_DMA_HSIZE_REG	0x0010	CSIC DMA Horizontal Size Register
CSIC_DMA_VSIZE_REG	0x0014	CSIC DMA Vertical Size Register
CSIC_DMA_F0_BUFA_REG	0x0020	CSIC DMA FIFO 0 Output Buffer-A Address Register
CSIC_DMA_F0_BUFA_RESULT_REG	0x0024	CSIC DMA FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_F1_BUFA_REG	0x0028	CSIC DMA FIFO 1 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x002C	CSIC DMA FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_F2_BUFA_REG	0x0030	CSIC DMA FIFO 2 Output Buffer-A Address Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CSIC_DMA_F1_BUFA_RESULT_REG	0x0034	CSIC DMA FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_BUF_LEN_REG	0x0038	CSIC DMA Buffer Length Register
CSIC_DMA_FLIP_SIZE_REG	0x003C	CSIC DMA Flip Size Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_CAP_STA_REG	0x004C	CSIC DMA Capture Status Register
CSIC_DMA_INT_EN_REG	0x0050	CSIC DMA Interrupt Enable Register
CSIC_DMA_INT_STA_REG	0x0054	CSIC DMA Interrupt Status Register
CSIC_DMA_LINE_CNT_REG	0x0058	CSIC DMA LINE Counter Register
CSIC_DMA_FRM_CNT_REG	0x005C	CSIC DMA Frame Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0060	CSIC DMA Frame Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0064	CSIC DMA Accumulated And Internal Clock Counter Register
CSIC_DMA_FIFO_STAT_REG	0x0068	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x006C	CSIC DMA FIFO Threshold Register
CSIC_DMA_PCLK_STAT_REG	0x0070	CSIC DMA PCLK Statistic Register
CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG	0x0080	CSIC DMA BUF Address FIFO0 Entry Register
CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG	0x0084	CSIC DMA BUF Address FIFO1 Entry Register
CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG	0x0088	CSIC DMA BUF Address FIFO2 Entry Register
CSIC_DMA_BUF_TH_REG	0x008C	CSIC DMA BUF Threshold Register
CSIC_DMA_BUF_ADDR_FIFO_CON_REG	0x0090	CSIC DMA BUF Address FIFO Content Register
CSIC_DMA_STORED_FRM_CNT_REG	0x0094	CSIC DMA Stored Frame Counter Register
CSIC_LBC_CONFIG_REG	0x0100	CSIC LBC Configure Register
CSIC_LBC_LINE_TAR_BIT0_REG	0x0104	CSIC LBC Line Target Bit0 Register
CSIC_LBC_LINE_TAR_BIT1_REG	0x0108	CSIC LBC Line Target Bit1 Register
CSIC_LBC_RC_ADV_REG	0x010C	CSIC LBC RC ADV Register
CSIC_LBC_MB_MIN_REG	0x0110	CSIC LBC MB MIN Register
CSIC_FEATURE_REG	0x01F4	CSIC DMA Feature List Register

8.1.5. CCU Register Description

8.1.5.1. 0x0000 CCU Clock Mode Register(Default Value:0x8000_0000)

Offset: 0x0000			**Register Name: CCU_CLK_MODE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CCU_CLK_GATING_DISABLE 0: CCU Clock Gating Registers(0x0004~0x0010) effect 1: CCU Clock Gating Registers(0x0004~0x0010) not effect
30:5	/	/	/
4	R/W	0x0	MISP_CLK_MODE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: ISP core clock uses isp_clk2x when there is only 1 isp core working 1: ISP core clock uses isp_clk1x when there is 2 isp core working
3:2	/	/	/
1	R/W	0x0	MCSI_POST_CLK_MODE 0: Reserved 1: CSI Post works in csi clock
0	R/W	0x0	MCSI_PARSER_CLK_MODE 0: CSI Parser works in isp core clock 1: CSI Parser works in csi clock

8.1.5.2. 0x0004 CCU Parser Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CCU_PARSER_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE 0: Combo0 clock disable 1: Combo0 clock enable
7:2	/	/	/
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

8.1.5.3. 0x0008 CCU ISP Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	MISP1_BRIDGE_CLK_ENABLE 0: ISP1 bridge clock disable 1: ISP1 bridge clock enable
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE 0: ISP0 clock disable 1: ISP0 clock enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.5.4. 0x000C CCU Post0 Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CCU_POST0_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0:VIPP1 clock disable 1: VIPP1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable,when MCSI_POST0_CLK_ENABLE is 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE 0: BK1 clock disable 1: BK1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE 0: BK0 clock disable 1: BK0 clock enable,when MCSI_POST0_CLK_ENABLE is 1

8.1.6. CSIC Top Register Description

8.1.6.1. 0x0000 CSIC TOP Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ISP_BRIDGE_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Enable Async Bridge from parser to isp and isp to post, when isp uses different clock source from csi_top_clk 0: disable 1: enable
2	R/W	0x0	BIST_MODE_EN 0: Closed 1: EN BIST TEST
1	/	/	/
0	R/W	0x0	CSIC_TOP_EN 0: Reset and disable the CSIC module 1: Enable the CSIC module

8.1.6.2. 0x0004 CSIC Pattern Generation Enable Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software writes this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to ”0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

8.1.6.3. 0x0008 CSIC Pattern Control Register(Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	PTN_PORT_SEL Pattern generator output port selection 000:reserved 001:reserved 010:reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			011:reserved 100:reserved 101:reserved 110:COMBO 111:reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8-bit 01:10-bit 10:12-bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000~1011:reserved 1100:BAYER 12 bits for ISPFE 1101:UYVY422 12 bits for ISPFE 1110:UYVY420 12 bits for ISPFE 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

8.1.6.4. 0x0020 CSIC Pattern Generation Length Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

8.1.6.5. 0x0024 CSIC Pattern Generation Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

8.1.6.6. 0x0028 CSIC Pattern ISP Size Register(Default Value:0x0000_0000)

Offset: 0x0028	Register Name: CSIC_PTN_ISP_SIZE_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

8.1.6.7. 0x0030 CSIC ISP0 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	ISP0 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.8. 0x0034 CSIC ISP0 Input1 Select Register(Default Value:0x0000_0001)

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x1	ISP0 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.9. 0x0038 CSIC ISP0 Input2 Select Register(Default Value:0x0000_0002)

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x2	ISP0 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.10. 0x003C CSIC ISP0 Input3 Select Register(Default Value:0x0000_0003)

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	ISP0 Input3 Select 0000: input from Parser0 CH0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.11. 0x0040 CSIC ISP1 Input0 Select Register(Default Value:0x0000_0004)

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x4	ISP1 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.12. 0x0044 CSIC ISP1 Input1 Select Register(Default Value:0x0000_0005)

Offset :0x0044	Register Name: CSIC_ISP1_INPUT1_SEL_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x5	ISP1 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.13. 0x0048 CSIC ISP1 Input2 Select Register(Default Value:0x0000_0006)

Offset: 0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x6	ISP1 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.6.14. 0x004C CSIC ISP1 Input3 Select Register(Default Value:0x0000_0007)

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x7	ISP1 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.15. 0x0050 CSIC ISP2 Input0 Select Register(Default Value:0x0000_0008)

Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x8	ISP2 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.16. 0x0054 CSIC ISP2 Input1 Select Register(Default Value:0x0000_0009)

Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x9	ISP2 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.17. 0x0058 CSIC ISP2 Input2 Select Register(Default Value:0x0000_000A)

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xa	ISP2 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.18. 0x005C CSIC ISP2 Input3 Select Register(Default Value:0x0000_000B)

Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xb	ISP2 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.19. 0x0060 CSIC ISP3 Input0 Select Register(Default Value:0x0000_000C)

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xC	ISP3 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.20. 0x0064 CSIC ISP3 Input1 Select Register(Default Value:0x0000_000D)

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xD	ISP3 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.21. 0x0068 CSIC ISP3 Input2 Select Register(Default Value:0x0000_000e)

Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xE	ISP3 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.22. 0x006C CSIC ISP3 Input3 Select Register(Default Value:0x0000_000F)

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xF	ISP3 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

8.1.6.23. 0x0070 CSIC ISP Bridge Buffer Maxuse Counter Clear Register(Default Value:0x0000_0000)

Offset :0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:6	/	/	/
5	R/W	0x0	ISP1_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
4	R/W	0x0	ISP1_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
3:2	/	/	/
1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear

8.1.6.24. 0x0074 CSIC ISP0 Bridge Buffer Maxuse Counter Register(Default Value:0x0000_0000)

Offset :0x0074			Register Name: CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	ISP0_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG0_BUF_MAXUSE_CNT

8.1.6.25. 0x007C CSIC ISP1 Bridge Buffer Maxuse Counter Register(Default Value:0x0000_0000)

Offset :0x007C			Register Name: CSIC_ISP1_BRG_BUF_MAXUSE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	ISP1_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP1_BRG0_BUF_MAXUSE_CNT

8.1.6.26. 0x0084 CSIC ISP0 Bridge Interrupt Enable Register(Default Value:0x0000_0000)

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:17	/	/	/
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:9	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:1	/	/	/
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

8.1.6.27. 0x0088 CSIC ISP1 Bridge Interrupt Enable Register(Default Value:0x0000_0000)

Offset :0x0088			Register Name: CSIC_ISP1_BRG_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	ISP1_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP1 Bridge0 Slow to Fast Side
23:17	/	/	/
16	R/W	0x0	ISP1_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP1 Bridge0 Fast to Slow Side
15:9	/	/	/
8	R/W	0x0	ISP1_BRG0_BUF_OV_INT_EN ISP1 Bridge0 Buffer overflow interrupt enable
7:1	/	/	/
0	R/W	0x0	ISP1_BRG0_RS_INT_EN ISP1 Bridge0 Read clock too slow interrupt enable

8.1.6.28. 0x008C CSIC ISP0 Bridge Interrupt Pending Register(Default Value:0x0000_0000)

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:17	/	/	/
16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:9	/	/	/
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:1	/	/	/
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.6.29. 0x0090 CSIC ISP1 Bridge Interrupt Pending Register(Default Value:0x0000_0000)

Offset :0x0090			Register Name: CSIC_ISP1_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	ISP1_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP1 Bridge0 Slow to Fast Side
23:17	/	/	/
16	R/W1C	0x0	ISP1_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP1 Bridge0 Fast to Slow Side
15:9	/	/	/
8	R/W1C	0x0	ISP1_BRG0_BUF_OV_INT_PD ISP1 Bridge0 Buffer overflow interrupt pending
7:1	/	/	/
0	R/W1C	0x0	ISP1_BRG0_RS_INT_PD ISP1 Bridge0 Read clock too slow interrupt pending

8.1.6.30. 0x00A0 CSIC DMA0 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA0 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.31. 0x00A4 CSIC DMA1 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.32. 0x00A8 CSIC DMA2 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA2 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.33. 0x00AC CSIC DMA3 Input Select Register(Default Value:0x0000_0000)

Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA3 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.34. 0x00DC CSIC BIST CS Register(Default Value:0x0000_0000)

Offset :0x00DC	Register Name: CSIC_BIST_CS_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	BIST_CS 000: Set when BK0 or ISP0_BRIDGE0 memory bist 001: Set when BK1 or ISP0_BRIDGE1 memory bist 010: Set when BK2 or ISP0_BRIDGE2 memory bist 011: Set when BK3 or ISP0_BRIDGE3 memory bist 100: Set when BK4 or ISP1_BRIDGE0 memory bist Others: Reserved

8.1.6.35. 0x00E0 CSIC BIST Control Register(Default Value:0x0000_0200)

Offset :0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP 0:running 1:STOP
8	R	0x0	BIST_BUSY BIST Busy 0:idle 1:busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG Select
4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address Mode Select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write Data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			others: reserved
0	R/W	0x0	BIST_EN BIST Enable A positive will trigger the BIST to start.

8.1.6.36. 0x00E4 CSIC BIST Start Address Register(Default Value:0x0000_0000)

Offset :0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

8.1.6.37. 0x00E8 CSIC BIST End Address Register(Default Value:0x0000_0000)

Offset :0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

8.1.6.38. 0x00EC CSIC BIST Data Mask Register(Default Value:0x0000_0000)

Offset :0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0:Unmask 1:Mask

8.1.6.39. 0x00F0 CSIC MBUS REQ MAX Register(Default Value:0x000F_0F0F)

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0f	MISP_MEM_REQ_MAX
15:13	/	/	/
12:8	R/W	0x0f	MCSI_MEM_1_REQ_MAX
7:5	/	/	/
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.6.40. 0x0100 CSIC Multi-Frame Mode Register(Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	MULF_STATUS
23:16	/	/	/
15:8	R/W	0x0	MULF_CS
7:1	/	/	/
0	R/W	0x0	MULF_EN

8.1.6.41. 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD
16	R/W1C	0x0	MULF_DONE_PD
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN
0	R/W	0x0	MULF_DONE_EN

8.1.6.42. 0x01F0 CSIC Feature List Register(Default Value:0x2211_4400)

Offset: 0x01F0			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R	0x2	VER_SMALL_PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x2	MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x1	NCSI_NUM Only can be read when version register read enable is on.
19:16	R	0x1	ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x4	DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7. Parser Register Description

8.1.7.1. 0x0000 Parser Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:3	/	/	/
2	R/W	0x0	PRS_CH_MODE 0: Parser output channel 0~3 corresponding from input channel 0~3 1: Parser output channel 0~3 all from input channel 0(MIPI SEHDR)
1	R/W	0x0	PRS_MODE 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

8.1.7.2. 0x0008 Parser MCSIC Interface Configuration Register(Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.3. 0x000C Parser Capture Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	RC/W	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
13:12	/	/	/
21:18	R/W	0x0	CH2_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	RC/W	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
15:14	/	/	/
13:10	R/W	0x0	CH1_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames ……

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			15: 1/16 fps, only receives the first frame every 16 frames
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	RC/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

8.1.7.4. 0x0024 Parser Channel_0 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0024			Register Name: PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.5. 0x0028 Parser Channel_0 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.6. 0x002C Parser Channel_0 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.7.7. 0x003C Parser Channel_0 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.8. 0x0034 Parser Channel_0 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0034			Register Name: PRS_CH0_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.9. 0x0038 Parser Channel_0 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0038			Register Name: PRS_CH0_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.10. 0x003C Parser Channel_0 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.11. 0x0040 Parser Channel_0 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.12. 0x0044 Parser Channel_0 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.13. 0x0048 Parser Channel_0 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0048	Register Name: PRS_CH0_LINE_TIME_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.14. 0x0124 Parser Channel_1 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0124			Register Name: PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.15. 0x0128 Parser Channel_1 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0128			Register Name: PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.16. 0x012C Parser Channel_1 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x012C			Register Name: PRS_CH1_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.17. 0x0130 Parser Channel_1 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0130			Register Name: PRS_CH1_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.18. 0x0134 Parser Channel_1 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0134			Register Name: PRS_CH1_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.19. 0x0138 Parser Channel_1 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0138			Register Name: PRS_CH1_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.20. 0x013C Parser Channel_1 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x013C			Register Name: PRS_CH1_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.21. 0x0140 Parser Channel_1 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.22. 0x0144 Parser Channel_1 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag is set to 1. Write 1 to clear.

8.1.7.23. 0x0148 Parser Channel_1 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0148			Register Name: PRS_CH1_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.24. 0x0224 Parser Channel_2 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0224			Register Name: PRS_CH2_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.25. 0x0228 Parser Channel_2 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.26. 0x022C Parser Channel_2 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x022C			Register Name: PRS_CH2_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.7.27. 0x0230 Parser Channel_2 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0230			Register Name: PRS_CH2_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.28. 0x0234 Parser Channel_2 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0234			Register Name: PRS_CH2_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.29. 0x0238 Parser Channel_2 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PRS_CH2_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.30. 0x023C Parser Channel_2 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x023C			Register Name: PRS_CH2_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.31. 0x0240 Parser Channel_2 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0240			Register Name: PRS_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.32. 0x0244 Parser Channel_2 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.33. 0x0248 Parser Channel_2 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0248			Register Name: PRS_CH2_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.34. 0x0324 Parser Channel_3 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0324			Register Name: PRS_CH3_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0011: YUV422 0100: YUV420 Others: reserved

8.1.7.35. 0x0328 Parser Channel_3 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0328			Register Name: PRS_CH3_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.36. 0x032C Parser Channel_3 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x032C			Register Name: PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.37. 0x0330 Parser Channel_3 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0330			Register Name: PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.38. Parser Channel_3 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.39. 0x0338 Parser Channel_3 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0338			Register Name: PRS_CH3_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.40. 0x033C Parser Channel_3 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x033C			Register Name: PRS_CH3_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.41. 0x0340 Parser Channel_3 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0340			Register Name: PRS_CH3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.7.42. 0x0344 Parser Channel_3 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0344			Register Name: PRS_CH3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.43. 0x0348 Parser Channel_3 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0348			Register Name: PRS_CH3_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.44. 0x0520 Parser CSIC SYNC EN Register(Default Value:0x0000_0000)

Offset :0x0520			Register Name: CSIC_SYNC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	Input vsync singal source select 0000: Vsync signals all from 1 parser 0001: Vsync signals from 2 parser 0010: Vsync signals from 4 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	Generate sync singal benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1 to use input
7:4	R/W	0x0	Parser input vsync singal enable in sync mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1 to enable input
3	/	/	/
2	R/W	0x0	Parser sent sync singal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	Parser sync singal source select 0: From outside 1: Generate by self
0	R/W	0x0	Enable Parser sent sync singal 0: Disable 1: Enable

8.1.7.45. 0x0524 Parser CSIC SYNC CFG Register(Default Value:0x0000_0000)

Offset :0x0524			Register Name: CSIC_PULSE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PUL_WID Sync signal pulse width $N*T_{24M}$, $N*T_{24M} \geq 4*Tpclk$
15:0	R/W	0x0	SYNC_DISTANCE The interval of two sync signal

8.1.7.46. 0x0528 Parser CSIC VS WAIT N Register(Default Value:0x0000_0000)

Offset :0x0528			Register Name: CSIC_SYNC_WAIT_N_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come, the max wait time.

8.1.7.47. 0x052C Parser CSIC VS WAIT M Register(Default Value:0x0000_0000)

Offset :0x052C			Register Name: CSIC_SYNC_WAIT_M_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode,vsync comes at the different time,these bits indicate the max wait time.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.8. CSIC DMA Register Description

8.1.8.1. 0x0000 CSIC DMA Enable Register(Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE Buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:8	/	/	/
7	R/W	0x0	BUF_ADDR_MODE 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode(only DMA0/1 support)
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FRAME_CNT_EN When BK_TOP_EN is enabled, this bit is set to 1, it indicates that the frame counter starts to add. 0: Disable 1: Enable
4	R/W	0x0	DMA_EN When BK_TOP_EN is enabled, this bit is set to 1, it indicates that module works in DMA mode. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN 0: Disable 1: Enable

8.1.8.2. 0x0004 CSIC DMA Configuration Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV 10-bit input cut to 8-bit 0: disable 1: enable
20	R/W	0x0	YUV 10-bit store configure 0: YUV 10-bit stored in low 10-bit of a 16-bit word 1: YUV 10-bit stored in high 10-bit of a 16-bit word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set to RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set to YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set to YUV420 0000: LBC mode output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection 00: capturing with field 0 01: capturing with field 1 10: capturing with either field

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 00: 256 bytes (if hflip is enabled, and always selected 256 bytes) 01: 512 bytes 10: 1k bytes 11: 2k bytes

8.1.8.3. 0x0010 CSIC DMA Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSIC_DMA_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled, these bits indicate input width in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC is disabled, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC is enabled, these bits indicate input width in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.8.4. 0x0014 CSIC DMA Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x0014			Register Name: CSIC_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			these bits indicate Input height in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC is disabled, these bits indicate Valid line number of a frame in DMA mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC is enabled, these bits indicate Input height in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.8.5. 0x0020 CSIC DMA FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled, these bits indicate output address of overhead data in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC_EN is disabled, these bits indicate FIFO 0 output buffer-A address in DMA mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, LBC_EN is enabled, these bits indicate the output buffer address in LBC mode.

8.1.8.6. 0x0024 CSIC DMA FIFO 0 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_DMA_F0_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.7. 0x0028 CSIC DMA FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_DMA_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F1_BUFA When BK_TOP_EN is enabled, FBC_EN is enabled, DMA_EN is disabled, these bits indicate output address of compressed data in FBC mode. When BK_TOP_EN is enabled, FBC_EN is disabled, DMA_EN is enabled, these bits indicate FIFO 1 output buffer-A address in DMA mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.8.8. 0x002C CSIC DMA FIFO 1 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x002C			Register Name: CSIC_DMA_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.9. 0x0030 CSIC DMA FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_DMA_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address.

8.1.8.10. 0x0034 CSIC DMA FIFO 2 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_DMA_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.11. 0x0038 CSIC DMA Buffer Length Register(Default Value:0x0280_0500)

Offset: 0x0038			Register Name: CSIC_DMA_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0.
15:14	/	/	/
13:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.8.12. 0x003C CSIC DMA Flip Size Register(Default Value:0x02D0_0500)

Offset: 0x003C			Register Name: CSIC_DMA_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE is set 0.
15:14	/	/	/
13:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE is set 0.

8.1.8.13. 0x0040 CSIC DMA Video Input Timeout Threshold0 Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , the time unit is a 12M clock period.

8.1.8.14. 0x0044 CSIC DMA Video Input Timeout Threshold1 Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, the time unit is a 12M clock period.

8.1.8.15. 0x0048 CSIC DMA Video Input Timeout Counter Value Register(Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

8.1.8.16. 0x004C CSIC DMA Capture Status Register(Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_DMA_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

8.1.8.17. 0x0050 CSIC DMA Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0050			**Register Name: CSIC_DMA_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	FRM_LOST_INT_EN Set an INT when frame starts with empty Buffer Address FIFO, only use in BUF Address FIFO MODE.
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE.
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE.
12	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
11	R/W	0x0	CLR_FRAME_CNT_INT_EN Set a INT when Clear Frame cnt.
10	R/W	0x0	SENT_SYNC_INT_EN Set a INT when sent a SYNC signal.
9	R/W	0x0	FBC_DATA_WRDDR_FULL_EN Error flag of FBC_DATA_WRDDR_FULL.
8	R/W	0x0	FBC_OVHD_WRDDR_FULL_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, changing the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 became overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 became overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 became overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

8.1.8.18. 0x0054 CSIC DMA Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0054			**Register Name: CSIC_DMA_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT when frame starts with empty Buffer Address FIFO, only use in

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			BUF Address FIFO MODE
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT pending when no video input exceeds the setting threshold time
11	R/W1C	0x0	CLR_FRAME_CNT_INT Set a INT when clear Frame cnt.
10	R/W1C	0x0	SENT_SYNC_INT Set a INT when sent a SYNC signal.
9	R/W1C	0x0	FBC_DATA_WRDDR_FULL_PD Error flag of FBC_DATA_WRDDR_FULL.
8	R/W1C	0x0	FBC_OVHD_WRDDR_FULL_PD Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

8.1.8.19. 0x0058 CSIC DMA Line Counter Register(Default Value:0x0000_0000)

Offset: 0x0058			**Register Name: CSIC_DMA_LINE_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value, the LC_PD will be set.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8.1.8.20. 0x005C CSIC DMA Frame Counter Register(Default Value:0x0001_0000)

Offset: 0x005C			Register Name: CSIC_DMA_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FRM_CNT_CLR When the bit set to 1, Frame cnt is cleared to 0
30:16	R/W	0x1	PCLK_DMA_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15:0	R	0x0	FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full, it is cleared to 0. When parser sent a sync signal, it is cleared to 0.

8.1.8.21. 0x0060 CSIC DMA Frame Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0060			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12 MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

8.1.8.22. 0x0064 CSIC DMA Accumulated and Internal Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0064			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame is done, the software checks this accumulated value and clears it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			registers.

8.1.8.23. 0x0068 CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)

Offset: 0x0068			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	Line Index Indicates the line index in current vsync.
15:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

8.1.8.24. 0x006C CSIC DMA FIFO Threshold Register(Default Value:0x0000_0400)

Offset: 0x006C			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x400	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change.

8.1.8.25. 0x0070 CSIC DMA PCLK Statistic Register(Default Value:0x0000_7FFF)

Offset: 0x0070			Register Name: CSIC_DMA_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

8.1.8.26. 0x0080 CSIC DMA BUF Address FIFO0 Entry Register(Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.27. 0x0084 CSIC DMA BUF Address FIFO1 Entry Register(Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.28. 0x0088 CSIC DMA BUF Address FIFO2 Entry Register(Default Value:0x0000_0000)

Offset: 0x0088			Register Name: CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.29. 0x008C CSIC DMA BUF Threshold Register(Default Value:0x0020_0000)

Offset: 0x008C			Register Name: CSIC_DMA_BUF_TH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode.
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO less than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode.

8.1.8.30. 0x0090 CSIC DMA BUF Address FIFO Content Register(Default Value:0x0000_0000)

Offset: 0x0090			Register Name: CSIC_DMA_BUF_ADDR_FIFO_CON_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Buffer Addr FIFO Mode.
15:14	/	/	/
13:8	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode.
7:6	/	/	/
5:0	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode.

8.1.8.31. 0x0094 CSIC DMA Stored Frame Counter Register(Default Value:0x0000_0000)

Offset: 0x0094			Register Name: CSIC_DMA_STORED_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	RO	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode.

8.1.8.32. 0x0100 CSIC LBC Configure Register(Default Value:0x8F30_0008)

Offset: 0x0100			Register Name: CSIC_LBC_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

8.1.8.33. 0x0104 CSIC LBC Line Target Bit0 Register(Default Value:0x0000_2400)

Offset: 0x0104			Register Name: CSIC_LBC_LINE_TAR_BIT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

8.1.8.34. 0x0108 CSIC LBC Line Target Bit1 Register(Default Value:0x0000_3600)

Offset: 0x0108			Register Name: CSIC_LBC_LINE_TAR_BIT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

8.1.8.35. 0x010C CSIC LBC RC ADV Register(Default Value:0x1010_1010)

Offset: 0x010C			Register Name: CSIC_LBC_RC_ADV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

8.1.8.36. 0x0110 CSIC LBC MB MIN Register(Default Value:0x006E_0037)

Offset: 0x0110			Register Name: CSIC_LBC_MB_MIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

8.1.8.37. 0x01F4 CSIC DMA Feature List Register(Default Value:0x0000_0000)

Offset: 0x01F4			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R	0x0	DMA0_EMBEDDED_LBC 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC 0: No Embedded DMA 1: Embedded FBC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 9 Audio 598
9.1. I2S/PCM 598
9.1.1. Overview 598
9.1.2. Block Diagram 598
9.1.3. Operations and Functional Descriptions 599
9.1.4. Programming Guidelines 604
9.1.5. Register List 606
9.1.6. Register Description 607
9.2. DMIC 636
9.2.1. Overview 636
9.2.2. Block Diagram 636
9.2.3. Operations and Functional Descriptions 636
9.2.4. Register List 638
9.2.5. Register Description 639
9.3. OWA 650
9.3.1. Overview 650
9.3.2. Block Diagram 650
9.3.3. Operations and Functional Descriptions 651
9.3.4. Register List 655
9.3.5. Register Description 655
9.4. Audio Codec 663
9.4.1. Overview 663
9.4.2. Block Diagram 663
9.4.3. Operations and Functional Descriptions 664
9.4.4. Programming Guidelines 674
9.4.5. Register List 674
9.4.6. Register Description 677

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 9- 1. I2S/PCM Interface System Block Diagram 599
Figure 9- 2. I2S Standard Mode Timing 600
Figure 9- 3. Left-Justified Mode Timing 601
Figure 9- 4. Right-Justified Mode Timing 601
Figure 9- 5. PCM Long Frame Mode Timing 601
Figure 9- 6. PCM Short Frame Mode Timing 602
Figure 9- 7. 16 Channels Mapping Configuration 602
Figure 9- 8. I2S/PCM Operation Flow 603
Figure 9- 9. DMIC Block Diagram 636
Figure 9- 10. DMIC Operation Mode 637
Figure 9- 11. OWA Block Diagram 650
Figure 9- 12. OWA Biphase-Mark Code 652
Figure 9- 13. OWA Sub-Frame Format 652
Figure 9- 14. OWA Frame/Block Format 653
Figure 9- 15. OWA Operation Flow 654
Figure 9- 16. Audio Codec Block Diagram 664
Figure 9- 17. Audio Codec Clock Diagram 666
Figure 9- 18. Audio Codec Digital Part Reset System 667
Figure 9- 19. Audio Codec Analog Part Reset System 667
Figure 9- 20. Audio Codec Data Path Diagram 668
Figure 9- 21. Headphone Output Application 669
Figure 9- 22. External Accessory Detection 670
Figure 9- 23. Audio Codec Interrupt System 670
Figure 9- 24. DAP Data Flow 671
Figure 9- 25. HPF Function 671
Figure 9- 26. DRC Block Diagram 671
Figure 9- 27. DRC Static Curve Parameters 672
Figure 9- 28. Energy Filter Structure 672
Figure 9- 29. Gain Smooth Filter 673

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 9- 1. I2S/PCM External Signals....599
Table 9- 2. I2S/PCM Clock Sources....600
Table 9- 3. DIN Slot ID and Encoder....602
Table 9- 4. DMIC External Signals....636
Table 9- 5. DMIC Clock Sources....637
Table 9- 6. OWA External Signals....651
Table 9- 7. OWA Clock Sources....651
Table 9- 8. Biphase-Mark Encoder....652
Table 9- 9. Preamble Codes....653

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 9 Audio

9.1. I2S/PCM

9.1.1. Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format and TDM mode format.

The I2S/PCM controller includes the following features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master/slave mode
- Adjustable interface voltage
- Clock up to 24.576 MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Up to 16 channel(fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
- Sample rate from 8 kHz to 384 kHz(CHAN = 2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports loop back mode for test

9.1.2. Block Diagram

The block diagram of I2S/PCM interface is shown as follows.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

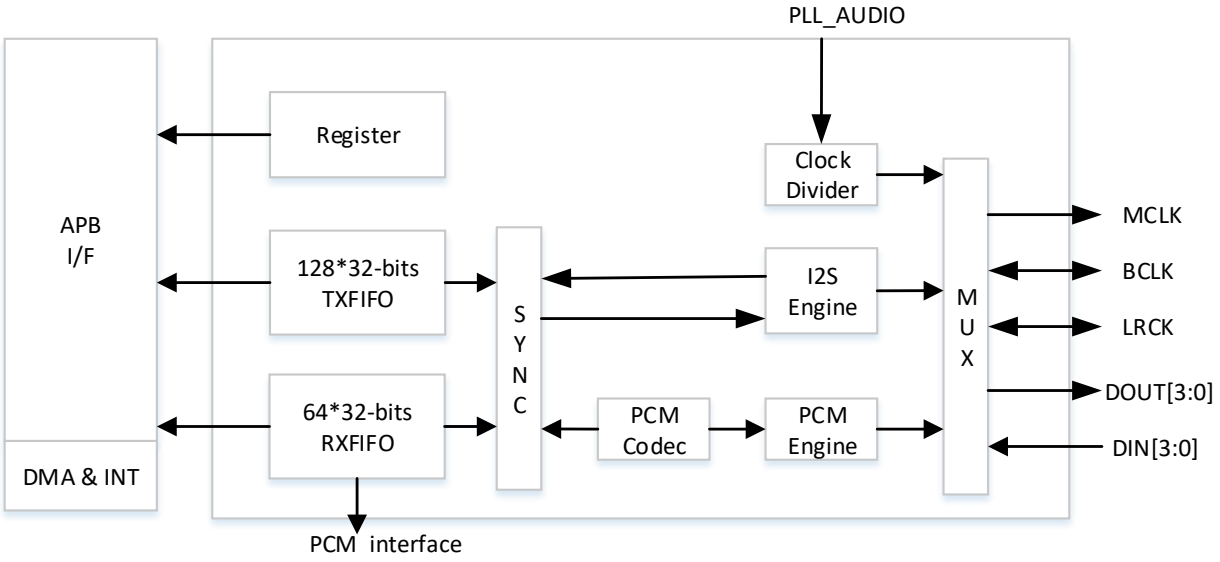


Figure 9- 1. I2S/PCM Interface System Block Diagram

9.1.3. Operations and Functional Descriptions

9.1.3.1. External Signals

Table 9-1 describes the external signals of I2S/PCM interface. LRCK and BCLK are bidirectional I/O, when I2S/PCM interface is configured as Master device, LRCK and BCLK is output pin; when I2S/PCM interface is configured as slave device, LRCK and BCLK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input pin. For information about General Purpose I/O port, see Port Controller.

Table 9- 1. I2S/PCM External Signals

Signal	Description	Type
I2S0_MCLK	I2S0 Master Clock	O
I2S0_LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0_BCLK	I2S0/PCM0 Sample Rate Clock	I/O
I2S0_DOUT[1:0]	I2S0/PCM0 Serial Data Output Channel [1:0]	O
I2S0_DIN[1:0]	I2S0/PCM0 Serial Data Input Channel [1:0]	I
I2S1_MCLK	I2S1 Master Clock	O
I2S1_LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1_BCLK	I2S1/PCM1 Sample Rate Clock	I/O
I2S1_DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1_DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S2_MCLK	I2S2 Master Clock	O
I2S2_LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2_BCLK	I2S2/PCM2 Sample Rate Clock	I/O
I2S2_DOUT[1:0]	I2S2/PCM2 Serial Data Output Channel [1:0]	O
I2S2_DIN[1:0]	I2S2/PCM2 Serial Data Input Channel [1:0]	I
I2S3_MCLK	I2S3 Master Clock	O

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

I2S3_LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3_BCLK	I2S3/PCM3 Sample Rate Clock	I/O
I2S3_DOUT[3:0]	I2S3/PCM3 Serial Data Output Channel [3:0]	O
I2S3_DIN[3:0]	I2S3/PCM3 Serial Data Input Channel [3:0]	I

9.1.3.2. Clock Sources

Table 9-2 describes the clock sources for I2S/PCM. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 9- 2. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO(4X)	The 98.304 MHz frequency generated by PLL_AUDIO(4X) to produce 48 kHz sample frequency.
PLL_COM_AUDIO	The 90.3168 MHz frequency generated by PLL_COM_AUDIO is divided by 4(=22.5792 MHz) and then passed to the module to produce 44.1 kHz sample frequency.

9.1.3.3. Timing Diagram

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode and TDM mode. Software can select any modes by setting the **I2S/PCM Control Register**. Figure 9-2 to Figure 9-6 describe the waveforms for SYNC, BCLK and DOUT, DIN.

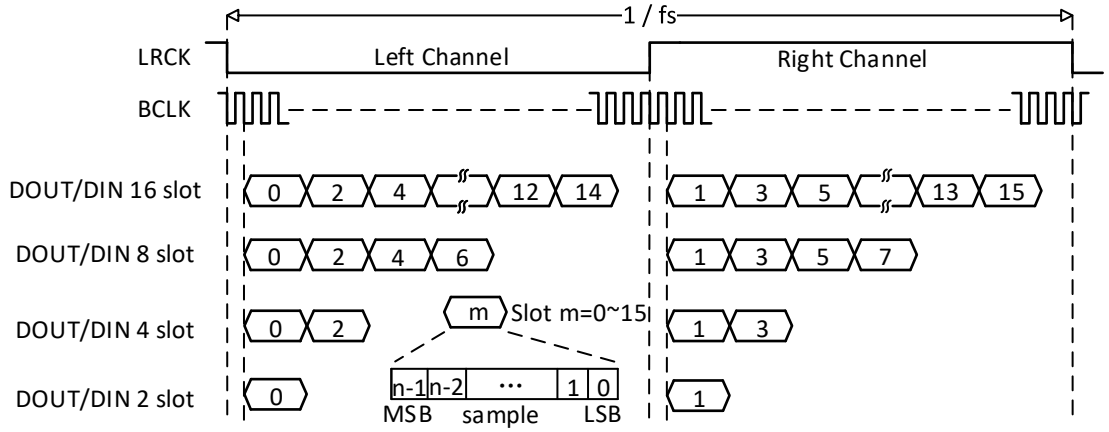


Figure 9- 2. I2S Standard Mode Timing

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

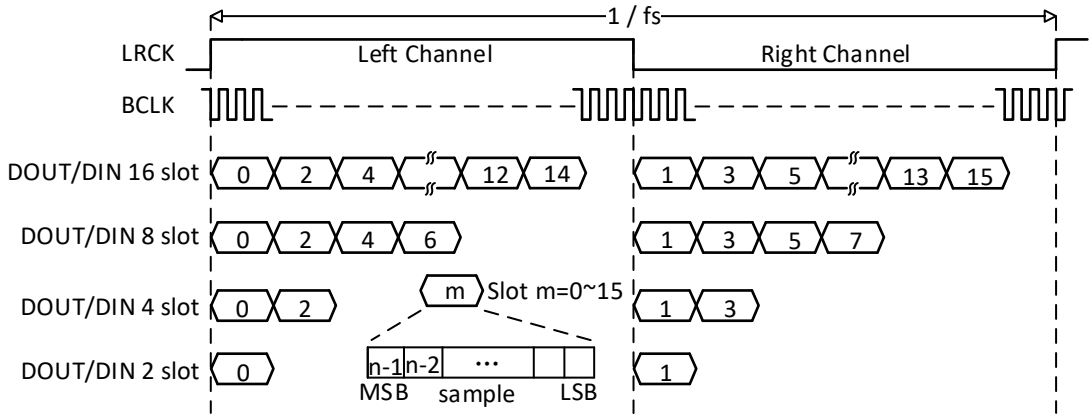


Figure 9- 3. Left-Justified Mode Timing

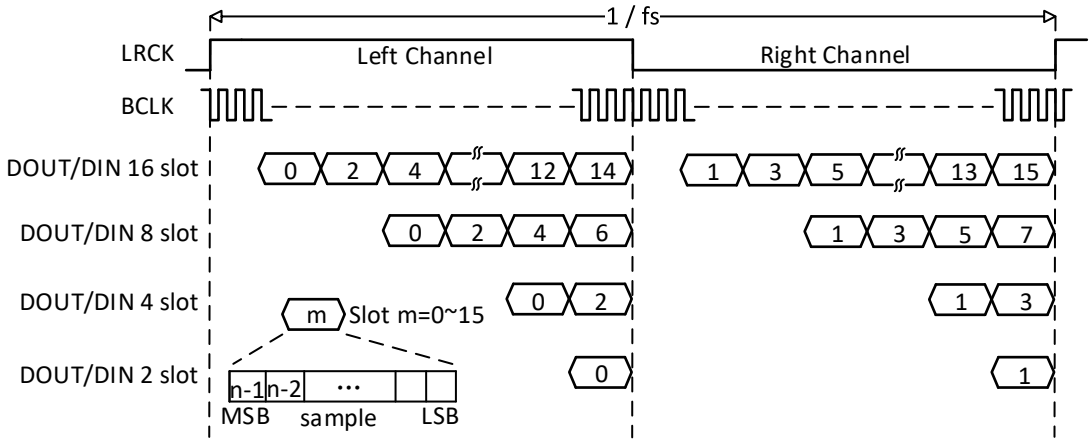


Figure 9- 4. Right-Justified Mode Timing

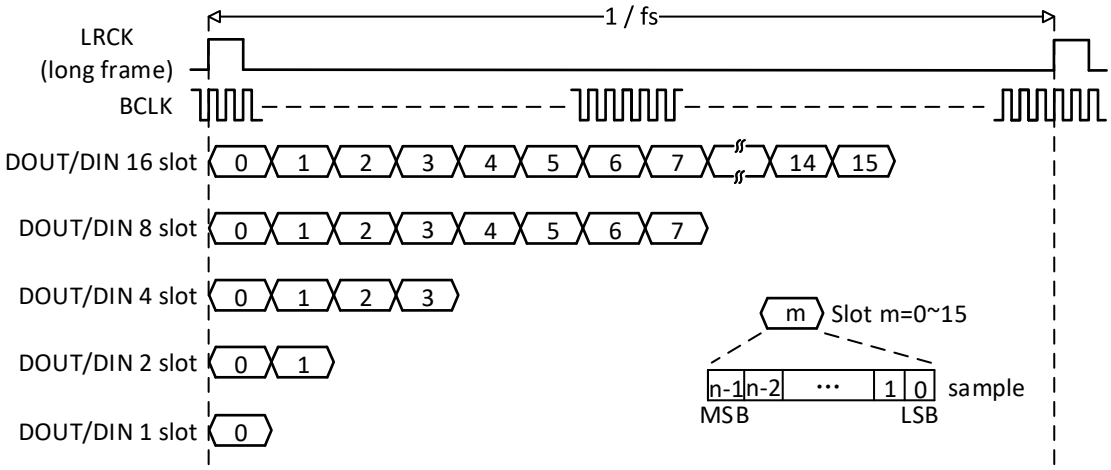


Figure 9- 5. PCM Long Frame Mode Timing

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

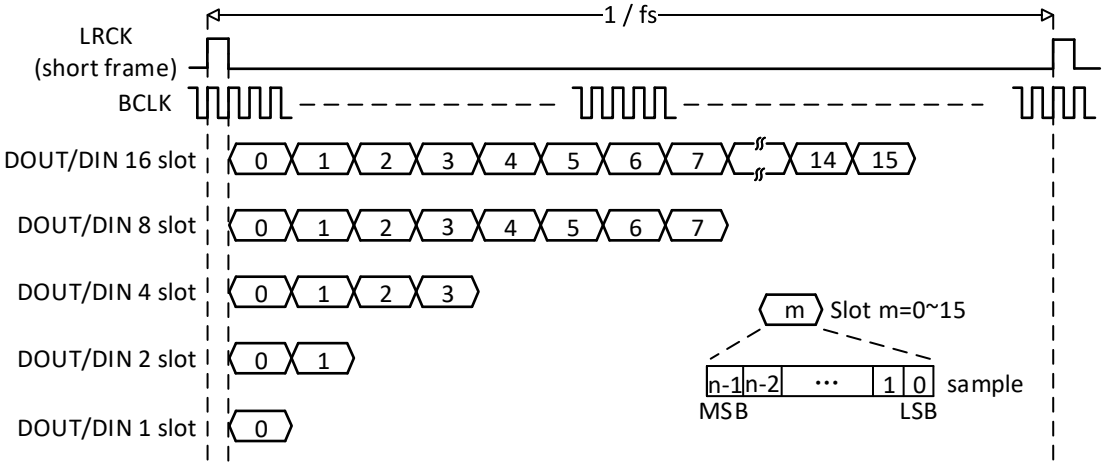


Figure 9- 6. PCM Short Frame Mode Timing

9.1.3.4. DIN Slot Mapping

The 4-wire DIN has 64 slots, each wire DIN has 16 slots, but RX is only 16 channels valid, the relationship between slot id and encoder is as follows.

Table 9- 3. DIN Slot ID and Encoder

DIN0 Slot ID	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DIN1 Slot ID	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DIN2 Slot ID	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DIN3 Slot ID	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

There are 16 channels mapping configuration, each wire is selected four slots into RX.

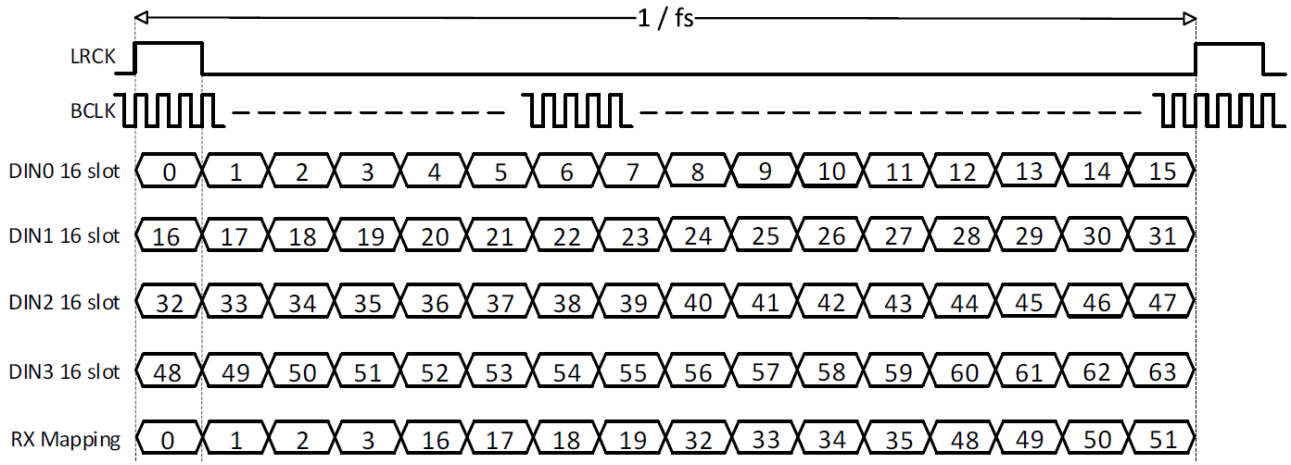


Figure 9- 7. 16 Channels Mapping Configuration

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.3.5. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

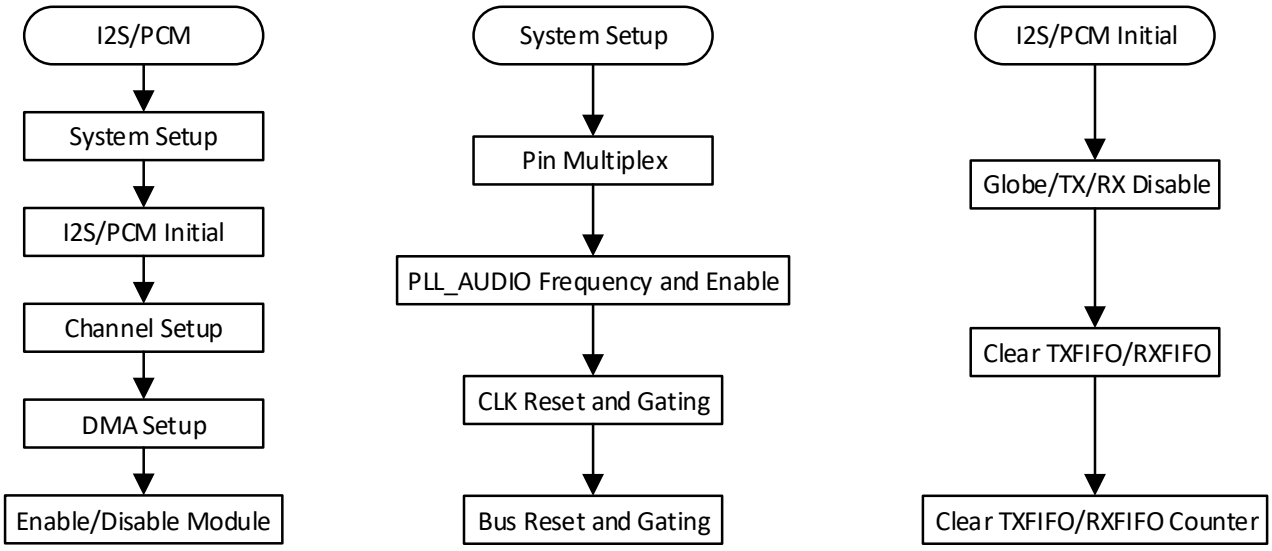


Figure 9- 8. I2S/PCM Operation Flow

(1). System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. At first you must disable the PLL_AUDIO through the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating through the **I2S/PCM_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset and open the I2S/PCM bus gating in the **I2S/PCM_BGR_REG**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]), **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel Setup and DMA Setup

First, you can setup the master I2S/PCM and the slave I2S/PCM. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and the trigger level and so on. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

found in the **DMA**. In this module, you just enable the DRQ.

(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing **the I2S/PCM_CTL**[2:1]. After that, you must enable I2S/PCM by writing 1 to the **Globe Enable** bit in the **I2S/PCM_CTL**. Write 0 to the **Globe Enable** bit to disable I2S/PCM.

9.1.4. Programming Guidelines

The following example assumes that the audio channels are stereo channels in I2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits. The recording and playback processes are as follows.

----------GPIO configuration----------

Step1: Ensure that I2S/PCM0 GPIO has power supply.

Step2: Configure GPIOB4/GPIOB5/GPIOB6/GPIOB7/GPIOB8 as Function3.

----------Clock configuration----------

Step1: Configure PLL_AUDIO as 24.576 MHz, that is, set **PLL_AUDIO Control Register** to 0xA90B1701, set **PLL_AUDIO Pattern0 Register** to 0xC00126E9 (If PLL_AUDIO is set as 22.5792 MHz, that is, set **PLL_AUDIO Control Register** to 0xA90B1501, set **PLL_AUDIO Pattern0 Register** to 0xC001288D).

Step2: Check whether **PLL_AUDIO Control Register**[PLL_AUDIO_LOCK] is 0x1. If is 1, set **I2S/PCM0 Clock Register** to 0x80000000.

Step3: Write 0x1 to the bit16 of **I2S/PCM0 Bus Gating Reset Register** to dessert I2S/PCM0 reset.

Step4: Write 0x1 to the bit0 of **I2S/PCM0 Bus Gating Reset Register** to open I2S/PCM0 gating.

NOTE

The Step3 and Step4 is set separately.

----------Initialization I2S/PCM----------

Step1: Set the bit[2:0] of **I2S/PCM Control Register** to 0 to close TXEN,RXEN and GEN.

Step2: Set the bit[25:24] of **I2S/PCM FIFO Control Register** to 0x3 to clear TXFIFO and RXFIFO.

Step3: Set **I2S/PCM TX Counter Register** to 0 to clear TX counter, set **I2S/PCM RX Counter Register** to 0 to clear RX counter.

----------Format configuration----------

Step1: Master/slave configuration. In master mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0x3; in slave mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0.

Step2: Configure the[5:4] of **I2S/PCM Control Register** to 0x1 to set standard I2S mode, configure the bit[21:20] of **I2S/PCM TX0 Channel Select Register** to 0x1, configure the bit[21:20] of **I2S/PCM RX Channel Select Register** to 0x1.

Step3: Configure the bit[6:4] of **I2S/PCM Format Register0** to 0x3 to set sample resolution, configure the bit[2:0] of **I2S/PCM Format Register0** to 0x3 to set channel width.

Step4: Configure the bit[7:4] of **I2S/PCM Channel Configuration Register** to 0x1 to set RX channel number, configure

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

the bit[3:0] of **I2S/PCM Channel Configuration Register** to 0x1 to set TX channel number. Configure the bit[19:16] of **I2S/PCM TX0 Channel Select Register** to 0x1, configure the bit[1:0] of **I2S/PCM TX0 Channel Select Register** to 0x3. Configure the bit[19:16] of **I2S/PCM RX Channel Select Register** to 0x1.

Step5: Configure the bit[7:0] of **I2S/PCM TX0 Channel Mapping Register 1** to 0x10, configure the bit[5:0] of **I2S/PCM RX Channel Mapping Register 3** to 0x0, configure the bit[13:8] of **I2S/PCM RX Channel Mapping Register 3** to 0x1.

----------Clock divider configuration----------

Step1: Set MCLK divider. Configure the bit[3:0] of **I2S/PCM Clock Divide Register** to 0x1, that is, MCLK=24.576MHz. Configure the bit8 of **I2S/PCM Clock Divide Register** to 0x1 to enable MCLK.

Step2: Set BCLK divider. Configure the bit[7:4] of **I2S/PCM Clock Divide Register** to 0xF, that is, BCLK=Sample ratio*Slot_Width*Slot_Num=48K*16*2=1.536MHz.

Step3: Set LRCK divider. Configure the bit[17:8] of **I2S/PCM Format Register** to 0xF, that is, N-1=BCLK/Sample ratio/ Slot_Num =16,N=15.

----------DMA configuration----------

Step1: Set data width of both DMA_SRC and DMA_DEST to 16-bit.

Step2: Set DMA BLOCK SIZE,DMA_SRC BLOCK SIZE and DMA_DEST BLOCK SIZE to 8.

Step3: TX DMA configuration. Set DMA_SRC_DRQ_TYPE to DRAM, set DMA_SRC_ADDR_MODE to Linear Mode, set DMA_DEST_DRQ_TYPE to I2S/PCM0-TX, set DMA_DEST_ADDR_MODE to IO Mode, set DMA_SRC_ADDR to DRAM address of storing data, set DMA_DEST_ADDR to **I2S/PCM TXFIFO**(address: 0x05090020).

Step4: RX DMA configuration. Set DMA_SRC_DRQ_TYPE to I2S/PCM0-RX, set DMA_SRC_ADDR_MODE to IO Mode, set DMA_DEST_DRQ_TYPE to DRAM, set DMA_DEST_ADDR_MODE to Linear Mode, set DMA_SRC_ADDR to **I2S/PCM RXFIFO**(address: 0x05090010), set DMA_DEST_ADDR to DRAM address of storing data.

For more details about DMA, please see the description of DMA in section 3.9.

NOTE

If data is stored in SRAM, then DRAM is modified to SRAM.

----------Recording/playback/pause----------

Step1: Enable globe, set the bit0 of **I2S/PCM Control Register** to 0x1. Enable DOUT0_EN, set the bit8 of **I2S/PCM Control Register** to 0x1.

Step2: Recording start: set the bit1 of **I2S/PCM Control Register** to 0x1, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step3: Playback start: set the bit2 of **I2S/PCM Control Register** to 0x1, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step4: Recording pause: set the bit1 of **I2S/PCM Control Register** to 0, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0.

Step5: Playback pause: set the bit2 of **I2S/PCM Control Register** to 0, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.5. Register List

Module Name	Base Address
I2S/PCM0	0x05090000
I2S/PCM1	0x05091000
I2S/PCM2	0x05092000
I2S/PCM3	0x05093000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TX0CHCFG	0x0034	I2S/PCM TX0 Channel Configuration Register
I2S/PCM_TX1CHCFG	0x0038	I2S/PCM TX1 Channel Configuration Register
I2S/PCM_TX2CHCFG	0x003C	I2S/PCM TX2 Channel Configuration Register
I2S/PCM_TX3CHCFG	0x0040	I2S/PCM TX3 Channel Configuration Register
I2S/PCM_TX0CHMAP0	0x0044	I2S/PCM TX0 Channel Mapping Register0
I2S/PCM_TX0CHMAP1	0x0048	I2S/PCM TX0 Channel Mapping Register1
I2S/PCM_TX1CHMAP0	0x004C	I2S/PCM TX1 Channel Mapping Register0
I2S/PCM_TX1CHMAP1	0x0050	I2S/PCM TX1 Channel Mapping Register1
I2S/PCM_TX2CHMAP0	0x0054	I2S/PCM TX2 Channel Mapping Register0
I2S/PCM_TX2CHMAP1	0x0058	I2S/PCM TX2 Channel Mapping Register1
I2S/PCM_TX3CHMAP0	0x005C	I2S/PCM TX3 Channel Mapping Register0
I2S/PCM_TX3CHMAP1	0x0060	I2S/PCM TX3 Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1
I2S/PCM_RXCHMAP2	0x0070	I2S/PCM RX Channel Mapping Register2
I2S/PCM_RXCHMAP3	0x0074	I2S/PCM RX Channel Mapping Register3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.6. Register Description

9.1.6.1. 0x0000 I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	RX_SYNC_EN Audio/I2S/DMIC RX (RXEN) Synchronize Enable 0: Disable 1: Enable
20	R/W	0x0	RX_EN_MUX Audio RX (RXEN) Enable MUX 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN 0: Disable, Hi-Z State 1: Enable
9	R/W	0x0	DOUT1_EN 0: Disable, Hi-Z State 1: Enable
8	R/W	0x0	DOUT0_EN 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal Transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1' , the bit indicates that the DOUT connects to the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable 0: Disable 1: Enable

9.1.6.2. 0x0004 I2S/PCM Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0004			**Register Name: I2S/PCM_FMT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH LRCK Width(only apply in PCM mode) 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY In I2S/Left-Justified/Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high In PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follows. **PCM mode**: Number of BCLKs within (Left + Right) channel width. **I2S/Left-Justified/Right-Justified mode**: Number of BCLKs within each

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			individual channel width (Left or Right) . For example: N = 7: 8 BCLKs width … N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, DOUT drives data at negative edge 1: Invert mode, DOUT drives data at positive edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT drives data and DIN sample data at the different BCLK edge 1: DOUT drives data and DIN sample data at the same BCLK edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN sample data at positive edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN sample data at positive edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

9.1.6.3. 0x0008 I2S/PCM Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

9.1.6.4. 0x000C I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			**Register Name: I2S/PCM_ISTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: TXFIFO underrun pending interrupt Write ‘1’ to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No pending interrupt 1: TXFIFO overrun pending interrupt Write ‘1’ to clear this interrupt.
4	R	0x1	TXE_INT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TXFIFO Empty Pending Interrupt 0: No pending IRQ 1: TXFIFO empty pending interrupt when data in TXFIFO are less than TX trigger level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: RXFIFO underrun pending interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Write '1' to clear this interrupt.
0	R/W	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ when data in RXFIFO are more than RX trigger level

9.1.6.5. 0x0010 I2S/PCM RXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.1.6.6. 0x0014 I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/WAC	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
24	R/WAC	0x0	FRX

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to flush RXFIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12’h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12’h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding ‘0’ at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by ‘0’ 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12’h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16’h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

9.1.6.7. 0x0018 I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			**Register Name: I2S/PCM_FSTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
27:24	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO available sample word counter

9.1.6.8. 0x001C I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When setting to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When setting to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

9.1.6.9. 0x0020 I2S/PCM TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: I2S/PCM_TXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written to this register one by one. The left channel sample data is first and then the right channel sample.

9.1.6.10. 0x0024 I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: I2S/PCM_CLKD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **Note: Whether in slave or master mode, when this bit is set to '1', MCLK should be output.**
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

9.1.6.11. 0x0028 I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.12. 0x002C I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.13. 0x0030 I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to Hi-Z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 in non-transferring slot 1: Turn to Hi-Z State (TDM) in non-transferring slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots

9.1.6.14. 0x0034 I2S/PCM TX0 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TX0CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 Offset Tune(TX0 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.15. 0x0038 I2S/PCM TX1 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: I2S/PCM_TX1CHSEL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX1_OFFSET TX1 Offset Tune(TX1 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX1_CHSEL TX1 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX1_CHEN TX1 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.16. 0x003C I2S/PCM TX2 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x003C			**Register Name: I2S/PCM_TX2CHSEL**
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:22	/	/	/
21:20	R/W	0x0	TX2_OFFSET TX2 Offset Tune(TX2 data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX2_CHSEL TX2 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX2_CHEN TX2 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.17. 0x0040 I2S/PCM TX3 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: I2S/PCM_TX3CHSEL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX3_OFFSET TX3 Offset Tune(TX3 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX3_CHSEL TX3 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX3_CHEN TX3 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.1.6.18. 0x0044 I2S/PCM TX0 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX0_CH10_MAP

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TX0 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.19. 0x0048 I2S/PCM TX0 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1000: 9th Sample ... 1111: 16th Sample

9.1.6.20. 0x004C I2S/PCM TX1 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: I2S/PCM_TX1CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX1_CH15_MAP TX1 Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX1_CH14_MAP TX1 Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
23:20	R/W	0x0	TX1_CH13_MAP TX1 Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX1_CH12_MAP TX1 Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX1_CH11_MAP TX1 Channel 11 Mapping 0000: 1st Sample ...

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
11:8	R/W	0x0	TX1_CH10_MAP TX1 Channel 10 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX1_CH9_MAP TX1 Channel 9 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX1_CH8_MAP TX1 Channel 8 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

9.1.6.21. 0x0050 I2S/PCM TX1 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: I2S/PCM_TX1CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX1_CH7_MAP TX1 Channel 7 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX1_CH6_MAP TX1 Channel 6 Mapping 0000: 1st Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			… 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX1_CH5_MAP TX1 Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX1_CH4_MAP TX1 Channel 4 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX1_CH3_MAP TX1 Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	TX1_CH2_MAP TX1 Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX1_CH1_MAP TX1 Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:0	R/W	0x0	TX1_CH0_MAP TX1 Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

9.1.6.22. 0x0054 I2S/PCM TX2 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S/PCM_TX2CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX2_CH15_MAP TX2 Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX2_CH14_MAP TX2 Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
23:20	R/W	0x0	TX2_CH13_MAP TX2 Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX2_CH12_MAP TX2 Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ...

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1111: 16th Sample
15:12	R/W	0x0	TX2_CH11_MAP TX2 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX2_CH10_MAP TX2 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX2_CH9_MAP TX2 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX2_CH8_MAP TX2 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.23. 0x0058 I2S/PCM TX2 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S/PCM_TX2CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX2_CH7_MAP TX2 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			... 1111: 16th Sample
27:24	R/W	0x0	TX2_CH6_MAP TX2 Channel 6 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	TX2_CH5_MAP TX2 Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX2_CH4_MAP TX2 Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX2_CH3_MAP TX2 Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	TX2_CH2_MAP TX2 Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX2_CH1_MAP TX2 Channel 1 Mapping 0000: 1st Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			… 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX2_CH0_MAP TX2 Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.24. 0x005C I2S/PCM TX3 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: I2S/PCM_TX3CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX3_CH15_MAP TX3 Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX3_CH14_MAP TX3 Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX3_CH13_MAP TX3 Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX3_CH12_MAP TX3 Channel 12 Mapping

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX3_CH11_MAP TX3 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX3_CH10_MAP TX3 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX3_CH9_MAP TX3 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX3_CH8_MAP TX3 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.25. 0x0060 I2S/PCM TX3 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: I2S/PCM_TX3CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX3_CH7_MAP

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TX3 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX3_CH6_MAP TX3 Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX3_CH5_MAP TX3 Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX3_CH4_MAP TX3 Channel 4 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX3_CH3_MAP TX3 Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	TX3_CH2_MAP TX3 Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			... 1111: 16th Sample
7:4	R/W	0x0	TX3_CH1_MAP TX3 Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX3_CH0_MAP TX3 Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

9.1.6.26. 0x0064 I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX Offset Tune(RX Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	/	/	/

9.1.6.27. 0x0068 I2S/PCM RX Channel Mapping Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:30	/	/	/
29:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample

9.1.6.28. 0x006C I2S/PCM RX Channel Mapping Register1(Default Value: 0x0000_0000)

Offset: 0x006C			**Register Name: I2S/PCM_RXCHMAP1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample

9.1.6.29. 0x0070 I2S/PCM RX Channel Mapping Register2(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: I2S/PCM_RXCHMAP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 000000: 1st Sample … 000111: 8th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			001000: 9th Sample ... 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

9.1.6.30. 0x0074 I2S/PCM RX Channel Mapping Register3(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:22	/	/	/
21:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2. DMIC

9.2.1. Overview

The DMIC controller supports one 8-channels digital microphone interface, the DMIC controller can output 128fs or 64fs (fs= ADC sample rate).

The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

9.2.2. Block Diagram

Figure 9-9 shows a block diagram of the DMIC.

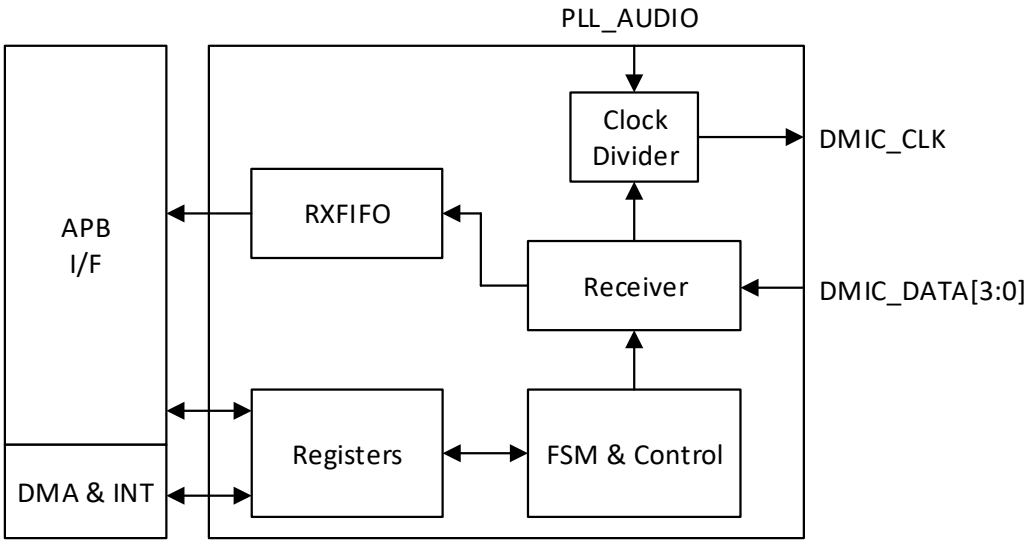


Figure 9- 9. DMIC Block Diagram

9.2.3. Operations and Functional Descriptions

9.2.3.1. External Signals

Table 9-4 describes the external signals of DMIC.

Table 9- 4. DMIC External Signals

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Signal	Description	Type
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA0	Digital Microphone Data Input	I
DMIC_DATA1	Digital Microphone Data Input	I
DMIC_DATA2	Digital Microphone Data Input	I
DMIC_DATA3	Digital Microphone Data Input	I

9.2.3.2. Clock Sources

Table 9-5 describes the clock source for DMIC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 9- 5. DMIC Clock Sources

Clock Sources	Description
PLL_AUDIO(4X)	The 98.304 MHz frequency generated by PLL_AUDIO(4X) to produce 48 kHz sample frequency.
PLL_COM_AUDIO	The 90.3168 MHz frequency generated by PLL_COM_AUDIO is divided by 4(=22.5792 MHz) and then passed to the module to produce 44.1 kHz sample frequency.
APB CLK	The frequency must be greater than 24MHz in order to write RXFIFO data.

9.2.3.3. Operation Mode

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup and Enable/Disable module. Five steps are described in detail in the following sections.

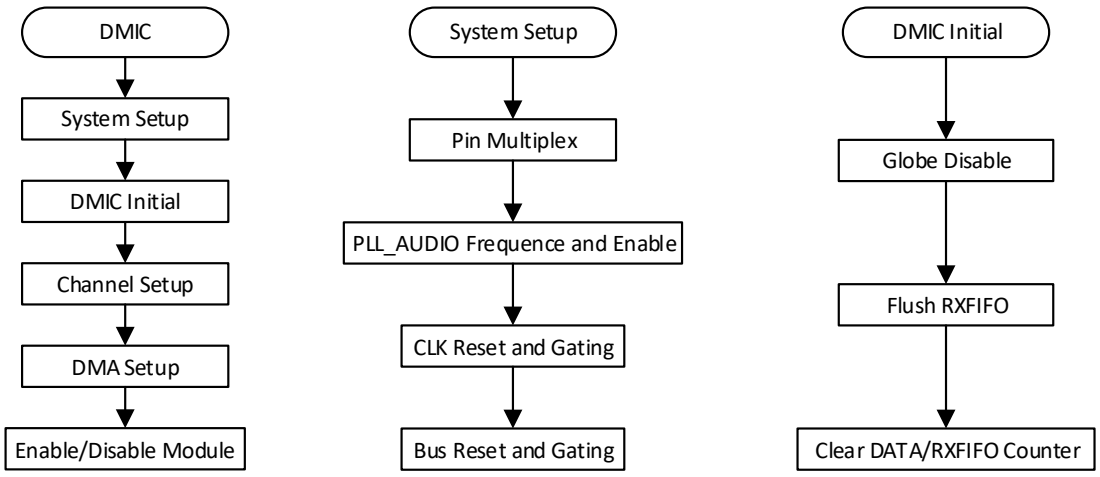


Figure 9- 10. DMIC Operation Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2.3.3.1. System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO. Because the DMIC port is a multiplex pin. You can find the function in the pin multiplex specification.

The clock source for the DMIC should be followed. At first you must disable the PLL_AUDIO through the PLL_ENABLE bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. Then enable PLL_AUDIO. After that, you must open the DMIC gating through the **DMIC_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes 1. At last, you must reset and open the DMIC bus gating in the **DMIC_BGR_REG**.

After the system setup, the register of DMIC can be setup. At first, you should initialize the DMIC. You should close the **globe enable bit**(DMIC_EN[8]) , **data channel enable bit**(DMIC_EN[7:0]) by writing 0 to it. After that, you must flush the RXFIFO by writing 1 to **DMIC_RXFIFO_CTR**[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to **DMIC_RXFIFO_STA, DMIC_CNT**.

9.2.3.3.2. Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over sample rate, the channel number, the RXFIFO output mode and the RXFIFO trigger level and so on. The setup of register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the DMA specification. In this module, you just enable the DRQ.

9.2.3.3.3. Enable and Disable DMIC

To enable the function, you can enable **data channel enable bit** (DMIC_EN[7:0]) by writing 1 to it. After that, you must enable DMIC by writing 1 to the **Globe Enable bit** (DMIC_EN[8]). Write 0 to **Globe Enable bit** to disable DMIC.

9.2.4. Register List

Module Name	Base Address
DMIC	0x05095000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_ DATA	0x0010	DMIC Data Register
DMIC_INTC	0x0014	MIC Interrupt Control Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	Data0 and Data1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	Data2 And Data3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

9.2.5. Register Description

9.2.5.1. 0x0000 DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: DMIC_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	RX_SYNC_EN Audio/I2S/DMIC RX (GLOBE_EN) Synchronize Enable 0: Disable 1: Enable
28	R/W	0x0	RX_EN_MUX Audio RX (GLOBE_EN) Enable MUX 0: Disable 1: Enable
27:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disable 1: Enable
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

9.2.5.2. 0x0004 DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

9.2.5.3. 0x0008 DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5ms 01: 10ms 10: 20ms 11: 30ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disable 1: Enable
7	R/W	0x0	DATA3 Left Data and Right Data Swap Enable 0: Disable 1: Enable
6	R/W	0x0	DATA2 Left Data and Right Data Swap Enable 0: Disable 1: Enable
5	R/W	0x0	DATA1 Left Data and Right Data Swap Enable 0: Disable 1: Enable
4	R/W	0x0	DATA0 Left Data and Right Data Swap Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Support 8 kHz ~ 24 kHz) 1: 64 (Support 16 kHz ~ 48 kHz)

9.2.5.4. 0x0010 DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMIC_DATA

9.2.5.5. 0x0014 DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disable 1: Enable

9.2.5.6. 0x0018 DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.

9.2.5.7. 0x001C DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_FIFO_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self clear to '0'
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[20:0],11'h0}

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Mode 1: APB_RDATA[31:0] = {8{RXFIFO[20]}, RXFIFO[20:0],3'h0} For 16-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[20:5], 16'h0} Mode 1: APB_RDATA[31:0] = {16{RXFIFO[20]}, RXFIFO[20:5]}
8	R/W	0x0	Sample_Resolution 0: 16-bit 1: 24-bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV[7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV[7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

9.2.5.8. 0x0020 DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

9.2.5.9. 0x0024 DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N+1).

9.2.5.10. 0x0028 DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

9.2.5.11. 0x002C DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			**Register Name: DMIC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **Note: It is used for Audio/Video Synchronization.**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2.5.12. 0x0030 DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA1L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2.5.13. 0x0034 DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA3L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA3R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2.5.14. 0x0038 High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disable 1: Enable

9.2.5.15. 0x003C High Pass Filter Coef Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFAA45	High Pass Filter Coefficient

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.2.5.16. 0x0040 High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFD522	High Pass Filter Gain

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.3. OWA

9.3.1. Overview

The One Wire Audio(OWA) provides a serial bus interface for audio data between system. This interface is widely used for consumer audio.

The OWA controller includes the following features:

- IEC-60958 transmitter functionality
- Compliance with S/PDIF interface
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit, 20-bit, 24-bit data formats

9.3.2. Block Diagram

The block diagram of the OWA is shown as follows.

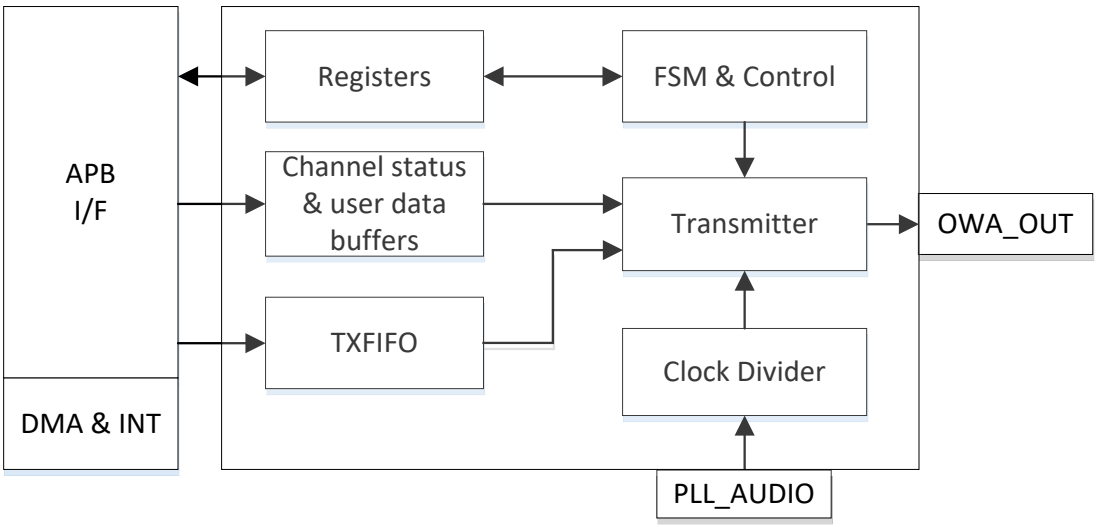


Figure 9- 11. OWA Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.3.3. Operations and Functional Descriptions

9.3.3.1. External Signals

OWA is a Biphase-Mark Encoding Digital Audio Transfer protocol. In this protocol, the clock signal and data signal are transferred in the same line. Table 9-6 describes the external signals of OWA. OWA_OUT is output pin for output clock and data.

Table 9- 6. OWA External Signals

Signal Name	Description	Type
OWA_OUT	OWA output	O

9.3.3.2. Clock Sources

Table 9-7 describes the clock sources for OWA. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 9- 7. OWA Clock Sources

Clock Name	Description
PLL_AUDIO(4X)	The 98.304 MHz frequency generated by PLL_AUDIO(4X) to produce 48 kHz sample frequency.
PLL_COM_AUDIO	The 90.3168 MHz frequency generated by PLL_COM_AUDIO is divided by 4(=22.5792 MHz) and then passed to the module to produce 44.1 kHz sample frequency.

9.3.3.3. Biphase-Mark Code (BMC)

In OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal—the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. Figure 9-12 and Table 9-8 show how data is encoded to the BMC format.

As shown in Figure 9-12, the frequency of the clock is twice the data bit rate. In addition, the clock is always programmed to 128xfs, where fs is the sample rate. The device receiving in OWA format can recover the clock and frame information from the BMC signal.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

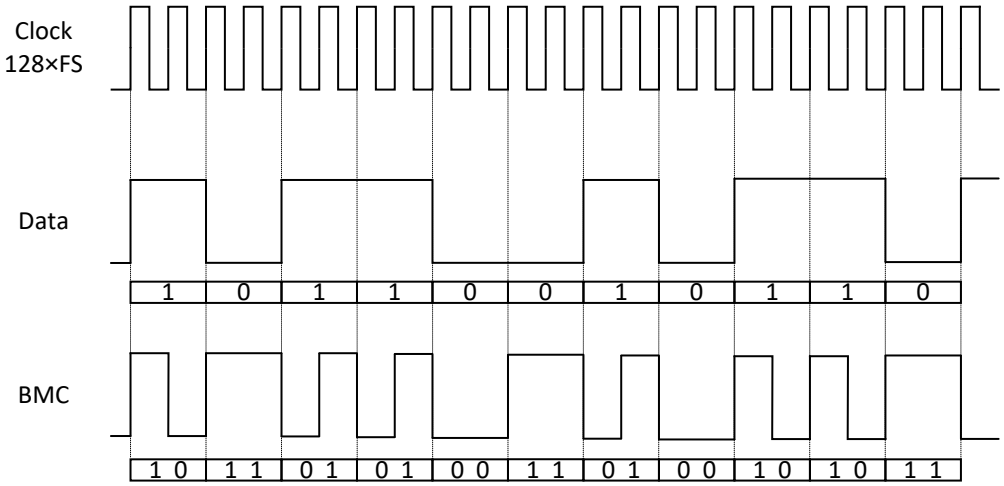


Figure 9- 12. OWA Biphase-Mark Code

Table 9- 8. Biphase-Mark Encoder

Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

9.3.3.4. OWA Transmit Format

The OWA supports digital audio data transfer out and receive in. And it supports full-duplex synchronous work mode. Software can set the work mode by the OWA Control Register.

Every audio sample transmitted in a subframe consists of 32-bit, numbered from 0 to 31. Figure 9-13 shows a subframe.

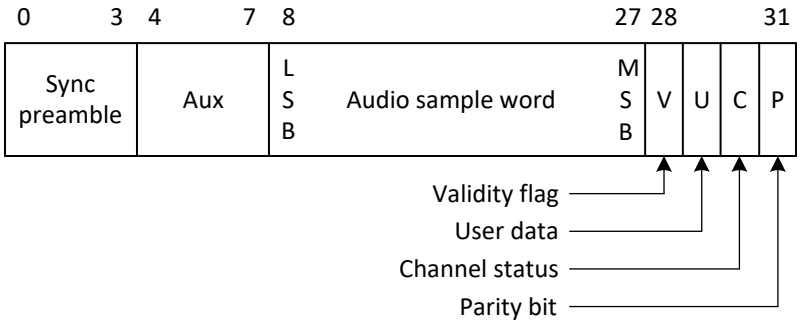


Figure 9- 13. OWA Sub-Frame Format

Bit 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

or 1 logical states in a row. See Table 9-8.

Bit 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the least-significant bit (LSB) is in bit 4. When a 20-bit coding range is used, bit 8-27 carry the audio sample word with the LSB in bit 8. Bit 4-7 may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the subframe.

Bit 29 carries the user data channel (U) associated with the main data field in the subframe.

Bit 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.

Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in Table 9-9, the preambles (bit 0-3) are also defined with even parity.

Table 9- 9. Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B(or Z)	0	1110 1000	Start of a block and subframe 1
M(or X)	0	1110 0010	Subframe 1
W(or Y)	0	1110 0100	Subframe 2

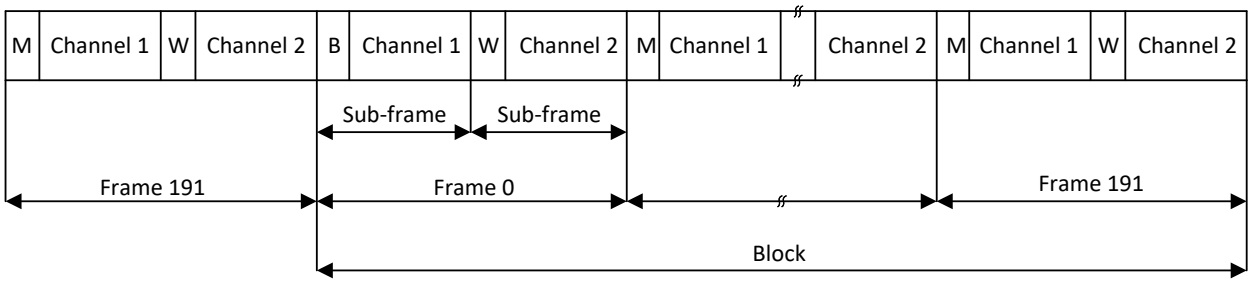


Figure 9- 14. OWA Frame/Block Format

9.3.3.5. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, channel setup, DMA setup and enable/disable module. These five steps are described in detail in the following sections.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

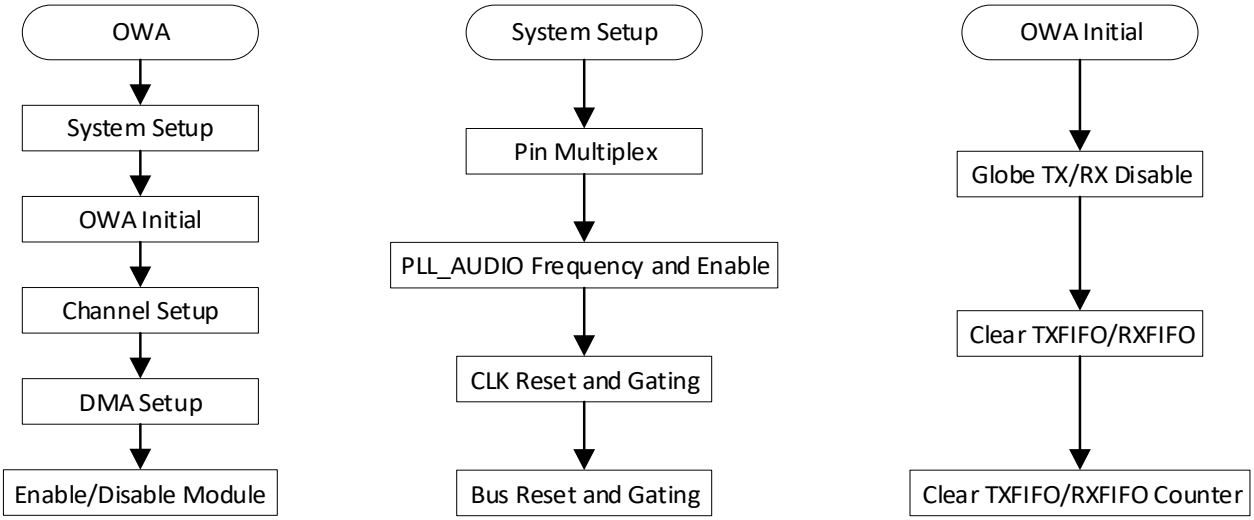


Figure 9- 15. OWA Operation Flow

(1) System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO. Because the OWA port is a multiplex pin. You can find the function in the **Port Controller**.

The clock source for the OWA should be followed. At first you must reset the audio PLL in the **CCU**. The second step, you must setup the frequency of the Audio PLL. After that, you must open the OWA gating. At last, you must open the OWA bus gating.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to **OWA_CTL**[0] and clear the TX FIFO by writing 1 to **OWA_FCTL**[30]. After that you should enable the globe enable bit by writing 1 to **OWA_CTL**[1], and clear the interrupt and TX counter by the **OWA_ISTA** and **OWA_TX_CNT**.

(2) Channel Setup and DMA Setup

The OWA supports two methods to transfer the data. The most common way is DMA, the configuration of DMA can be found in the **DMA**. In this module, you just enable the DRQ by writing the **OWA_INT**[7].

(3) Enable and Disable OWA

To enable the function, you can enable TX by writing the **OWA_TX_CFIG**[0]. After that, you must enable OWA by writing 1 to the **GEN** bit in the **OWA_CTL** register. Writing 0 to the **GEN** bit to disable process.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.3.4. Register List

Module Name	Base Address
OWA	0x05094000

Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1

9.3.5. Register Description

9.3.5.1. 0x0000 OWA General Control Register (Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:5	R/W	0x4	MCLKDIV MCLK Clock Divide Ratio MCLK Divide Ratio from PLL_AUDIO 00000: Divide by 128 00001: Divide by 2 00010: Divide by 4 00011: Divide by 6 00100: Divide by 8 00101: Divide by 10 00110: Divide by 12 00111: Divide by 14 01000: Divide by 16 01001: Divide by 18 01010: Divide by 20 01011: Divide by 22 01100: Divide by 24 …… 11111: Divide by 62
4	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	R/W	0x0	MCLKEN MCLK Enable 0: Disable 1: Enable
2	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1', DOUT and DIN need be connected.
1	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W	0x0	RST Reset 0: Normal 1: Reset Self clear to 0.

9.3.5.2. 0x0004 OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			**Register Name: OWA_TX_CFIG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_SINGLE_MODE Tx Single Channel Mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select with TX FIFO Underrun when 0: Sending 0 1: Sending the last audio **Note: This bit is only valid in PCM mode.**
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX_TATIO +1 Fs= PLL_AUDIO/[(TX_TATIO +1)*64*2]

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated from TX_CHSTA
0	R/W	0x0	TXEN 0: Disabled 1: Enabled

9.3.5.3. 0x000C OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt Writing “1” to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing “1” to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing “1” to clear this interrupt or automatically clear if the interrupt condition fails.
3:0	/	/	/

9.3.5.4. 0x0014 OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
30	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
29:20	/	/	/
19:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11:3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of TXFIFO Register 1: Valid data at the LSB of TXFIFO Register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[23:0] = {APB_WDATA[31:12], 4'h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4'h0}
1:0	/	/	/

9.3.5.5. 0x0018 OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x1	TXE TXFIFO Empty (indicate TXFIFO is not full) 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>=1 Word)
30:24	/	/	/
23:0	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter

9.3.5.6. 0x001C OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3:0	/	/	/

9.3.5.7. 0x0020 OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

9.3.5.8. 0x0024 OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter This is the audio sample number sent into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on base of this initial value.

9.3.5.9. 0x002C OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sample Frequency 0000: 44.1 kHz 0001: Not indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs / 15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001~111: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM sample 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application This bit must be fixed to “0”.

9.3.5.10. 0x0030 OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			**Register Name: OWA_TX_CHSTA1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sample Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R/W	0x0	WL Sample Word Length

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4. Audio Codec

9.4.1. Overview

The A133 is integrated with high-performance audio codec, including two high-quality playback DAC channels (95 dB SNR), two differential microphone inputs; two high-quality recording ADC channels (95 dB SNR), one stereo headphone output and one single-ended differential line output.

The Audio Codec has the following features:

- Two DAC channels
  - Supports 8 kHz to 192 kHz DAC sample rate
  - SNR 95 dB ± 3 dB
  - Supports 16-bit and 20-bit audio sample resolution
- Two audio outputs
  - One stereo headphone output (HPOUTL and HPOUTR)
  - One single-ended differential line output (LINEOUTLP and LINEOUTLN)
- Two ADC channels
  - Supports 8 kHz to 48 kHz ADC sample rate
  - SNR 95 dB ± 3 dB
  - Supports 16-bit and 20-bit audio sample resolution
- Two audio inputs
  - Two differential microphone inputs (MICIN1P/N and MICIN2P/N)
- Capless stereo headphone driver
  - 95 dB ± 3 dB SNR@A-weight, THD+N -77 dB ± 3 dB
  - Output Level 0.56 Vrms@10 kOhm, 0.4Vrms@16 Ohm
- Two low-noise analog microphone bias outputs
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback and ADC capture
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Interrupt and DMA support

9.4.2. Block Diagram

Figure 9-16 shows the block diagram of Audio Codec.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

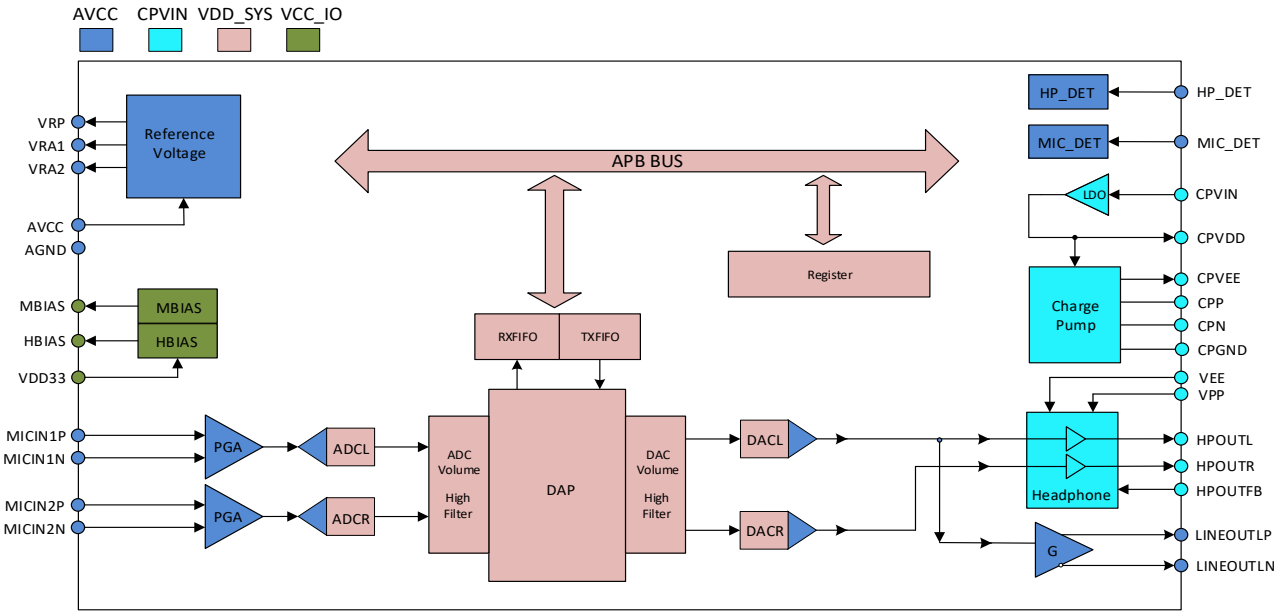


Figure 9- 16. Audio Codec Block Diagram

9.4.3. Operations and Functional Descriptions

9.4.3.1. External Signals

9.4.3.1.1. Analog I/O Pins

Signal	Type	Description
MICIN1P	AI	Positive differential input for MIC1
MICIN1N	AI	Negative differential input for MIC1
MICIN2P	AI	Positive differential input for MIC2
MICIN2N	AI	Negative differential input for MIC2
HPOUTL	AO	Headphone left output
HPOUTR	AO	Headphone right output
LINEOUTLP	AO	Positive differential output for lineout
LINEOUTLN	AO	Negative differential output for lineout
MIC_DET	AI	Headphone MIC detect
HP_DET	AI	Headphone Jack detect

9.4.3.1.2. Reference

Signal	Type	Description
MBIAS	AO	First bias voltage output for main microphone
HBIAS	AO	Second bias voltage output for headset microphone
HPOUTFB	AI	Pseudo differential headphone ground reference

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

VRA1	AO	Internal reference voltage
VRA2	AO	Internal reference voltage

9.4.3.1.3. Power/Ground

Signal	Type	Description
AVCC	P	Analog power 1.8 V
AGND	G	Analog ground
CPVIN	P	Analog power for LDO
CPVDD	P	Analog power for headphone charge pump
CPVEE	P	Charge pump negative voltage output
VEE	P	PA negative voltage input

9.4.3.2. Clock Sources

Figure 9-17 describes the Audio Codec clock source. Users can see ***CCU*** for clock setting, configuration and gating information.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

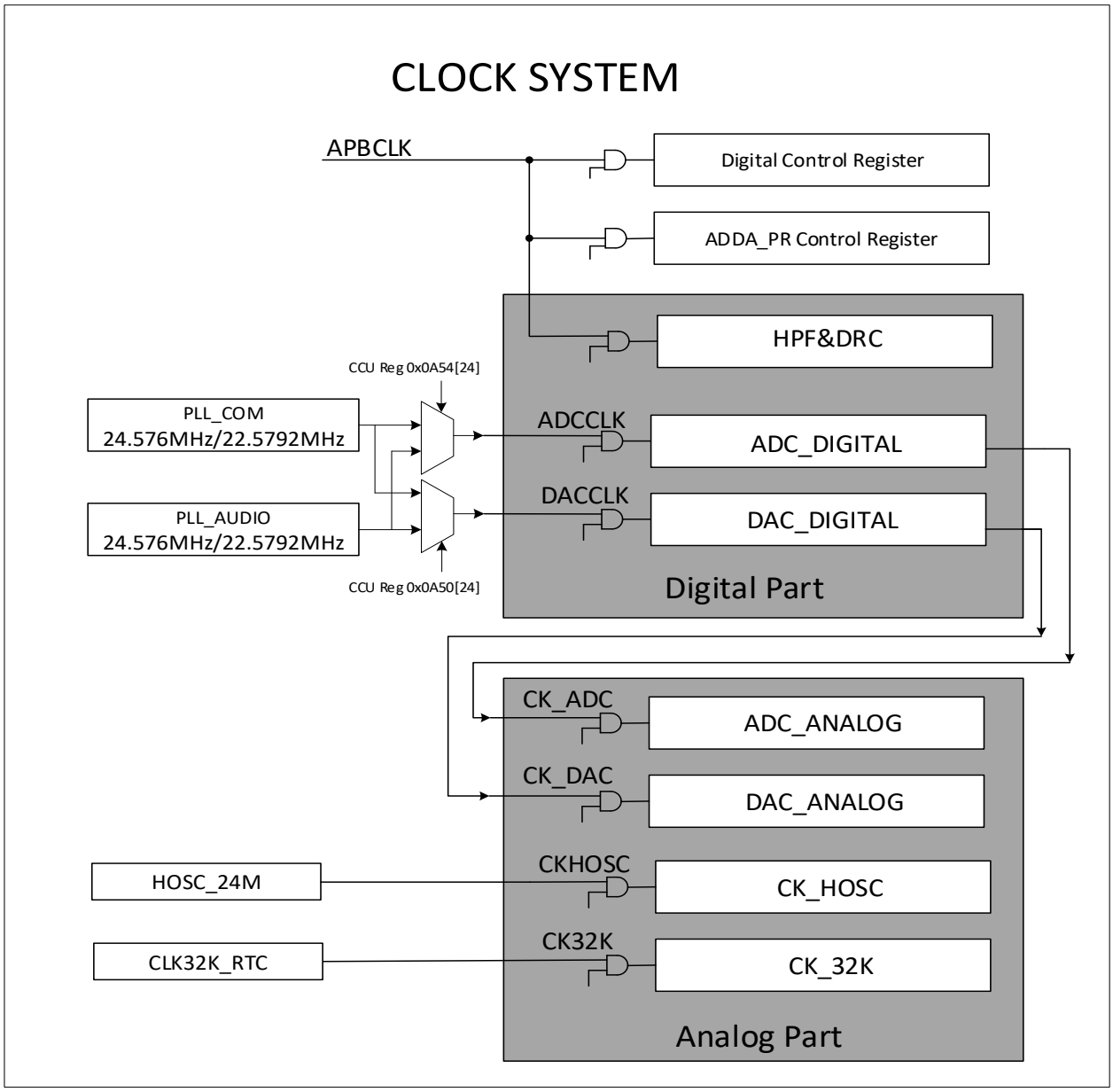


Figure 9- 17. Audio Codec Clock Diagram

The clocks of digital part are from PLL_AUDIO and PLL_COM. The clock is connected to ADCCLK by configuring the reg0x0A54[24] of CCU module; and the clock is connected to DACCLK by configuring the reg0x0A50[24] of CCU module.

The clocks of analog part include CK_ADC, CK_DAC, CHHOSC, CK32K. Where, CK_ADC and CK_DAC are provided by the digital divider of codec. CHHOSC and CK32K are provided by system oscillator 24M. These clocks need ensure that VDD-SYS is not power-off.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.3.3. Reset System

9.4.3.3.1. Digital Part Reset System

The SYS_RST will be provided by the VDD_SYS domain, which comes from VDD_SYS domain and is produced by RTC domain. Each domain has the de-bounce to confirm whether the reset system is strong. The codec register part, MIX will be reset by the SYS_RST during the power on or the system soft writing the reset control logic. The other parts will be reset by the soft configuration through writing register.

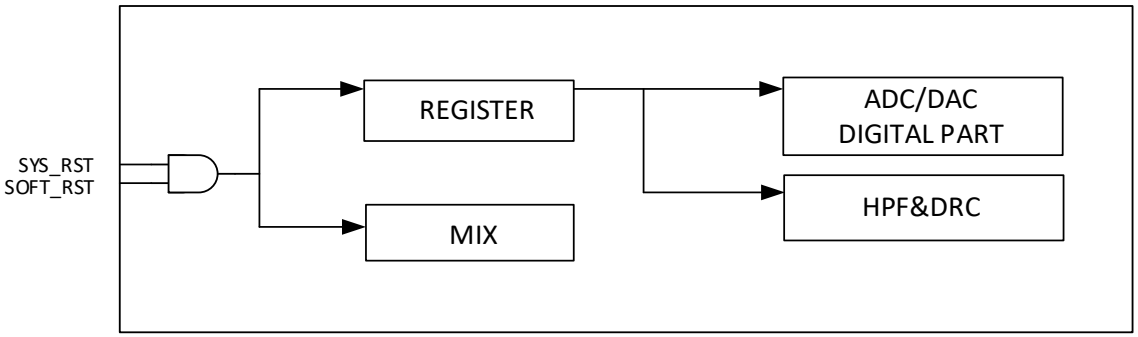


Figure 9- 18. Audio Codec Digital Part Reset System

9.4.3.3.2. Analog Part Reset System

When AVCC is powered on, it will send the AVCC_POR signal. And the AVCC_POR signal passes the level shift and RC filter part to ADDA logic core, which will reset the AVCC analog part.

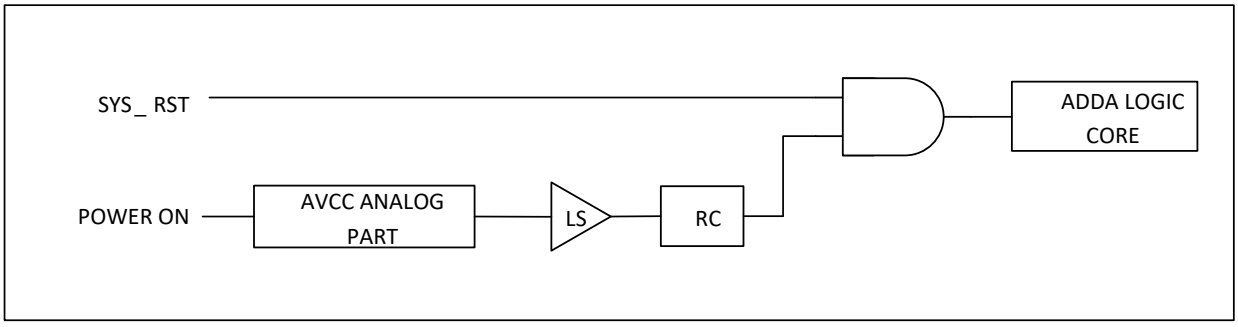


Figure 9- 19. Audio Codec Analog Part Reset System

9.4.3.4. Data Path Diagram

Figure 9-20 shows a data path of the Audio Codec.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

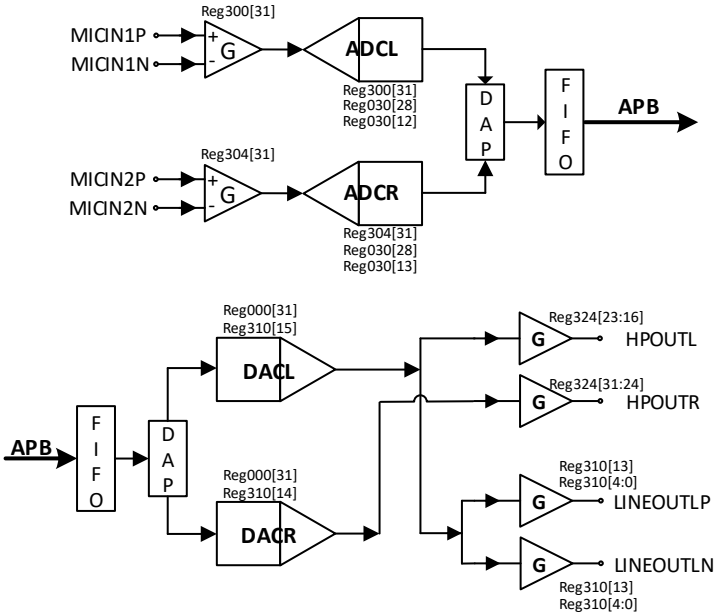


Figure 9- 20. Audio Codec Data Path Diagram

9.4.3.5. Two ADC

The two ADC is used for recording sound and a reference signal. The sample rate of the two ADC is independent of DAC sample rate. The digital ADC part can be enabled/disabled by the bit[28] of the AC_ADC_FIFOC register.

9.4.3.6. Stereo DAC

In order to save power, the DAC can be enabled/disabled by setting the bit[15:14] of the DAC_REG register. The digital DAC part can be enabled/disabled by the bit[31] of the AC_DAC_DPC register.

9.4.3.7. Analog Audio Input Port

The Codec supports four analog audio input paths:

- MICIN1P/N
- MICIN2P/N

MICIN1P/N, MICIN2P/N provide differential input. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. The gain for each pre-amplifier can be set independently. MBIAS provide reference voltage for electret condenser type(ECM) microphones.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.3.8. Analog Audio Output Port

The Codec has two type analog output ports:

- LINEOUTLP
- LINEOUTLN
- HPOUTL
- HPOUTR

9.4.3.8.1. LINEOUTL

LINEOUTL provides one differential output to drive line signals to external audio equipment. The LINEOUTLP/N output source is from DACL. The volume control is logarithmic with an 43.5 dB rang in 1.5 dB step from -43.5 dB to 0 dB. The LINEOUTL output buffer is powered up or down by the bit13 of the DAC_REG register.

9.4.3.8.2. Headphone Output

The headphone PA is powered up or down by the bit15(HPPA_EN) of the HP_REG register. HPOUTL/R can drive a 16R or 32R headphone load without DC capacitors by using Charge Pump to generate the negative rails. HP-FB is the ground loop noise rejection feedback. HBIAS provides reference voltage for electret condenser type(ECM) microphones.

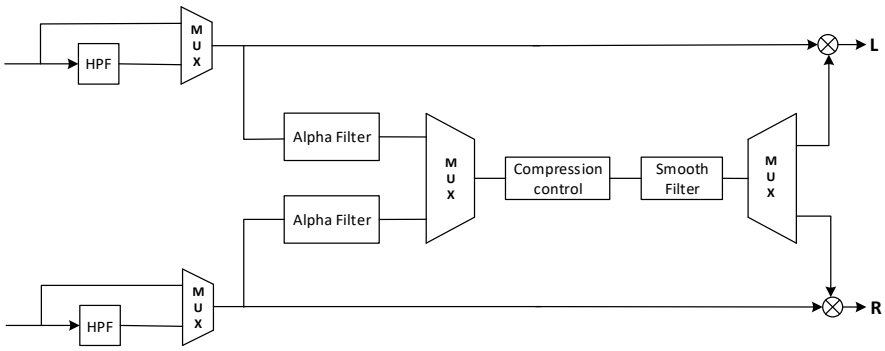


Figure 9- 21. Headphone Output Application

9.4.3.8.3. External Accessory Detection

The codec provides external accessory detection functions which can sense the presence and impedance of external components. This can be used to detect the insertion and removal of headphone.

Headphone insertion is detected using the HP-DET pin, which must be connected to switch contacts within the jack socket. An interrupt event is generated whenever a headphone insertion or removal event is detected.

Microphones, push-buttons and other accessories can be detected via the MIC-DET pin. The presence of a microphone, and the status of a hook switch can be detected. This feature also can be used to detect push-button operation.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The 24 MHz oscillator clock is required for all of External accessory detection functions.

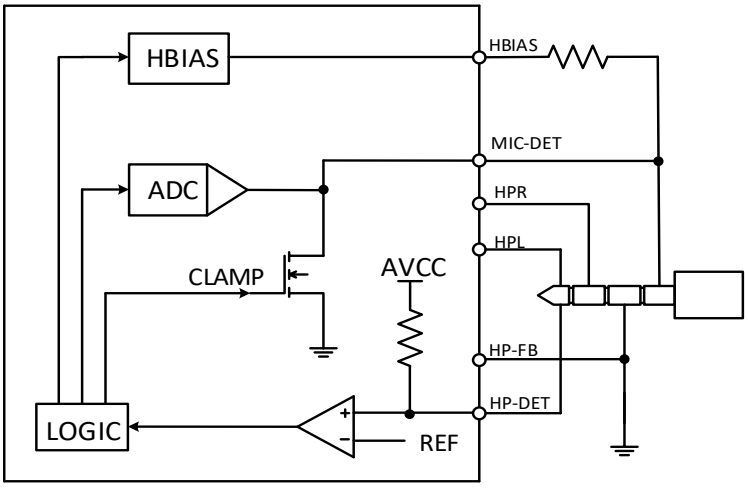


Figure 9- 22. External Accessory Detection

9.4.3.9. Microphone BIAS

The MBIAS/HBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

9.4.3.10. Interrupt

Figure 9-23 describes the Audio Codec interrupt system.

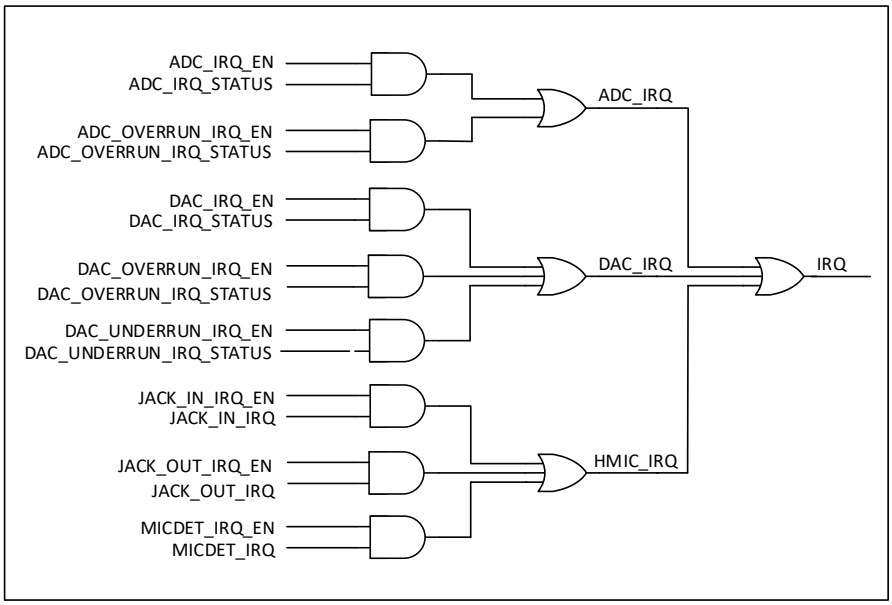


Figure 9- 23. Audio Codec Interrupt System

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.3.11. DAP

9.4.3.11.1. DAP Data Flow

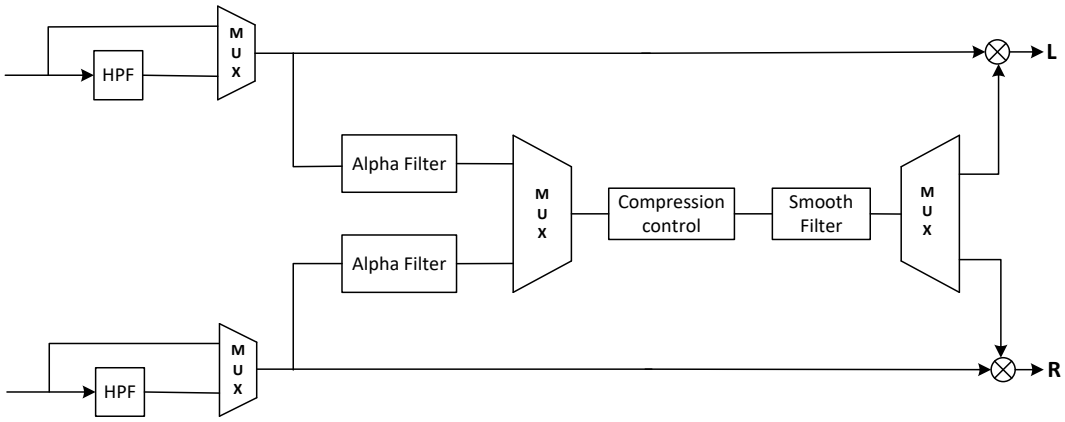


Figure 9- 24. DAP Data Flow

9.4.3.11.2. HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enable and disable. The filter cutoff frequency is less than 1 Hz that can be remove DC offset from ADC recording. The HPF can also be bypassed.

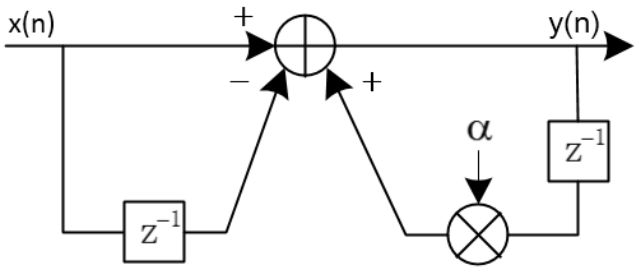


Figure 9- 25. HPF Function

9.4.3.11.3. DRC Function

The DRC scheme has three thresholds, three offsets, and four slopes (all programmable). There is one ganged DRC for the left/right channels. The diagram of DRC input/output is as follows.

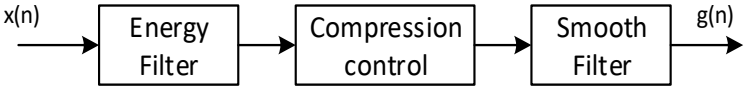


Figure 9- 26. DRC Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

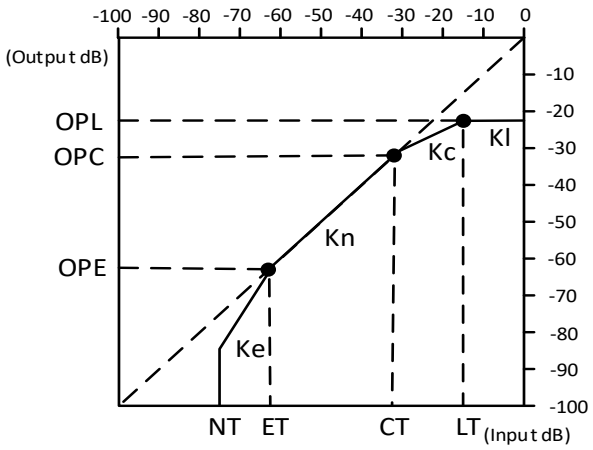


Figure 9- 27. DRC Static Curve Parameters

Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

One DRC is for left/right, and one DRC is for subwoofer.

Each DRC has adjustable threshold, offset, and compression levels, programmable energy, attack, and decay time constants.

Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

DRC parameter setting:

- **Number format**

The number format is N.M which means there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 9.23 means that there are 9 bits at the left of the decimal point and 23 bits at the right decimal point.

- **Energy Filter**

The energy filter is to estimate the RMS value of the audio data stream into DRC, and has two parameters, which determines the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2Ts/ta}$.

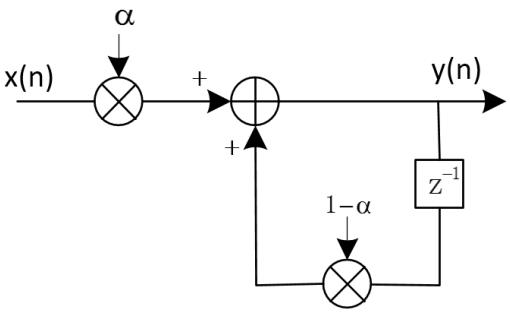


Figure 9- 28. Energy Filter Structure

Compression Control

This element has ten parameters (ET, CT, LT, Ke, Kn, Kc, Kl, OPL, OPC, OPE), which are all programmable, and the computation will be explained as follows.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- **Threshold Parameter Computation(T parameter)**

The threshold is the value that determines the signal to be compressed or not. When the RMS of the signal is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

There, T_{dB} must less than zero, the positive value is illegal.

For example, it is desired to set CT=-40dB, then the Tin require to set CT to -40dB is CT_{in} = - (-40dB)/6.0206 = 6.644, CT_{in} is entered as a 32-bit number in 8.24 format.
Therefore, CT_{in} = 6.644 = 0000 0110.1010 0100 1101 0011 1100 0000 = 0x06A4 D3C0 in 8.24 format.

- **Slope Parameter Computation (K parameter)**

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB is for n dB RMS input. The k input to the coefficient ram is computed by $K = \frac{1}{n}$

There, n is from 1 to 50, and must be integer.
For example, it is desired to set 2:1, then the Kc require to set to 2:1 is Kc = 1/2 = 0.5, Kc is entered as a 32-bit number in 8.24 format.
Therefore, Kc = 0.5 = 0000 0000.1000 0000 0000 0000 0000 0000 = 0x0080 0000 in 8.24 format.

- **Gain Smooth Filter**

The gain smooth filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 9-29. The structure of the gain smooth filter is also the Alpha filter, so the rise time computation is the same as the energy filter which is $\alpha = 1 - e^{-2.2Ts/ta}$.

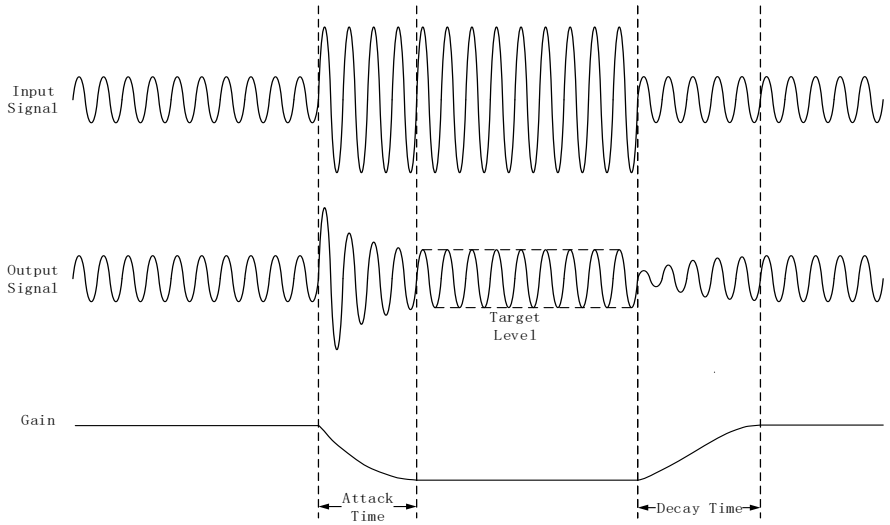


Figure 9- 29. Gain Smooth Filter

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.4. Programming Guidelines

9.4.4.1. Playback Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate, configure data transfer format, enable DAC.
(4) DMA configure and DMA request.
(5) Enable DAC DRQ and DMA.

9.4.4.2. Recording Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate, configure data transfer format, enable ADC.
(4) DMA configure and DMA request.
(5) Enable ADC DRQ and DMA.

9.4.5. Register List

Module Name	Base Address
Audio Codec	0x05096000

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
DAC_VOL_CTRL	0x0004	DAC Volume Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
ADC_VOL_CTRL	0x0034	ADC Volume Control Register
AC_ADC_FIFOS	0x0038	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0118	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth Filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth Filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth Filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_OPT	0x01B4	DAC DRC Optimum Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth Filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth Filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth Filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGLS	0x02A4	ADC DRC MIN Gain High Setting Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

AC_ADC_DRC_MXGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_OPT	0x02B4	ADC DRC Optimum Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
Analog Domain Register		
ADCL_REG	0x0300	ADCL Analog Control Register
ADCR_REG	0x0304	ADCR Analog Control Register
DAC_REG	0x0310	DAC Analog Control Register
MICBIAS_REG	0x0318	MICBIAS Analog Control Register
BIAS_REG	0x0320	BIAS Analog Control Register
HP_REG	0x0324	HEADPHONE Analog Control Register
HMIC_CTRL	0x0328	HMIC Control Register
HMIC_STS	0x032C	HMIC Status Register

9.4.6. Register Description

9.4.6.1. 0x0000 DAC Digital Part Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: AC_DAC_DPC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable

9.4.6.2. 0x0004 DAC Volume Control Register(Default Value: 0x0000_A0A0)

Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DAC_VOL_SEL DAC Volume Control Selection Enable 0: Disable 1: Enable
15:8	R/W	0xA0	DAC_VOL_L DAC Left Channel Volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB
7:0	R/W	0xA0	DAC_VOL_R DAC Right Channel Volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB

9.4.6.3. 0x0010 DAC FIFO Control Register(Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 20-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:12]} 01/11: FIFO_I[19:0] = {TXDATA[19:0]} For 16-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:16], 4'b0} 01/11: FIFO_I[19:0] = {TXDATA[15:0], 4'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ generated when WLEVEL ≤ TXTL **Note: WLEVEL represents the number of valid samples in the TX FIFO.** **Only TXTL[6:0] valid when TXMODE = 0**
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: mono, 128 levels FIFO When enabled, L & R channel send same data.
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH DAC FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’

9.4.6.4. 0x0014 DAC FIFO Status Register(Default Value: 0x0080_8008)

Offset: 0x0014			**Register Name: AC_DAC_FIFOS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

9.4.6.5. 0x0020 DAC TX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

9.4.6.6. 0x0024 DAC TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: AC_DAC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **Note: It is used for Audio/Video Synchronization**

9.4.6.7. 0x0028 DAC Debug Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock is from PLL 1: CODEC Clock is from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC Output Channel Swap Enable 0: Disable 1: Enable
5:2	/	/	/
1:0	R/W	0x0	ADDA_LOOP_MODE ADDA Loop Mode Select 00: Disable 01: ADDA LOOP MODE DACL/DACR connects to ADCL/ADCR 1X: Reserved

9.4.6.8. 0x0030 ADC FIFO Control Register(Default Value : 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by PLL_Audio Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:26	R/W	0x0	ADCFDT ADC FIFO Delay Time for writing data after EN_AD

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00:5ms 01:10ms 10:20ms 11:30ms
25	R/W	0x0	ADCDFEN ADC FIFO Delay Function for writing data after EN_AD 0: Disable 1: Enable
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 20-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:0], 12'h0} Mode 1: RXDATA[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0],} For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:4], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
23:22	/	/	/
21	R/W	0x0	RX_SYNC_EN Audio/I2S/DMIC RX (EN_AD) Synchronize Enable 0: Disable 1: Enable
20	R/W	0x0	RX_EN_MUX Audio RX (EN_AD) Enable MUX 0: Disable 1: Enable
19:18	/	/	/
17	R/W	0x0	ADC_VOL_SEL ADC Volume Control Selection Enable 0: Disable 1: Enable
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 20 bits
15:14	/	/	/
13:12	R/W	0x0	ADC_CHANNEL_EN Bit 13: ADCR enable Bit 12: ADCL enable
11	/	/	/
10:4	R/W	0x40	RX_FIFO_TRG_LEVEL. RX FIFO Trigger Level (RXTL[5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			IRQ/DRQ Generated when WLEVEL > RXTL[5:0] **Note: WLEVEL represents the number of valid samples in the RX FIFO.**
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'.

9.4.6.9. 0x0034 ADC Volume Control Register(Default Value: 0x0000_A0A0)

Offset: 0x0034			**Register Name: ADC_VOL_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0xA0	ADC_VOL_L ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB
7:0	R/W	0xA0	ADC_VOL_R ADC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			…… 0xFF = 71.25dB

9.4.6.10. 0x0038 ADC FIFO Status Register(Default Value : 0x0000_0000)

Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:15	/	/	/
14:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/WC	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/WC	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt
0	/	/	/

9.4.6.11. 0x0040 ADC RX DATA Register(Default Value : 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.4.6.12. 0x0044 ADC RX Counter Register(Default Value : 0x0000_0000)

Offset: 0x0044	Register Name: AC_ADC_CNT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

9.4.6.13. 0x004C ADC Debug Register(Default Value : 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP ADC output channel swap enable (for digital filter) 0: disable 1: enable
23:0	/	/	/

9.4.6.14. 0x00F0 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP_EN DAP for DRC Enable 0: Bypass 1: Enable
30	/	/	/
29	R/W	0x0	DDAP_DRC_EN DRC enable control 0: Disable 1: Enable
28	R/W	0x0	DDAP_HPF_EN HPF enable control 0: Disable 1: Enable
27:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.15. 0x00F8 ADC DAP Control Register(Default Value : 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_DAP0_EN(adjust position, and two DRC use the same parameter) DAP for ADC enable 0:bypass 1:enable
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 enable control 0:disable 1:enable
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 enable control 0:disable 1:enable
27:0	/	/	/

9.4.6.16. 0x0100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.4.6.17. 0x0104 DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.4.6.18. 0x0108 DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable
5	R/W	0x0	DRC gain min limit enable When this function is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT /AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.4.6.19. 0x010C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

9.4.6.20. 0x0110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

9.4.6.21. 0x0118 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.4.6.22. 0x011C DAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.23. 0x0120 DAC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.4.6.24. 0x012C DAC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.4.6.25. 0x0130 DAC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.4.6.26. 0x013C DAC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (The default value is -40dB)

9.4.6.27. 0x0140 DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (The default value is -40dB)

9.4.6.28. 0x0144 DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0080	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is 2 : 1)

9.4.6.29. 0x0148 DAC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is 2 : 1)

9.4.6.30. 0x014C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24 (The default value is -40dB)

9.4.6.31. 0x0150 DAC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24 (The default value is -40dB)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.32. 0x0154 DAC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (The default value is -10dB)

9.4.6.33. 0x0158 DAC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

9.4.6.34. 0x015C DAC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0005	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.4.6.35. 0x0160 DAC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.4.6.36. 0x0164 DAC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			format is 8.24 (The default value is -25dB)

9.4.6.37. 0x0168 DAC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (The default value is -25dB)

9.4.6.38. 0x016C DAC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.4.6.39. 0x0170 DAC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.4.6.40. 0x0174 DAC DRC Expander Slope High Setting Register(Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.4.6.41. 0x0178 DAC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.4.6.42. 0x017C DAC DRC Expander High Output at Expander Threshold Register(Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.43. 0x0180 DAC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.44. 0x0184 DAC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

9.4.6.45. 0x0188 DAC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.46. 0x018C DAC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.4.6.47. 0x0190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.4.6.48. 0x0194 DAC DRC Smooth Filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.4.6.49. 0x0198 DAC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.4.6.50. 0x019C DAC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

9.4.6.51. 0x01A0 DAC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

9.4.6.52. 0x01A4 DAC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.4.6.53. 0x01A8 DAC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

9.4.6.54. 0x01AC DAC DRC Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.55. 0x01B0 DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.4.6.56. 0x01B8 DAC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.4.6.57. 0x01BC DAC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.4.6.58. 0x0200 ADC DRC High HPF Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.4.6.59. 0x0204 ADC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.60. 0x0208 ADC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable
5	R/W	0x0	DRC gain min limit enable. When this fuction is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable
4	R/W	0x0	Control the drc to detect noise when ET is enabled 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused.(AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT/AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable 1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.4.6.61. 0x020C ADC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.4.6.62. 0x0210 ADC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.4.6.63. 0x021C ADC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.64. 0x0220 ADC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.4.6.65. 0x022C ADC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.4.6.66. 0x0230 ADC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.4.6.67. 0x023C ADC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

9.4.6.68. 0x0240 ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

9.4.6.69. 0x0244 ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0080	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

9.4.6.70. 0x0248 ADC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

9.4.6.71. 0x024C ADC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24. (The default value is -40dB)

9.4.6.72. 0x0250 ADC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24. (The default value is -40dB)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.73. 0x0254 ADC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

9.4.6.74. 0x0258 ADC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

9.4.6.75. 0x025C ADC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0005	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.4.6.76. 0x0260 ADC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.4.6.77. 0x0264 ADC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			format is 8.24. (The default value is -25dB)

9.4.6.78. 0x0268 ADC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25dB)

9.4.6.79. 0x026C ADC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.80. 0x0270 ADC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.81. 0x0274 ADC DRC Expander Slope High Setting Register(Default Value:0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.4.6.82. 0x0278 ADC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.4.6.83. 0x027C ADC DRC Expander High Output at Expander Threshold Register(Default Value:0x0000_F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.84. 0x0280 ADC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.4.6.85. 0x0284 ADC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger. The format is 8.24. (The default value is <1:1>)

9.4.6.86. 0x0288 ADC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger. The format is 8.24. (The default value is <1:1>)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.87. 0x028C ADC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.4.6.88. 0x0290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.4.6.89. 0x0294 ADC DRC Smooth Filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.4.6.90. 0x0298 ADC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.4.6.91. 0x029C ADC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

9.4.6.92. 0x02A0 ADC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

9.4.6.93. 0x02A4 ADC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.4.6.94. 0x02A8 ADC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.4.6.95. 0x02AC ADC DAP Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9.4.6.96. 0x02B0 ADC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.4.6.97. 0x02B8 ADC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.4.6.98. 0x02BC ADC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.4.6.99. 0x0300 ADCL Analog Control Register(Default Value: 0x000C_0055)

Default:0x0300			Register Name: ADCL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIC1AMPEN and ADCLEN MIC1 Boost AMP Enable and ADCL Channel Enable 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	Dither Reset 0: New dither off 1: New dither on
28:20	/	/	/
19:18	R/W	0x3	PGA_CTRL_RCM PGA Common Mode Input Impedance Control for MIC-IN (The AC coupling capacitance of MIC-IN is 100 nF. And the AC coupling capacitor combined with common-mode input resistor to form high-pass filter, the corresponding cut-off frequency is 20 Hz~80 Hz)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 100 kΩ 01: 75 kΩ 10: 50 kΩ 11: 25 kΩ
17:16	R/W	0x0	PGA_IN_VCM_CTRL High gain microphone input common mode voltage control(The field is the common-mode level control of MIC-IN when the gain is greater than or equal to 8 dB) 00 : 900 mV 01 : 800 mV 10 : 750 mV 11 : 700 mV
15:13	/	/	/
12:8	R/W	0x0	PGA_GAIN_CTRL PGA Gain Setting Control for MICIN 0 : 0 dB 16 : 21 dB 1 : 6 dB 17 : 22 dB 2 : 6 dB 18 : 23 dB 3 : 6 dB 19 : 24 dB 4 : 9 dB 20 : 25 dB 5 : 10 dB 21 : 26 dB 6 : 11 dB 22 : 27 dB 7 : 12 dB 23 : 28 dB 8 : 13 dB 24 : 29 dB 9 : 14 dB 25 : 30 dB 10 : 15 dB 26 : 31 dB 11 : 16 dB 27 : 32 dB 12 : 17 dB 28 : 33 dB 13 : 18 dB 29 : 34 dB 14 : 19 dB 30 : 35 dB 15 : 20 dB 31 : 36 dB
7:6	R/W	0x1	IOPAAFL ADCL OP AAF Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
5:4	R/W	0x1	IOPSDML1 ADCL OP SDM Bias Current Select1 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
3:2	R/W	0x1	IOPSDML2 ADCL OP SDM Bias Current Select2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
1:0	R/W	0x1	IOPMICL PGA OPMIC Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA

9.4.6.100. 0x0304 ADCR Analog Control Register(Default Value: 0x000C_0055)

Default:0x0304			Register Name: ADCR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MIC2AMPEN and ADCREN MIC2 Boost AMP Enable and ADCR Channel Enable 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	Dither Reset 0: New dither off 1: New dither on
28:20	/	/	/
19:18	R/W	0x3	PGA_CTRL_RCM PGA Common Mode Input Impedance Control for MIC-IN(The AC coupling capacitance of MIC-IN is 100nF. And the AC coupling capacitor combined with common-mode input resistor to form high-pass filter, the corresponding cut-off frequency is 20 Hz~80 Hz) 00 : 100 kΩ 01 : 75 kΩ 10 : 50 kΩ 11 : 25 kΩ
17:16	R/W	0x0	PGA_IN_VCM_CTRL High gain microphone input common mode voltage control(The field is the common-mode level control of MIC-IN when the gain is greater than or equal to 8 dB) 00 : 900 mV 01 : 800 mV 10 : 750 mV 11 : 700 mV
15:13	/	/	/
12:8	R/W	0x0	PGA_GAIN_CTRL PGA Gain Setting Control for MICIN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0 : 0 dB 16 : 21 dB 1 : 6 dB 17 : 22 dB 2 : 6 dB 18 : 23 dB 3 : 6 dB 19 : 24 dB 4 : 9 dB 20 : 25 dB 5 : 10 dB 21 : 26 dB 6 : 11 dB 22 : 27 dB 7 : 12 dB 23 : 28 dB 8 : 13 dB 24 : 29 dB 9 : 14 dB 25 : 30 dB 10 : 15 dB 26 : 31 dB 11 : 16 dB 27 : 32 dB 12 : 17 dB 28 : 33 dB 13 : 18 dB 29 : 34 dB 14 : 19 dB 30 : 35 dB 15 : 20 dB 31 : 36 dB
7:6	R/W	0x1	IOPAAFR ADCR OP AAF Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
5:4	R/W	0x1	IOPSDMR1 ADCR OP SDM Bias Current Select1 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
3:2	R/W	0x1	IOPSDMR2 ADCR OP SDM Bias Current Select2 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
1:0	R/W	0x1	IOPMICR PGA OPMIC Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA

9.4.6.101. 0x0310 DAC Analog Control Register(Default Value: 0x0015_0000)

Offset: 0x0310	Register Name: DAC_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from LINEOUTLP pin) 0: Normal 1: For Debug
30:28	R/W	0x0	HEADPHONE_GAIN 000: -0 dB 001: -6 dB 010: -12 dB 011: -18 dB 100: -24 dB 101: -30 dB 110: -36 dB 111: -42 dB
27:26	/	/	/
25:24	R/W	0x0	CPLDO_VOLTAGE 00: 0.9 V 01: 1.0 V 10: 1.1 V 11: 1.2 V
23:22	R/W	0x0	OPDRV_CUR. OPDRV output stage current setting 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
21:20	R/W	0x1	IOPVRS VRA2 Buffer OP Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
19:18	R/W	0x1	ILINEOUTAMPS LINEOUTL/R AMP Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
17:16	R/W	0x1	IOPDACS OPDAC Bias Current Select 00: 7 uA 01: 8 uA 10: 9 uA 11: 10 uA
15	R/W	0x0	DACLEN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			DACL Enable 0: Disable 1: Enable
14	R/W	0x0	DACREN DACR Enable 0: Disable 1: Enable
13	R/W	0x0	LINEOUTLEN Left Channel LINEOUT Enable 0: Disable 1: Enable
12	R/W	0x0	LMUTE DACL to Left Channel LINEOUT Mute Control 0: Mute 1: Not mute
11:7	/	/	/
6	R/W	0x0	LINEOUTLDIFFEN Left Channel LINEOUT Output Control 0: Single-End 1: Differential
5	/	/	/
4:0	R/W	0x0	LINEOUT Volume Control, Total 30 level from 0x1F to 0x02 with the volume 0dB to -43.5dB, -1.5dB/step, mute when 00000 & 00001.

9.4.6.102. 0x0318 MICBIAS Analog Control Register(Default Value: 0x4000_3030)

Offset:0x0318			Register Name: MICBIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x4	SELDETADCFS Select sample interval of the ADC sample 000: 2 ms … 100: 32 ms … 111: 256 ms
27:26	R/W	0x0	SELDETADCDB Select debounce time when jack removal 00: 128 ms 01: 256 ms 10: 512 ms 11: 1024 ms
25:24	R/W	0x0	SELDETADCBF Select the time to enable HBIAS before micadc work

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 2 ms 01: 4 ms 10: 8 ms 11: 16 ms
23	R/W	0x0	JACKDETEN Jack detect enable 0: Disable 1: Enable
22:21	R/W	0x0	SELDETADCDY Select the delay time to pull low the micdet when jack removal 00: 0.5 ms 01: 1 ms 10: 1.5 ms 11: 2 ms
20	R/W	0x0	MICADCEN Microphone detect ADC enable 0: Disable 1: Enable
19	R/W	0x0	POPFREE When this bit is 0, HBIAS MICADC is controlled by registor
18	R/W	0x0	Det Mode 0: Jack in pull low 1: Jack in pull high
17	R/W	0x0	AUTOPLEN Enable the function to auto pull low micdet when jack removal 0: Disable 1: Enable
16	R/W	0x0	MICDETPL When this bit is 1 and AUTOPLEN is 0, the micdet is pull to GND
15	R/W	0x0	HMICBIASEN Headphone Microphone Bias Enable 0: Disable 1: Enable
14:13	R/W	0x1	HBIASSEL HMICBIAS Voltage Level Select 00: 1.88 V 01: 2.09 V 10: 2.33 V 11: 2.55 V
12	R/W	0x1	HMIC BIAS chopper enable 0: Disable 1: Enable
11:10	R/W	0x0	HMICBIAS chopper clock select 00: 250 kHz 01: 500 kHz

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 1 MHz 11: 2 MHz
9:8	/	/	/
7	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIASSEL MMICBIAS Voltage Level Select 00: 1.88 V 01: 2.09 V 10: 2.33 V 11: 2.55 V
4	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
3:2	R/W	0x0	MMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1 MHz 11: 2 MHz
1:0	/	/	/

9.4.6.103. 0x0320 BIAS Analog Control Register(Default Value: 0x0000_0080)

Offset:0x0320			**Register Name: BIAS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x80	BIASDATA Bias Current Register Setting Data **Note: The register is not controlled by the audio codec module, but is controlled by system bus reset.**

9.4.6.104. 0x0324 Headphone Analog Control Register(Default Value: 0x8080_0C44)

Offset: 0x0324			**Register Name: HP_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x80	HPRCALIVERIFY Right Headphone calibration setting data
23:16	R/W	0x80	HPLCALIVERIFY Left Headphone calibration setting data
15	R/W	0x0	HPPA_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Right & Left Headphone PA Enable 0: Disable 1: Enable
14:12	/	/	/
11	R/W	0x1	HPINPUTENABLE When this bit is written to 0, the input stage of headphone disabled.
10	R/W	0x1	HPOUTPUTENABLE When this bit is written to 0, the output stage of headphone disabled.
9:8	R/W	0x0	HPPA_DEL Headphone delay time when start up 00: 4 ms 01: 8 ms 10: 16 ms 11: 32 ms
7:6	R/W	0x1	CP_CLKS Charge pump clock select 00: 250 kHz 01: 330 kHz 10: 400 kHz 11: 500 kHz
5	R/W	0x0	HPCALIMODE HEADPHONE calibration equilibration mode select 0: equilibration mode 1: no equilibration
4	R/W	0x0	HPCALIVERIFY HEADPHONE calibration in verify mode enable 0: Disable 1: Enable
3	R/W	0x0	HPCALIFIRST When this bit is written to 1, HEADPHONE calibrates once before enable
2:0	R/W	0x4	HPCALICKS HEADPHONE calibration clock frequency select 000: 4 … 100: 64 … 111: 512

9.4.6.105. 0x0328 HMIC Control Register(Default Value: 0x0000_0008)

Offset: 0x0328			**Register Name: HMIC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

22:21	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128 Hz 01: Down by 2, 64 Hz 10: Down by 4, 32 Hz 11: Down by 8, 16 Hz
20:16	R/W	0x0	MDATA_Threshold The threshold of MIC_DET pending When not setting HMIC_M, and the deviation between the current obtained value and the threshold exceeds MDATA_Threshold_Debounce at twice time, the interrupt is pending.
15:14	R/W	0x0	HMIC_SF HMIC Smooth Filter Setting The compare value of MIC interrupt is the value after Smooth Filter. 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
13:10	R/W	0x0	HMIC_M Debounce when the MIC Key down or up 0000: 1 samlpe data 0001: 2 samlpe data ... 1111: 16 samlpe data
9:6	R/W	0X0	HMIC_N Debounce when earphone plug in or pull out 125 ms~2 s 0000: 125 ms 0001: 250 ms … 1111: 2 s
5:3	R/W	0x1	MDATA_Threshold_Debounce 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5 110: 6 111: 7
2	R/W	0x0	JACK_OUT_IRQ_EN MIC Detect Interrupt Set 0: disable 1: enable
1	R/W	0x0	JACK_IN_IRQ_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			MIC Detect Interrupt Set 0: disable 1: enable
0	R/W	0x0	MIC_DET_IRQ_EN MIC Detect Interrupt Set 0: disable 1: enable

9.4.6.106. 0x032C HMIC Status Register(Default Value: 0x0000_6000)

Offset: 0x032C			Register Name: HMIC_STS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:13	R/W	0x3	MDATA_DISCARD After MIC DATA data receiving, the first N-data will be discarded. N defined as follows: 00: 0, None discarded 01: 1, 1-data discarded 10: 2, 2-data discarded 11: 4, 4-data discarded
12:8	R	0x0	HMIC_DATA HMIC Average Data
7:5	/	/	/
4	R/W1C	0x0	JACK_DET_OIRQ Jack output detect pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
3	R/W1C	0x0	JACK_DET_IIRQ Jack input detect pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
2:1	/	/	/
0	R/W1C	0x0	MIC_DET_ST. MIC Detect Pending interrupt 0: No pending IRQ 1: Pending IRQ Writing 1 clear pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 10 Interfaces....723
10.1. TWI....723
10.1.1. Overview....723
10.1.2. Block Diagram....723
10.1.3. Operations and Functional Descriptions....724
10.1.4. Programming Guidelines....728
10.1.5. Register List....732
10.1.6. Register Description....733
10.2. UART....744
10.2.1. Overview....744
10.2.2. Block Diagram....745
10.2.3. Operations and Functional Descriptions....745
10.2.4. Programming Guidelines....750
10.2.5. Register List....754
10.2.6. Register Description....755
10.3. SPI....771
10.3.1. Overview....771
10.3.2. Block Diagram....771
10.3.3. Operations and Functional Descriptions....772
10.3.4. Programming Guidelines....779
10.3.5. Register List....783
10.3.6. Register Description....784
10.4. USB2.0 OTG....800
10.4.1. Overview....800
10.4.2. Block Diagram....800
10.4.3. Operations and Functional Descriptions....801
10.5. USB2.0 Host Controller....803
10.5.1. Overview....803
10.5.2. Block Diagram....803
10.5.3. Operations and Functional Descriptions....804
10.5.4. USB Host Register List....804
10.5.6. OHCI Register Description....819
10.5.7. HCI Contgroller and PHY Interface Description....836
10.6. Port Controller....841
10.6.1. Overview....841
10.6.2. Block Diagram....841
10.6.3. Operations and Functional Descriptions....842
10.6.4. Register List....848
10.6.5. GPIO(PB,PC,PD,PE,PF,PG,PH) Register Description....850
10.6.6. GPIO(PL) Register Description....938

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.7. GPADC 950
10.7.1. Overview 950
10.7.2. Block Diagram 950
10.7.3. Operations and Functional Descriptions 951
10.7.4. Programming Guidelines 952
10.7.5. Register List 952
10.7.6. Register Description 953
10.8. LRADC 959
10.8.1. Overview 959
10.8.2. Block Diagram 959
10.8.3. Operations and Functional Descriptions 959
10.8.4. Programming Guidelines 961
10.8.5. Register List 961
10.9. CIR Receiver 965
10.9.1. Overview 965
10.9.2. Block Diagram 965
10.9.3. Operations and Functional Descriptions 966
10.10. CIR Transmitter 976
10.10.1. Overview 976
10.10.2. Block Diagram 976
10.10.3. Operations and Functional Descriptions 977
10.10.4. Programming Guidelines 980
10.10.5. Register List 980
10.10.6. Register Description 981
10.11. PWM 987
10.11.1. Overview 987
10.11.2. Block Diagram 987
10.11.3. Operations and Functional Descriptions 988
10.11.4. Working Mode 997
10.11.5. Register List 998
10.11.6. Register Description 998
10.12. LEDC 1017
10.12.1. Overview 1017
10.12.2. Block Diagram 1017
10.12.3. Operations and Functional Descriptions 1017
10.12.4. Programming Guidelines 1021
10.12.5. Register List 1025
10.12.6. Register Description 1025
10.13. EMAC 1034
10.13.1. Overview 1034
10.13.2. Block Diagram 1034
10.13.3. Operations and Functional Descriptions 1035
10.13.4. Register List 1041
10.13.5. Register Description 1042

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 10- 1. TWI Block Diagram 724
Figure 10- 2. 7-bit Standard Address Write Timing 725
Figure 10- 3. 7-bit Standard Address Read Timing 726
Figure 10- 4. 10-bit Extended Address Write Timing 726
Figure 10- 5. 10-bit Extended Address Read Timing 726
Figure 10- 6. TWI Programming State Diagram 727
Figure 10- 7. TWI Initialization Process 729
Figure 10- 8. TWI Write Data Process 730
Figure 10- 9. TWI Read Data Process 731
Figure 10- 10. TWI Driver Packet Transmission Process 732
Figure 10- 11. UART Block Diagram 745
Figure 10- 12. UART Application Diagram 746
Figure 10- 13. UART Serial Data Format 746
Figure 10- 14. RTS/CTS Autoflow Control Timing 747
Figure 10- 15. Serial IrDA Data Format 747
Figure 10- 16. RS-485 Timing 747
Figure 10- 17. Process of UART Transmitting/Receiving Data in Interrupt Mode 752
Figure 10- 18. Process of DMA Transmitting Data in DMA Mode 754
Figure 10- 19. SPI Block Diagram 771
Figure 10- 20. SPI Application Block Diagram 773
Figure 10- 21. SPI Phase 0 Timing Diagram 774
Figure 10- 22. SPI Phase 1 Timing Diagram 774
Figure 10- 23. SPI 3-Wire Mode 775
Figure 10- 24. SPI Dual-Input/Dual-Output Mode 776
Figure 10- 25. SPI Dual I/O Mode 776
Figure 10- 26. SPI Quad-Input/Quad-Output Mode 777
Figure 10- 27. SPI Write/Read Data in CPU Mode 781
Figure 10- 28. SPI Write/Read Data in DMA Mode 782
Figure 10- 29. USB2.0 OTG Controller Block Diagram 801
Figure 10- 30. USB2.0 OTG Controller and PHY Connection Diagram 802
Figure 10- 31. USB2.0 Host Controller Block Diagram 803
Figure 10- 32. USB2.0 HOST Controller and PHY Connection Diagram 804
Figure 10- 33. Port Controller Block Diagram 841
Figure 10- 34. Pull up/down Logic 847
Figure 10- 35. IO Buffer Strength Diagram 847
Figure 10- 36. GPADC Block Diagram 950
Figure 10- 37. GPADC Clock and Timing Requirement 952
Figure 10- 38. GPADC Initial Process 952
Figure 10- 39. LRADC Block Diagram 959
Figure 10- 40. LRADC Interrupt 960

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 10- 41. LRADC Initial Process 961
Figure 10- 42. CIR Receiver Block Diagram 965
Figure 10- 43. CIR Receiver Clock 966
Figure 10- 44. CIR Receiver Application Diagram 966
Figure 10- 45. NEC Protocol 967
Figure 10- 46. Logical '0' and Logical '1' of NEC Protocol 967
Figure 10- 47. ATHR Definition 968
Figure 10- 48. ITHR Definition 968
Figure 10- 49. NTHR Definition 968
Figure 10- 50. APAM Definition 969
Figure 10- 51. CIR Receiver Process 970
Figure 10- 52. CIR_TX Block Diagram 977
Figure 10- 53. CIR_TX Clock Description 978
Figure 10- 54. CIR One Bit Definition 978
Figure 10- 55. CIR Message Timing Diagram 979
Figure 10- 56. CIR Transmitter Process 980
Figure 10- 57. PWM Block Diagram 987
Figure 10- 58. PWM01 Clock Controller Diagram 988
Figure 10- 59. PWM01 Output Logic Module Diagram 989
Figure 10- 60. The Period and Duty-cycle of PWM0 High Level Active State 990
Figure 10- 61. The Period and Duty-cycle of PWM0 Low Level Active State 991
Figure 10- 62. The Phase of PWM0 High Level Active State 991
Figure 10- 63. PWM0 Output Waveform in Pulse Mode and Cycle Mode 992
Figure 10- 64. PWM01 Complementary Pair Output 992
Figure 10- 65. PWM01 Pair Waveform Before/After Insert Dead-time 993
Figure 10- 66. Group 0~3 PWM Signal Output 994
Figure 10- 67. PWM01 Capture Logic Module Diagram 995
Figure 10- 68. PWM0 Channel Capture Timing 996
Figure 10- 69. LEDC Block Diagram 1017
Figure 10- 70. LEDC Package Output Timing Diagram 1018
Figure 10- 71. LEDC 1-frame Output Timing Diagram 1018
Figure 10- 72. LEDC Input Data Structure 1019
Figure 10- 73. LEDC Typical Circuit 1019
Figure 10- 74. LEDC Data Input Code 1019
Figure 10- 75. LEDC Data Transfer Mode 1020
Figure 10- 76. LEDC Normal Configuration Process 1022
Figure 10- 77. LEDC Timeout Abnormal Processing Flow 1023
Figure 10- 78. FIFO Overflow Abnormal Processing Flow 1024
Figure 10- 79. EMAC Block Diagram 1035
Figure 10- 80. EMAC Typical Application 1037
Figure 10- 81. EMAC RX/TX Descriptor List 1037

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Tables

Table 10- 1. TWI External Signals 724
Table 10- 2. TWI Clock Sources 725
Table 10- 3. UART External Signals 745
Table 10- 4. UART Clock Sources 746
Table 10- 5. UART Mode Baud and Error Rates 748
Table 10- 6. IrDA Mode Baud and Error Rates 748
Table 10- 7. RS485 Mode Baud and Error Rates 749
Table 10- 8. SPI External Signals 772
Table 10- 9. SPI Clock Sources 773
Table 10- 10. SPI Transmit Format 774
Table 10- 11. SPI Old Sample Mode 778
Table 10- 12. SPI New Sample Mode 778
Table 10- 13. USB2.0 OTG External Signals 801
Table 10- 14. USB2.0 HOST External Signals 804
Table 10- 15. A133 Multi-function Port Table 842
Table 10- 16. PB Multiplex Function Select 842
Table 10- 17. PC Multiplex Function Select 842
Table 10- 18. PD Multiplex Function Select 843
Table 10- 19. PE Multiplex Function Select 844
Table 10- 20. PF Multiplex Function Select 844
Table 10- 21. PG Multiplex Function Select 844
Table 10- 22. PH Multiplex Function Select 845
Table 10- 23. PL Multiplex Function Select 845
Table 10- 24. Port Function 846
Table 10- 25. GPADC External Signals 951
Table 10- 26. GPADC Clock Sources 951
Table 10- 27. LRADC External Signals 960
Table 10- 28. LRADC Clock Sources 960
Table 10- 29. CIR Receiver External Signals 966
Table 10- 30. CIR_TX External Signals 977
Table 10- 31. PWM External Signals 988
Table 10- 32. LEDC External Signals 1018
Table 10- 33. LEDC Clock Sources 1018
Table 10- 34. EMAC Pin Mapping 1035
Table 10- 35. EMAC RGMII Pin List 1036
Table 10- 36. EMAC RMII Pin List 1036
Table 10- 37. EMAC Clock Characteristics 1036

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 10 Interfaces

10.1. TWI

10.1.1. Overview

The TWI is designed as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including slave and master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. The TWI can be operated in standard mode (100 kbit/s) or fast-mode (400 kbit/s). The 10-bit addressing mode is supported for this specified application. General call addressing is also supported in slave mode.

The TWI has the following features:

- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speed up to 400 kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in master mode

10.1.2. Block Diagram

Figure 10-1 shows the block diagram of TWI.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

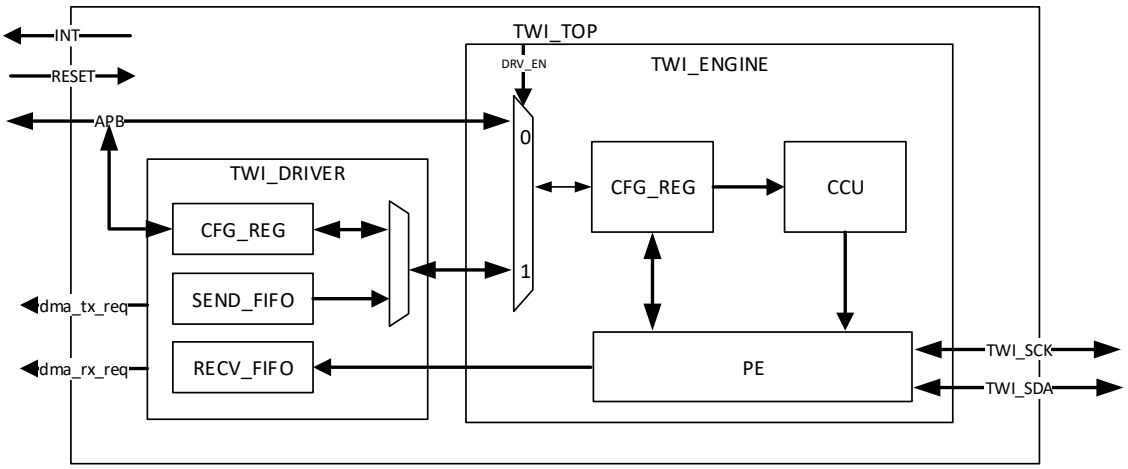


Figure 10- 1. TWI Block Diagram

RESET: Module reset signal
INT: Module output interrupt signal
CFG_REG: Module configuration register in TWI
PE: Packet encoding/decoding
CCU: Module clock controller unit

10.1.3. Operations and Functional Descriptions

10.1.3.1. External Signals

The TWI controller has 5 TWIs. Table 10-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O, when TWI is configured as master device, TWI_SCK is output pin; when TWI is configurable as slave device, TWI_SCK is input pin. The unused TWI ports are used as General Purpose I/O ports. For information about General Purpose I/O ports, see **Port Controller** in chapter10.

Table 10- 1. TWI External Signals

Signal	Description	Type
TWI0_SCK	TWI0 Clock Signal	I/O,OD
TWI0_SDA	TWI0 Serial Data	I/O,OD
TWI1_SCK	TWI1 Clock Signal	I/O,OD
TWI1_SDA	TWI1 Serial Data	I/O,OD
TWI2_SCK	TWI2 Clock Signal	I/O,OD
TWI2_SDA	TWI2 Serial Data	I/O,OD
TWI3_SCK	TWI3 Clock Signal	I/O,OD
TWI3_SDA	TWI3 Serial Data	I/O,OD
S_TWI0_SCK	S_TWI0 Clock Signal	I/O,OD
S_TWI0_SDA	S_TWI0 Serial Data	I/O,OD
S_TWI1_SCK	S_TWI1 Clock Signal	I/O,OD

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

S_TWI1_SDA	S_TWI1 Serial Data	I/O,OD

10.1.3.2. Clock Sources

Each TWI controller has a fixed clock source. Table 10-2 describes the clock source for TWI. Users can see **Clock Controller Unit(CCU)** in chapter3 for clock setting, configuration and gating information.

Table 10- 2. TWI Clock Sources

Clock Sources	Description
APB2_CLK	TWI0/1/2/3 clock source, for details on APB2 refer to CCU

After selected a proper clock, for using the TWI0/1/2/3, user must enable the gating of TWI and release the reset bit.

10.1.3.3. Write/Read Timing in Standard and Extended Address Mode

Figure 10-2 describes the write timing in 7-bit standard address mode.

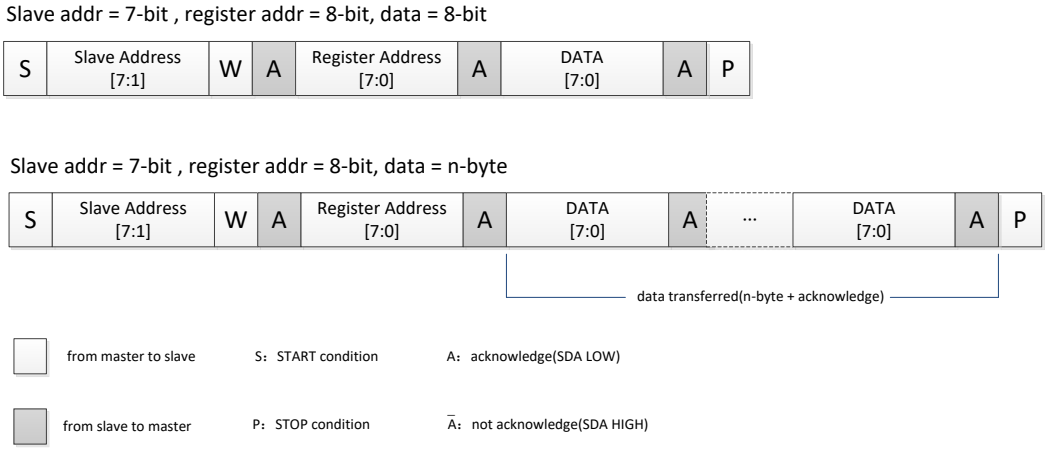
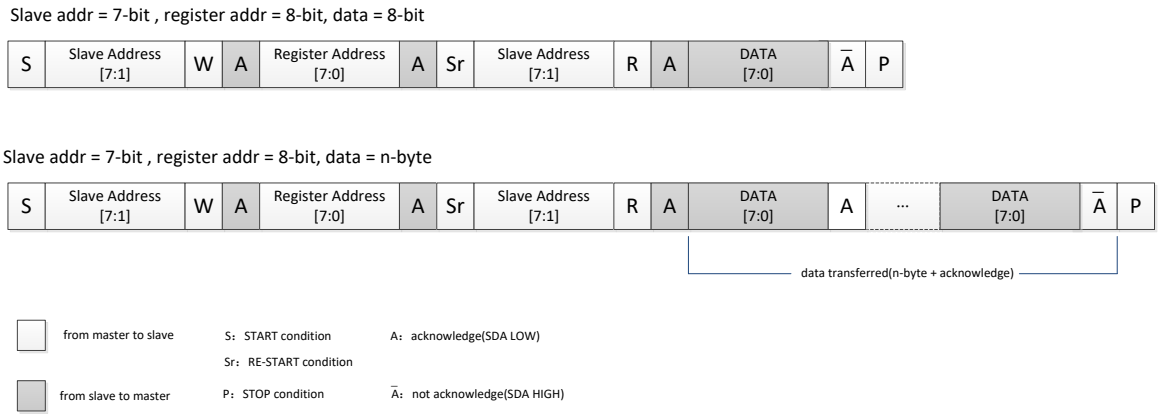


Figure 10- 2. 7-bit Standard Address Write Timing

Figure 10-3 describes the read timing in 7-bit standard address mode.



 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 10- 3. 7-bit Standard Address Read Timing

Figure 10-4 describes the write timing in 10-bit extended address mode.

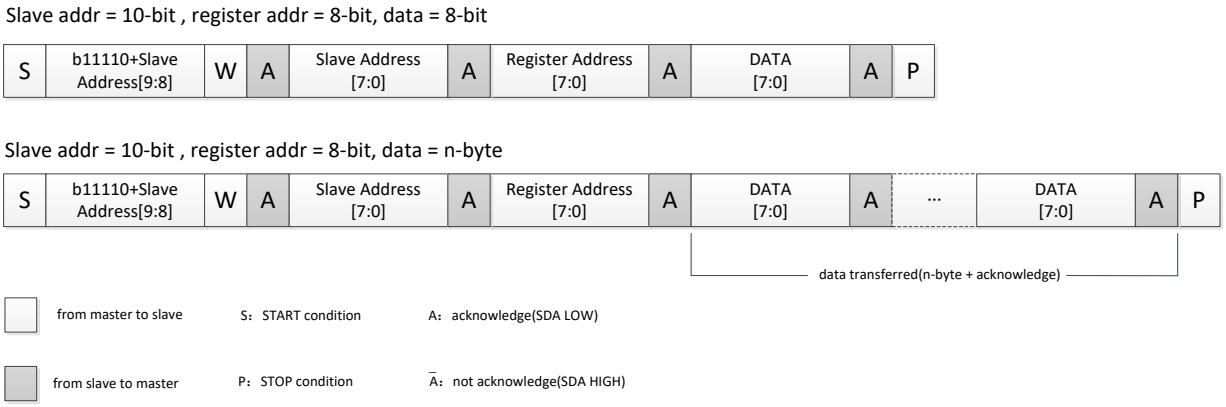


Figure 10- 4. 10-bit Extended Address Write Timing

Figure 10-5 describes the read timing in 10-bit extended address mode.

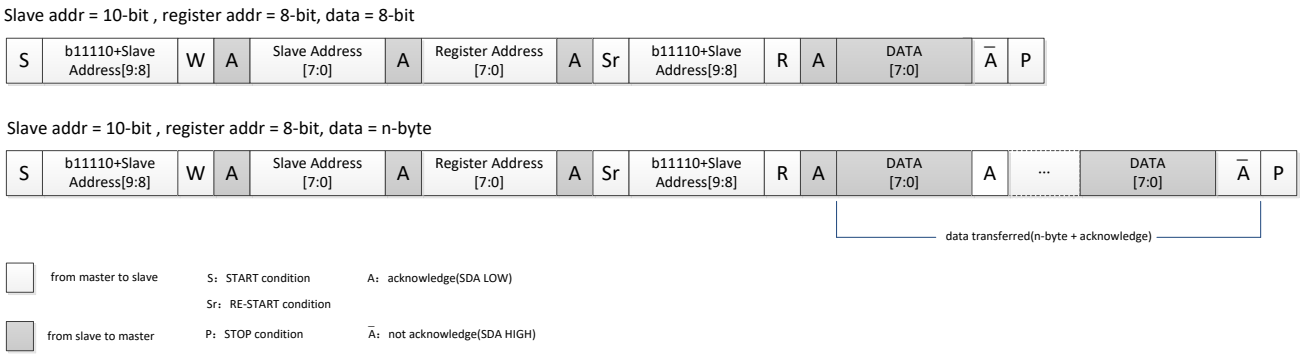


Figure 10- 5. 10-bit Extended Address Read Timing

10.1.3.4. Programming State Diagram

Figure 10-6 shows the TWI programming state diagram. For the value between two states, see TWI_STAT register in section 10.1.6.5.

M_SEND_S: master sends START signal;

M_SEND_ADDR: master sends slave address;

M_SEND_XADD: master sends slave extended address;

M_SEND_SR: master repeated start;

M_SEND_DATA: master sends data;

M_SEND_P: master sends STOP signal;

M_RECV_DATA: master receives data;

ARB_LOST: Arbitration lost;

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

C_IDLE: Idle;

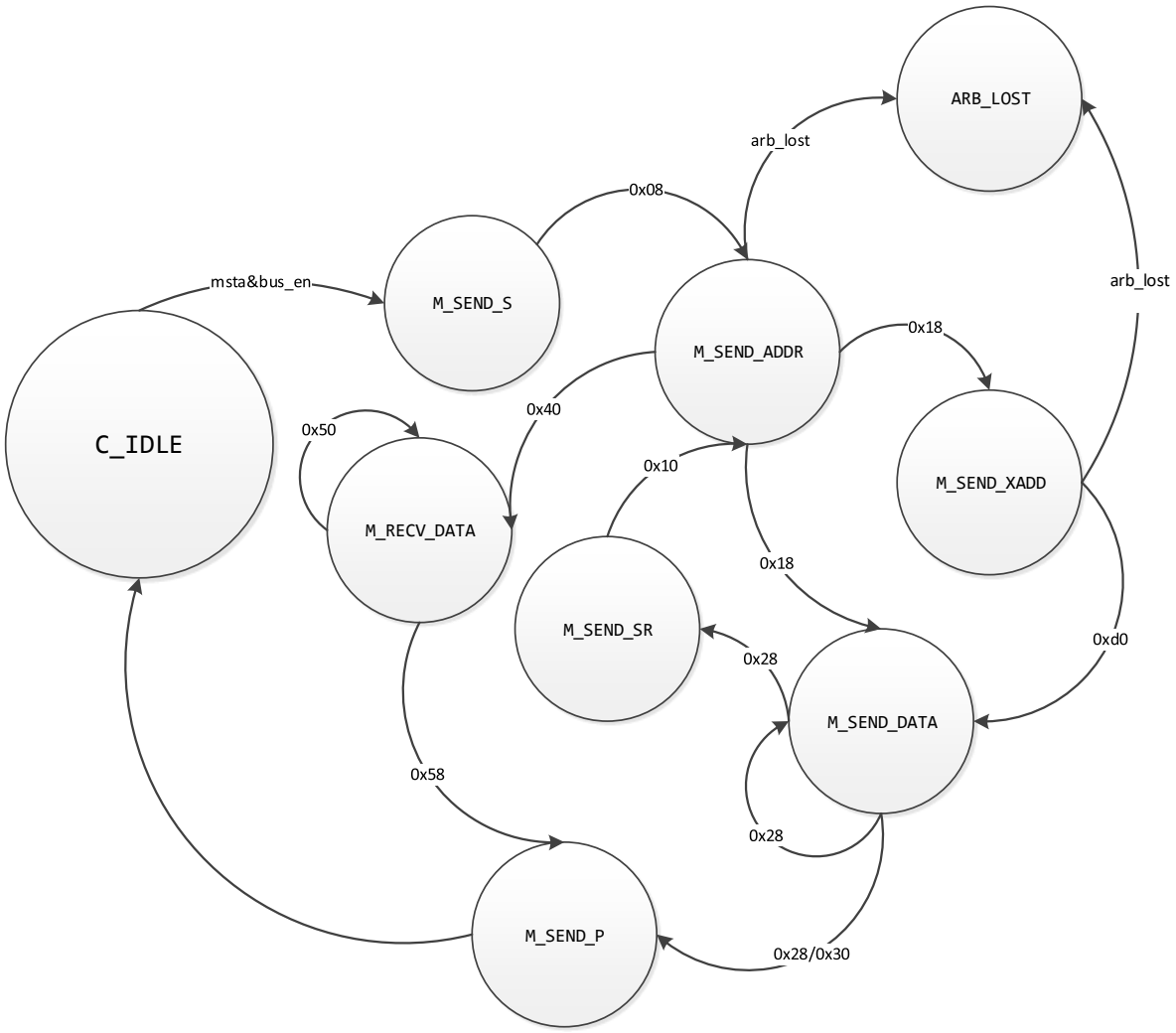


Figure 10- 6. TWI Programming State Diagram

10.1.3.5. TWI Engine Master and Slave Mode

There are four operation modes on the TWI bus. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI engine by writing command and data to its registers. TWI engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP command is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit of the TWI_CNTR register to high (before it must be low). The TWI engine will assert INT line and INT_FLAG to indicate a completion for the START command and each consequent byte transfer. At each interrupt, the micro-processor needs to check the TWI_STAT register for current status. A transfer has to be concluded with STOP command by setting M_STP bit to high.

In Slave mode, the TWI engine also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

the CPU host should read the status, read/write TWI_DATA data register, and set the TWI_CNTR control register. After each byte transfer, a slave device always stop the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START command.

10.1.4. Programming Guidelines

The TWI controller operates in 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller will sent a start condition. When in the addressing formats of 7-bit, TWI sends out one 8 bits message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, see the register description in Section 10.1.6.1 and 10.1.6.2.

10.1.4.1. Initialization

To initialize the TWI, perform the following steps:

Step1 Configure corresponding GPIO multiplex function as TWI mode.

Step2 For TWIx, set TWI_BGR_REG[TWIx_GATING] in CCU module to 0 to close TWIx clock;

Step3 For TWIx, set TWI_BGR_REG[TWIx_RST] in CCU module to 0, then set to 1 to reset TWIx;

Step4 For TWIx, set TWI_BGR_REG[TWIx_GATING] in CCU module to 1 to open TWIx clock;

Step5 Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate(The clock source of TWI is from APB2).

Step6 Configure TWI_CNTR[BUS_EN] and TWI_CNTR[A_ACK], when using interrupt, set TWI_CNTR[BUS_EN] to 1, and register system interrupt through GIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

Figure 10-7 shows the process of TWI initialization.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

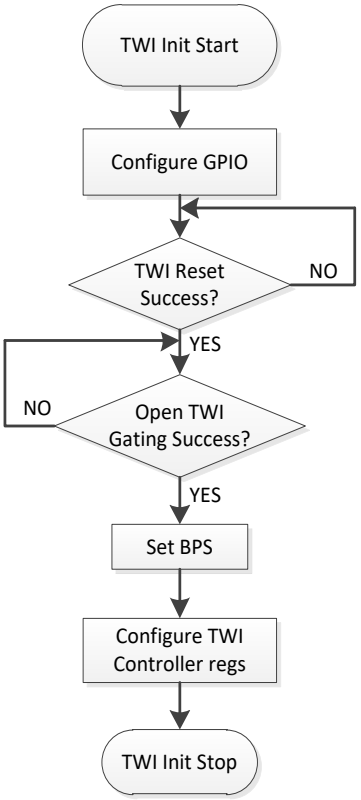


Figure 10- 7. TWI Initialization Process

10.1.4.2. Data Write Operation

To write data to device, perform the following steps:

Step1 Clear TWI_EFR register, and configure TWI_CNTR[M_STA] to 1 to transmit START signal.

Step2 After START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA(For 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step3 Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA(For 16-bit address, firstly write the first byte address, secondly write the second byte address).

Step4 Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA(For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).

Step5 After transmission completes, write TWI_CNTR[M_STP] to 1 to transmit STOP signal and end this write-operation.

Figure 10-8 shows the process of TWI write to device.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

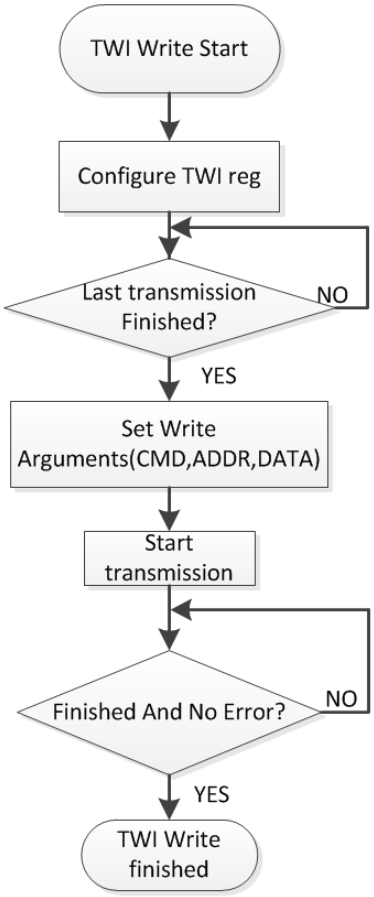


Figure 10- 8. TWI Write Data Process

10.1.4.3. Data Read Operation

To read data from device, perform the following steps:

Step1 Clear TWI_EFR register, set TWI_CNTR[A_ACK] to 1, and configure TWI_CNTR[M_STA] to 1 to transmit START signal.

Step2 After START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA(For 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step3 Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA(For 16-bit address, firstly write the first byte address, secondly write the second byte address).

Step4 Interrupt is triggered after data address transmission completes, write TWI_CNTR[M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.

Step5 After device address transmission completes, each receive completion will trigger interrupt, in turn, read TWI_DATA to get data, when receiving the previous interrupt of the last byte data, clear TWI_CNTR[A_ACK] to stop acknowledge signal of the last byte.

Step6 Write TWI_CNTR[M_STP] to 1 to transmit STOP signal and end this read-operation.

Figure 10-9 shows the process of TWI read from device.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

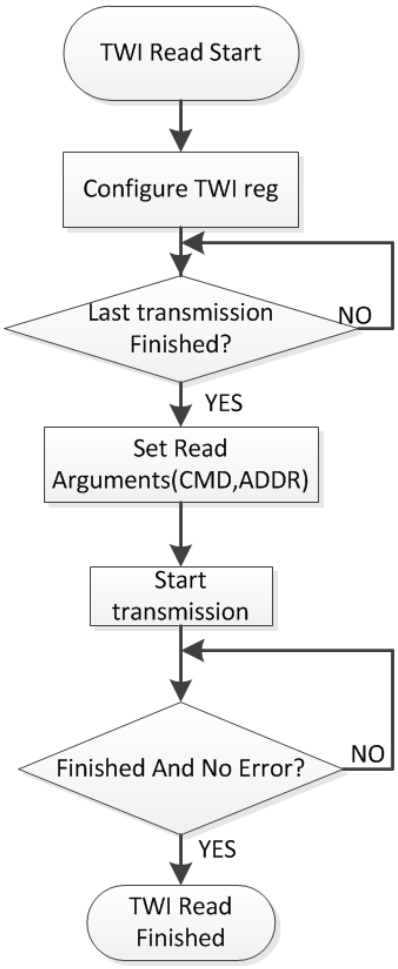


Figure 10- 9. TWI Read Data Process

10.1.4.4. Packet Transmission Operation

Figure 10-10 shows a software operation flow for packet transmission by TWI driver.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

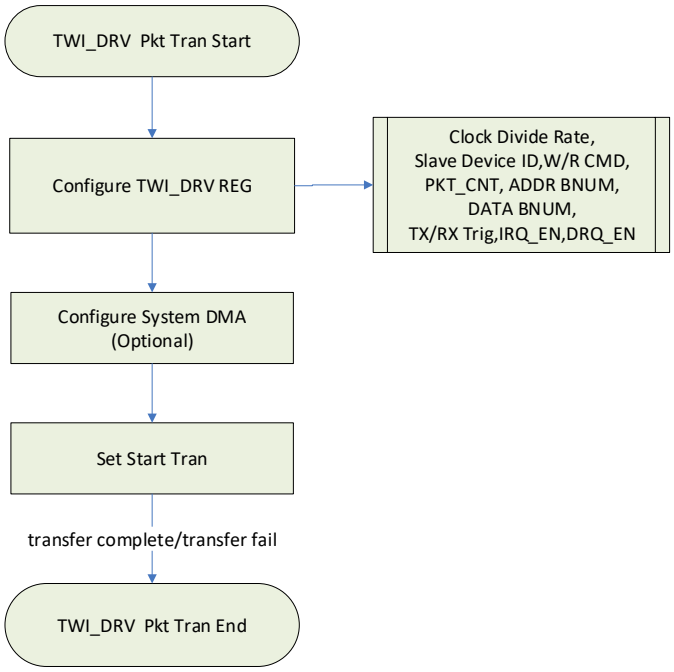


Figure 10- 10. TWI Driver Packet Transmission Process

10.1.5. Register List

Module Name	Base Address
TWI0	0x05002000
TWI1	0x05002400
TWI2	0x05002800
TWI3	0x05002C00
R_TWI0	0x07081400
R_TWI1	0x07081800

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address
TWI_XADDR	0x0004	TWI Extended Slave Address
TWI_DATA	0x0008	TWI Data Byte
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

10.1.6. Register Description

10.1.6.1. 0x0000 TWI Slave Address Register(Default Value:0x0000_0000)

Offset: 0x0000			**Register Name: TWI_ADDR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address 7-bit addressing: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.1.6.2. 0x0004 TWI Extend Address Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

10.1.6.3. 0x0008 TWI Data Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

10.1.6.4. 0x000C TWI Control Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus ISDA/ISCL is ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. **Note: In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to '1', TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE 0: scl clock high period count on oscl 1: scl clock high period count on iscl

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.1.6.5. 0x0010 TWI Status Register(Default Value:0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.1.6.6. 0x0014 TWI Clock Register(Default Value:0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x1	CLK_DUTY Setting duty cycle of clock as Master 0: 50% 1: 40%
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For example: Fin = 24 MHz (APB clock input) For 400 kHz full speed 2Wire, CLK_N = 1, CLK_M=2 F0 = 24 MHz/2^1=12 MHz, F1= F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2Wire, CLK_N=1, CLK_M=11 F0=24 MHz/2^1=12 MHz, F1=F0/(10*(11+1)) = 0.1 MHz

10.1.6.7. 0x0018 TWI Soft Reset Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

10.1.6.8. 0x001C TWI Enhance Feature Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1:0	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00 : No data byte can be written after read command 01 : Only 1 byte data can be written after read command 10 : 2 bytes data can be written after read command 11 : 3 bytes data can be written after read command

10.1.6.9. 0x0020 TWI Line Control Register(Default Value:0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0 : Low 1 : High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0 : Low 1 : High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When line control mode is enabled (bit[2] set), this bit decides the output level of TWI_SCL. 0 : Output low level 1 : Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0 : Disable TWI_SCL line control mode 1 : Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When line control mode is enabled (bit[0] set), this bit decides the output level of TWI_SDA. 0 : Output low level 1 : Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0 : Disable TWI_SDA line control mode 1 : Enable TWI_SDA line control mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.1.6.10. 0x0200 TWI_DRV Control Register(Default Value:0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	START_TRAN 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. All format setting and data will be loaded from registers and FIFO when transmission start.
30	/	/	/
29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the TWI_DRV action after sending register address.
28	R/W	0x0	READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W **Setting this bit to 1 if reading from a slave which register width is equal to 0**.
27:24	R	0x0	TRAN_RESULT 0000: OK 0001: FAIL Other: Reserved
23:16	R	0xf8	TWI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:8	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device does not response after **N*F$_{SCL}$** cycles. And software must do a reset to TWI_DRV module and send a stop condition to slave.
7:2	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	SOFT_RESET 0: normal 1: reset
0	R/W	0x0	TWI_DRV_EN 0: Module disable 1: Module enable (only use in TWI Master Mode)

10.1.6.11. 0x0204 TWI_DRV Transmission Configuration Register(Default Value:0x0000_0001)

Offset: 0x0204			Register Name: TWI_DRV_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format.

10.1.6.12. 0x0208 TWI_DRV Slave ID Register(Default Value:0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID • 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 • 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: write 1: read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0], low 8 bits for slave device ID with 10-bit addressing

10.1.6.13. 0x020C TWI_DRV Packet Format Register(Default Value:0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0~255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~65535

10.1.6.14. 0x0210 TWI_DRV Bus Control Register(Default Value:0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	W	0x0	CLK_COUNT_MODE 0: scl clock high period count on oscl 1: scl clock high period count on iscl
15	R/W	0x1	CLK_DUTY Setting duty cycle of Clock as Master 0: 50% 1: 40%
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10 Specially,Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

10.1.6.15. 0x0214 TWI_DRV Interrupt Control Register(Default Value:0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19	R/W	0x0	RX_REQ_INT_EN
18	R/W	0x0	TX_REQ_INT_EN
17	R/W	0x0	TRAN_ERR_INT_EN
16	R/W	0x0	TRAN_COM_INT_EN
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failed pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completed pending

10.1.6.16. 0x0218 TWI_DRV DMA Configure Register(Default Value:0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG When DMA_RX_EN is set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG or Read Packet Transmission completed with RECV_FIFO not empty.
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN
7:6	/	/	/
5:0	R/W	0x10	TX_TRIG When DMA_TX_EN set, send DMA TX Req when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO.

10.1.6.17. 0x021C TWI_DRV FIFO Content Register(Default Value:0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit is cleared automatically.
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit is cleared automatically.
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

10.1.6.18. 0x0300 TWI_DRV Send Data FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO, which stores reg address and data sending to slave device.

10.1.6.19. 0x0304 TWI_DRV Receive Data FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO, which stores data received from slave device

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2. UART

10.2.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in system where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART has the following features:

- Two separate FIFOs: RX FIFO and TX FIFO
  - Each of them is 64 bytes (For UART0, UART3, UART4, and S_UART)
  - Each of them is 256 bytes (For UART1 and UART2)
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s with 64 MHz APB clock, and speed up to 1.5 Mbit/s with 24 MHz APB clock
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2.2. Block Diagram

Figure 10-11 shows a block diagram of the UART.

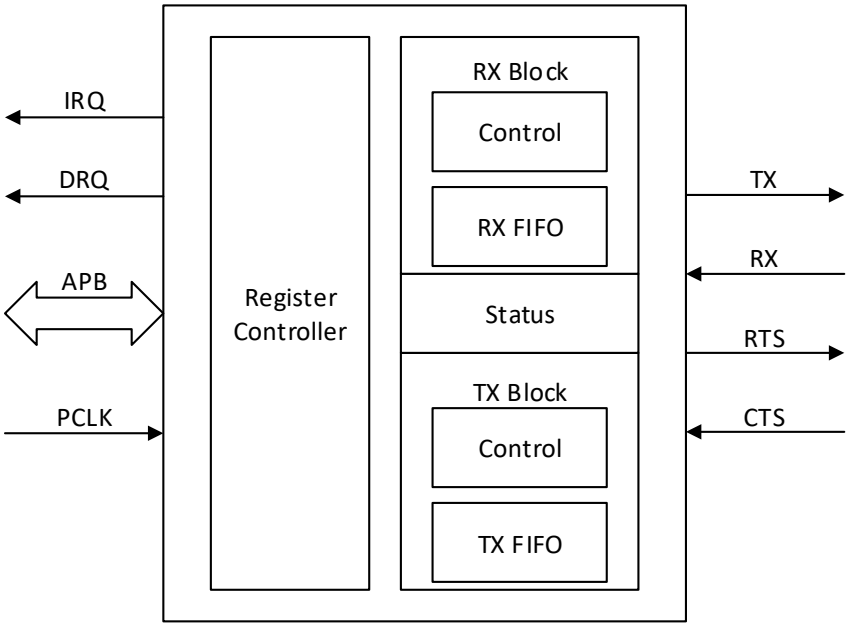


Figure 10- 11. UART Block Diagram

10.2.3. Operations and Functional Descriptions

10.2.3.1. External Signals

Table 10-3 describes the external signals of UART.

Table 10- 3. UART External Signals

Signal	Type	Description
UART0_TX	O	UART0 Data Transmit
UART0_RX	I	UART0 Data Receive
UART1_TX	O	UART1 Data Transmit
UART1_RX	I	UART1 Data Receive
UART1_CTS	I	UART1 Data Clear to Send
UART1_RTS	O	UART1 Data Request to Send
UART2_TX	O	UART2 Data Transmit
UART2_RX	I	UART2 Data Receive
UART2_CTS	I	UART2 Data Clear to Send
UART2_RTS	O	UART2 Data Request to Send
UART3_TX	O	UART3 Data Transmit
UART3_RX	I	UART3 Data Receive
UART3_CTS	I	UART3 Data Clear to Send

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

UART3_RTS	O	UART3 Data Request to Send
UART4_TX	O	UART4 Data Transmit
UART4_RX	I	UART4 Data Receive
UART4_CTS	I	UART4 Data Clear to Send
UART4_RTS	O	UART4 Data Request to Send
S_UART_TX	O	S_UART Data Transmit
S_UART_RX	I	S_UART Data Receive

10.2.3.2. Clock Sources

Table 10-4 describes the clock sources of UART.

Table 10- 4. UART Clock Sources

Clock Sources	Description
APB2_CLK	Clock of APB2

10.2.3.3. Typical Application

Figure 10-12 shows the application block diagram of UART.

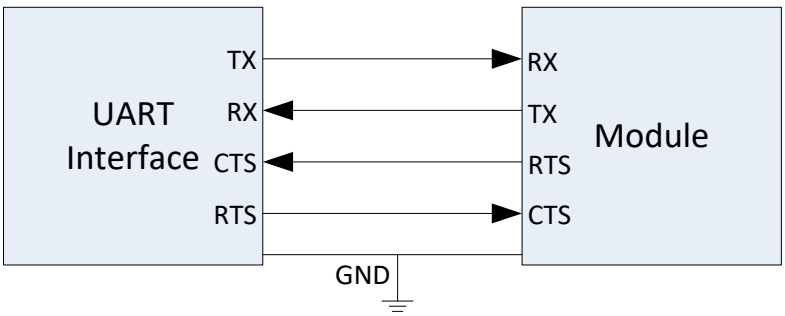


Figure 10- 12. UART Application Diagram

10.2.3.4. UART Timing Diagram

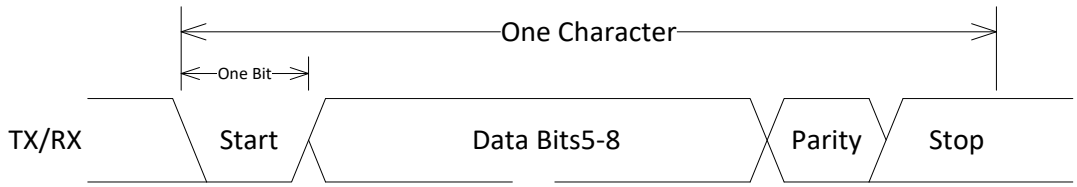


Figure 10- 13. UART Serial Data Format

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

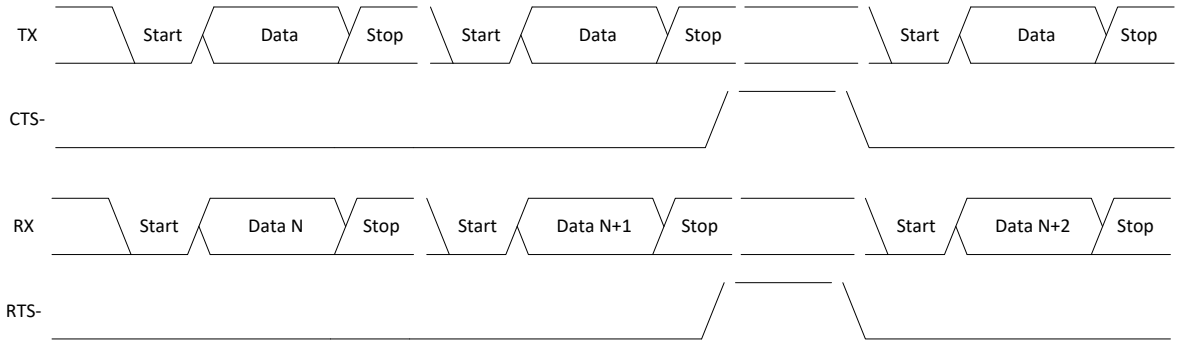


Figure 10- 14. RTS/CTS Autoflow Control Timing

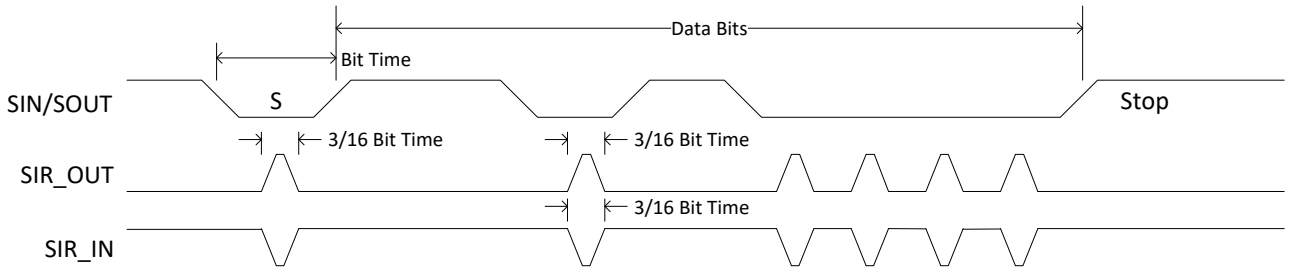


Figure 10- 15. Serial IrDA Data Format

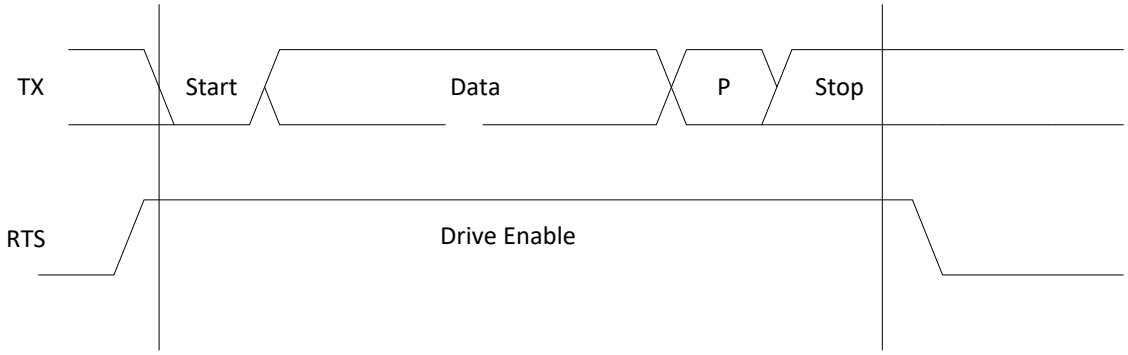


Figure 10- 16. RS-485 Timing

10.2.3.5. UART Operating Mode

10.2.3.5.1. Basic Mode Setting

The **UART_LCR** register can set basic parameter of a data frame: data width(5 to 8 bits), stop bit number(1/1.5/2), parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit and stop signal. The LSB is transmitted first.

- Start signal(start bit): It is the start flag of a data frame. According to UART protocol, the low level of TXD signal indicates the start of a data frame. When the UART transmits data, the level need hold high.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- Data signal(data bit): The data bit width can be configured as 5-bit,6-bit,7-bit,8-bit through different applications.
- Parity bit: It is 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the **UART_LCR** register.
- Stop Signal(stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit,1.5-bit and 2-bit by the **UART_LCR** register. The high level of TXD signal indicates the end of a data frame.

10.2.3.5.2. Baud Rate Setting

The baud rate is calculated as follows: Baud rate = SCLK /(16 * divisor). SCLK is usually APB2 and can be set in CCU. Divisor is frequency divider of UART. The frequency divider has 16-bit, the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.
The relationship between different UART mode and error rate is as follows.

Table 10- 5. UART Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Over sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
64000000	7	576000	16	-0.794
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
64000000	1	4000000	16	0

Table 10- 6. IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 10- 7. RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16

10.2.3.5.3. DLAB Setting

DLAB control bit (**UART_LCR[7]**) is the access control bit of divisor Latch register.
If DLAB is 0, then 0x00 offset address is **TX/RX FIFO** register, 0x04 offset address is **IER** register.
If DLAB is 1, then 0x00 offset address is **DLL** register, 0x04 offset address is **DLH** register.
When UART initial, divisor need be set. That is, writing 1 to DLAB can access the **DLL** and **DLH** register, after finished setting, writing 0 to DLAB can access the **TX/RX FIFO** register.

10.2.3.5.4. CHCFG_AT_BUSY Setting

The function of **CHCFG_AT_BUSY**(UART_HALT[1]) and **CHANGE_UPDATE**(UART_HALT[2]) are as follows.
CHCFG_AT_BUSY(configure at busy): Enable the bit, software can also set UART controller when UART is busy, such as the LCR,DLH,DLL register.
CHANGE_UPDATE(update configuration): If **CHCFG_AT_BUSY** is enabled, and **CHANGE_UPDATE** is written to 1, the configuration of UART controller can be updated. After completed update, the bit is cleared to 0 automatically.

Setting divisor, performs the following steps:
Step1 Write 1 to **CHCFG_AT_BUSY** to enable “configure at busy”.
Step2 Write 1 to **DLAB** , and set **DLH** and **DLL**.
Step3 Write 1 to **CHANGE_UPDATE** to update configuration. The bit is cleared to 0 automatically after completed update.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2.3.5.5. UART Busy

UART_USR[0] is a busy flag of UART controller or not.
When TX transmits data, or RX receives data, or TX FIFO is not empty, or RX FIFO is not empty, then the BUSY flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

10.2.4. Programming Guidelines

10.2.4.1. Initialization

Step1 System Initialization

- Configure APB2_CFG_REG in CCU module to set APB2 bus clock(The clock is 24MHz by default).
- Set UART_BGR_REG[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG[UARTx_RST] to 1 to de-assert the module.

Step2 UART Controller Initialization

- IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode(For detail, see the description in Port Controller).
- Baud-rate configuration:
  - Set UART baud-rate(refer to section 10.2.3.5.2);
  - Write UART_FCR[FIFOE] to 1 to enable TX/RX FIFO;
  - Write UART_HALT[HALT_TX] to 1 to disable TX transfer;
  - Set UART_LCR[DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to UART_DLL register, set 0x04 offset address to UART_DLH register;
  - Write the high 8-bit of divisor to UART_DLH, and write the low 8-bit of divisor to UART_DLL;
  - Set UART_LCR[DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to UART_RBR/UART_THR register, set 0x04 offset address to UART_IER register;
  - Set UART_HALT[HALT_TX] to 0 to enable TX transfer.

Step3 Controller Parameter Configuration

- Set data width, stop bits and even/odd parity type by writing UART_LCR register.
- Reset, enable FIFO and set FIFO trigger condition by writing UART_FCR register.
- Set flow control parameter by writing UART_MCR register.

Step4 Interrupt Configuration

- Configure UART interrupt vector number to request UART interrupt(please refer to GIC module for interrupt vector number).
- In DMA mode, write UART_IER to 0 to disable interrupt; write UART_HSK[Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR[DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
- In Interrupt mode, configure UART_IER to enable corresponding interrupt according to requirements: such as transmit(TX) interrupt, receive(RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX interrupt is usually used).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2.4.2. Data Transfer/Receive in Query Mode

Data transfer

Step1 Write data to UART_THR to start data transfer.

Step2 Check TX_FIFO status by reading UART_USR[TFNF]. If the bit is 1, data can continue to be written; if the bit is 0, wait data transfer, and data cannot continue to write until FIFO is not full.

Data receive

Step1 Check RX_FIFO status by reading UART_USR[RFNE].

Step2 Read data from UART_RBR if RX_FIFO is not empty.

Step3 If UART_USR[RFNE] is 0, data is received completely.

10.2.4.3. Data Transfer/Receive in Interrupt Mode

Data transfer

Step1 Set UART_IER[ETBEI] to 1 to enable UART transfer interrupt.

Step2 Write data to be transmitted to UART_THR.

Step3 When the data of TX_FIFO meets trigger condition(such as FIFO/2, FIFO/4), UART transfer interrupt is generated.

Step4 Check UART_USR[TFE] and determine whether TX_FIFO is empty. If UART_USR[TFE] is 1, it indicates that the data in TX_FIFO is transmitted completely.

Step5 Clear UART_IER[ETBEI] to 0 to disable transfer interrupt.

Data receive

Step1 Set UART_IER[ERBFI] to 1 to enable UART receive interrupt.

Step2 When the received data from RX_FIFO meets trigger condition(such as FIFO/2, FIFO/4), UART receive interrupt is generated.

Step3 Read data from UART_RBR.

Step4 Check RX_FIFO status by reading UART_USR[RFNE] and determine whether to read data. If the bit is 1, continue to read data from UART_RBR until UART_USR[RFNE] is cleared to 0, which indicates data is received completely.

Figure 10-17 shows the process of UART transmitting and receiving data in interrupt mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

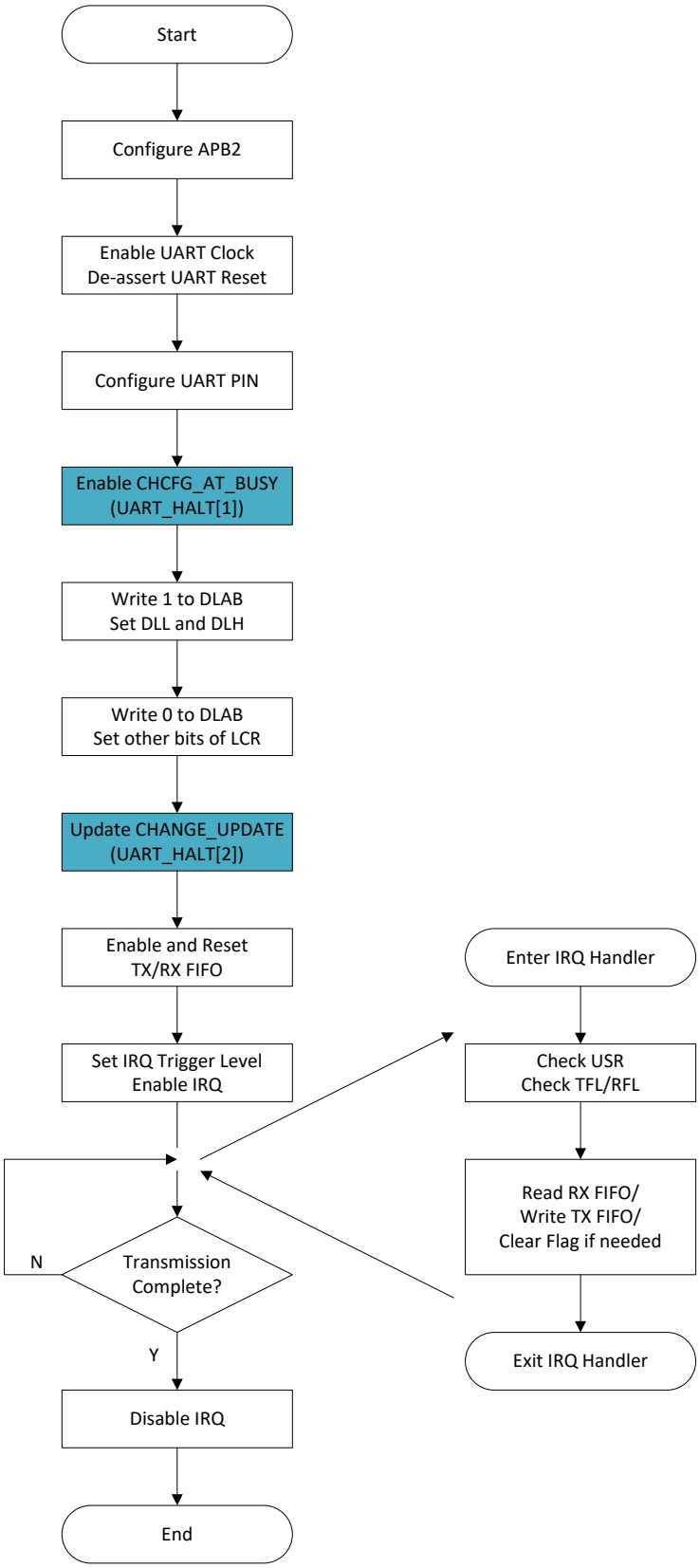


Figure 10- 17. Process of UART Transmitting/Receiving Data in Interrupt Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2.4.4. Data Transfer/Receive in DMA Mode

Data transfer

Step1 Configure UART DMA interrupt according to initialization process.

Step2 Configure DMA data channel, including transfer source address, transfer destination address, number of data to be transferred, and transfer type, etc(For details, see the description in DMAC module).

Step3 Enable DMA transfer function of the UART by setting the register of DMA module.

Step4 Determine whether UART data is transferred completely based on DMA status. If all data is transferred completely, disable DMA transfer function of the UART.

Data receive

Step1 Configure DMA data channel, including transfer source address, transfer destination address, number of data to be transferred, and transfer type, etc(For details, see the description in DMAC module).

Step2 Enable DMA receive function of the UART by setting the register of DMA module.

Step3 Determine whether UART data is received completely based on DMA status. If all data is received completely, disable DMA receive function of the UART.

Figure 10-18 shows the process of UART transmitting data in DMA mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

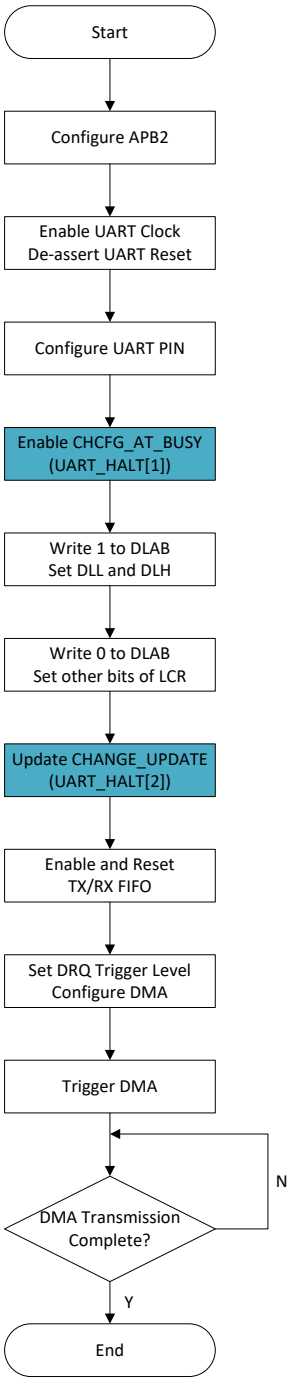


Figure 10- 18. Process of DMA Transmitting Data in DMA Mode

10.2.5. Register List

Module Name	Base Address
UART0	0x05000000
UART1	0x05000400
UART2	0x05000800

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

UART3	0x05000C00
UART4	0x05001000
R_UART	0x07080000

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register

10.2.6. Register Description

10.2.6.1. 0x0000 UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register can not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			overrun error occurs.

10.2.6.2. 0x0000 UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data is transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters data may be written to the THR before the FIFO is full. When the FIFO is full, any write data results in the write data being lost.

10.2.6.3. 0x0000 UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) are set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.4. 0x0004 UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) is set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.5. 0x0004 UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: UART_IER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupt. 0: Disable 1: Enable

10.2.6.6. 0x0008 UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011: RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout The bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/framing errors or break interrupt	Reading the line status register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE mode disabled) or XMIT FIFO at or below threshold (Program THRE mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

10.2.6.7. 0x0008 UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: UART_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO when the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TX Empty Trigger This is used to select the empty threshold level when the THRE Interrupts are generated and the mode is active. It also determines when the dma_tx_req_n signal is asserted in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enabled, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the rx drq will send when RFL is equal to or more than FIFO Trigger Level. 1: Mode 1 In this mode, if TX FIFO is enabled and the PTE is high, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level, the rx drq will be set to 1, in otherwise, it will be set to 0.
2	W	0x0	XFIFOR XMIT FIFO Reset The bit resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset The bit resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs The bit enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs is reset.

10.2.6.8. 0x000C UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x000C	Register Name: UART_LCR

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If setting to 0, the serial output is forced to the spacing (logic 0) state. When not in Loopback mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE is enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable/readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9^{th} bit--address bit. 11:9^{th} bit = 0, indicates that this is a data byte. 10:9^{th} bit = 1, indicates that this is an address byte. **Note: When using this function, PEN(LCR[3]) must set to 1.**
3	R/W	0x0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If setting to 0, one stop bit is

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			transmitted in the serial data. If setting to 1 and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

10.2.6.9. 0x0010 UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00: UART Mode 01: IrDA SIR Mode 10: RS485 Mode 11: Reserved
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control mode disabled 1: Auto Flow Control mode enabled
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] is set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] is set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The RTS (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] is set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] is set to one) and FIFOs enable (FCR[0] is set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] is set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] is set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

10.2.6.10. 0x0014 UART Line Status Register(Default Value: 0x0000_0060)

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to “1” when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided, there are no subsequent errors in the FIFO.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

10.2.6.11. 0x0018 UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			(dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] is set to 1), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. **Note: If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.**
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). **Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.**
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). **Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.**

10.2.6.12. 0x001C UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: UART_SCH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

10.2.6.13. 0x007C UART Status Register(Default Value: 0x0000_0006)

Offset: 0x007C			**Register Name: UART_USR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

10.2.6.14. 0x0080 UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level The bit indicates the number of data entries in the transmit FIFO.

10.2.6.15. 0x0084 UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	RFL Receive FIFO Level The bit indicates the number of data entries in the receive FIFO.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.2.6.16. 0x0088 UART DMA Handshake Configuration Register(Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

10.2.6.17. 0x00A4 UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set to 1, when TFL is less than trig, send the DMA request. If PTE is set to 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set to 1 and FIFO is on, when TFL is less than trig, send DMA request. If PTE is set to 1 and FIFO is off, when THRE is empty, send DMA request. If PTE is set to 0, when FIFO is empty, send DMA request.
6	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, if DMA_PTE_RX is 1 and FIFO is on, when RFL is more than trig, send DRQ. In other cases, once the receive data is valid, send DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user uses HALT[1] to change the baud rate or LCR configuration,

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			write 1 to update the configuration and wait this bit to self-clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baud rate register (DLH and DLL) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled **Note: If FIFOs are not enabled, the setting has no effect on operation.**

10.2.6.18. 0x00B0 UART DBG DLL Register(Default Value: 0x0000_0000)

Offset: 0x00B0			**Register Name: UART_DBG_DLL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLL

10.2.6.19. 0x00B4 UART DBG DLH Register(Default Value: 0x0000_0000)

Offset: 0x00B4			**Register Name: UART_DBG_DLH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLH

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.3. SPI

10.3.1. Overview

The SPI is a full-duplex, synchronous, serial communication interface which allows rapid data communication with fewer software interrupts. The SPI controller contains one 64x8 bits receiver buffer (RXFIFO) and one 64x8 bits transmit buffer (TXFIFO). It can work at master mode and slave mode.

The SPI has the following features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports mode0, mode1, mode2 and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1 bit to 32 bits
- Supports the SPI NAND flash and SPI NOR flash
- Supports standard SPI, dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI

10.3.2. Block Diagram

Figure 10-19 shows a block diagram of the SPI.

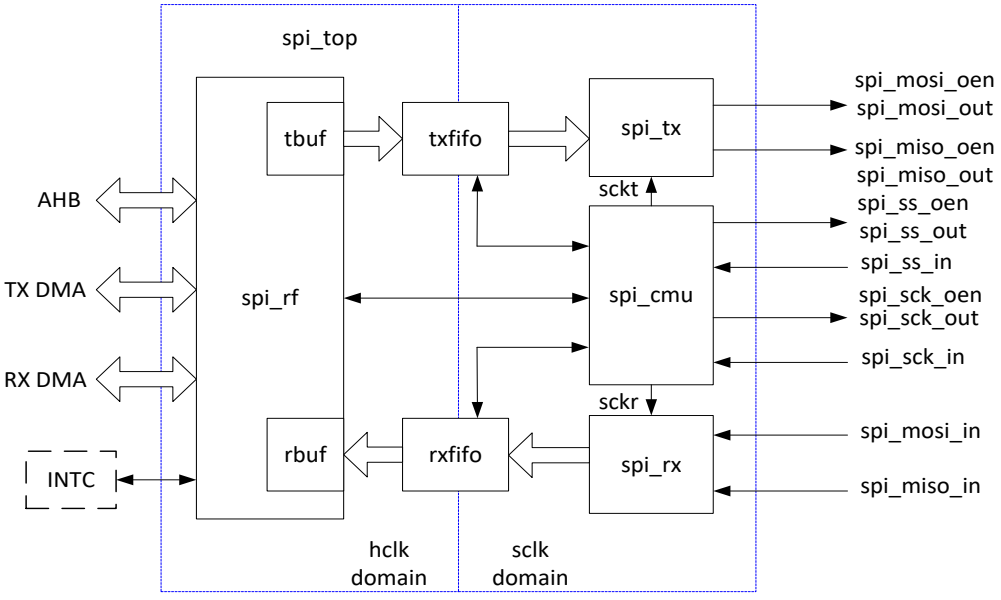


Figure 10- 19. SPI Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The SPI comprises with:
spi_rf: Responsible for implementing the internal register, interrupt and DMA Request.
spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8 bits, then the data is written into the rxfifo.
spi_rbuf: The block is used to convert the rxfifo data into read data length of AHB.
txfifo, rxfifo: For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the txfifo; data received from the external serial device into SPI is pushed into the rxfifo.
spi_cmu: Responsible for implementing SPI bus clock, chip select, internal sample and the generation of transfer clock.
spi_tx: Responsible for implementing SPI data transfer, the interface of the internal txfifo and status register.
spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

10.3.3. Operations and Functional Descriptions

10.3.3.1. External Signals

Table 10-8 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as master device, CLK and CS is output pin; when SPI is configurable as slave device, CLK and CS is input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 10- 8. SPI External Signals

Signal	Description	Type
SPI0_CS0	SPI0 Chip Select Signal0, Low Active	I/O
SPI0_CS1	SPI0 Chip Select Signal1, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_WP	Write protection and active low or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0_HOLD	The HOLD pin is used to temporarily pause serial communication without deselecting or resetting the device. While the HOLD pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1_CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI2_CS	SPI2 Chip Select Signal, Low Active	I/O
SPI2_CLK	SPI2 Clock Signal	I/O
SPI2_MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2_MISO	SPI2 Master Data In, Slave Data Out	I/O

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.3.3.2. Clock Sources

Each SPI interface has 5 different clock sources, users can select one of them to make SPI clock source. Table 10-9 describes the clock sources for SPI.

Table 10- 9. SPI Clock Sources

Clock Sources	Description
OSC24M	24 MHz Crystal
PLL_PERI0(1X)	Peripheral Clock, default value is 600 MHz
PLL_PERI1(1X)	Peripheral Clock, default value is 600 MHz
PLL_PERI0(2X)	Peripheral Clock, default value is 1200 MHz
PLL_PERI1(2X)	Peripheral Clock, default value is 1200 MHz

10.3.3.3. Typical Application

Figure 10-20 shows the application block diagram when the SPI master device is connected to a slave device.

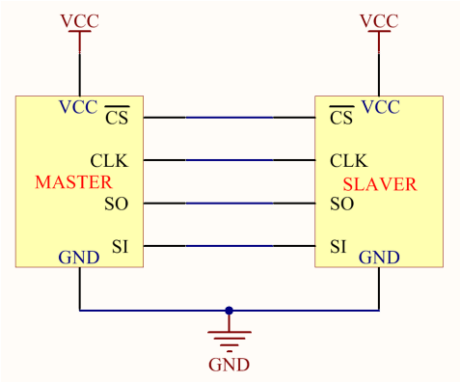


Figure 10- 20. SPI Application Block Diagram

10.3.3.4. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 10-10.

Table 10- 10. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 10-21 and Figure 10-22 describe four waveforms for SPI_SCLK.

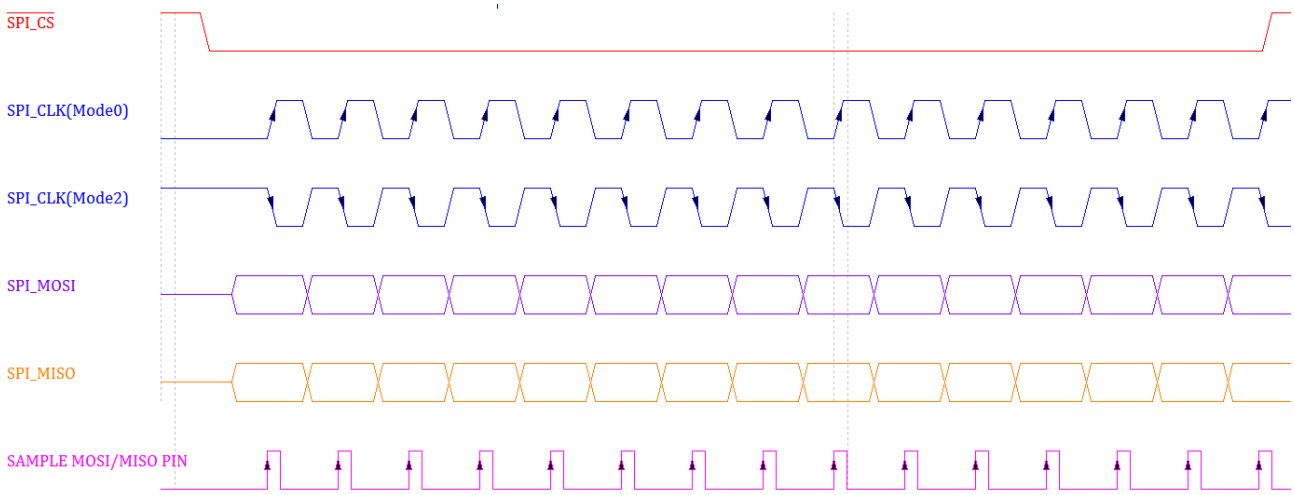


Figure 10- 21. SPI Phase 0 Timing Diagram

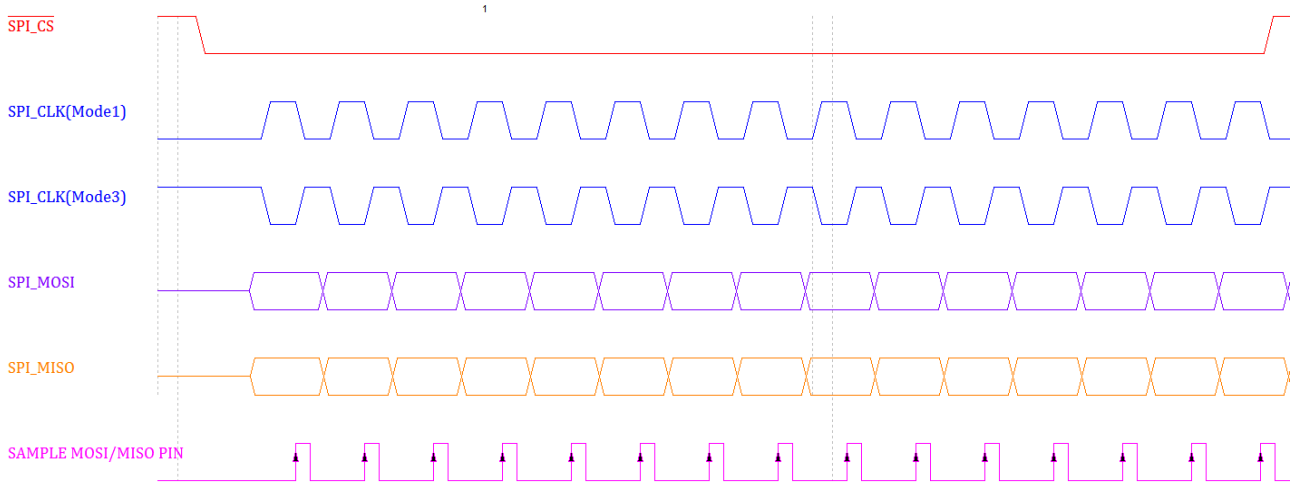


Figure 10- 22. SPI Phase 1 Timing Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.3.3.5. SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register;** slave mode is selected by clearing the **MODE** bit in the **SPI Global Control Register**.

In master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control, **SS_OWNER**(the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In slave mode, after software selects the **MODE** bit to '0', it waits for master initiate a transaction. When the master asserts SPI_SS and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

10.3.3.6. SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the **Work Mode Select(bit[1:0])** is equal to 0x2 in the **SPI Bit-Aligned Transfer Configure Register**. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes this mode.

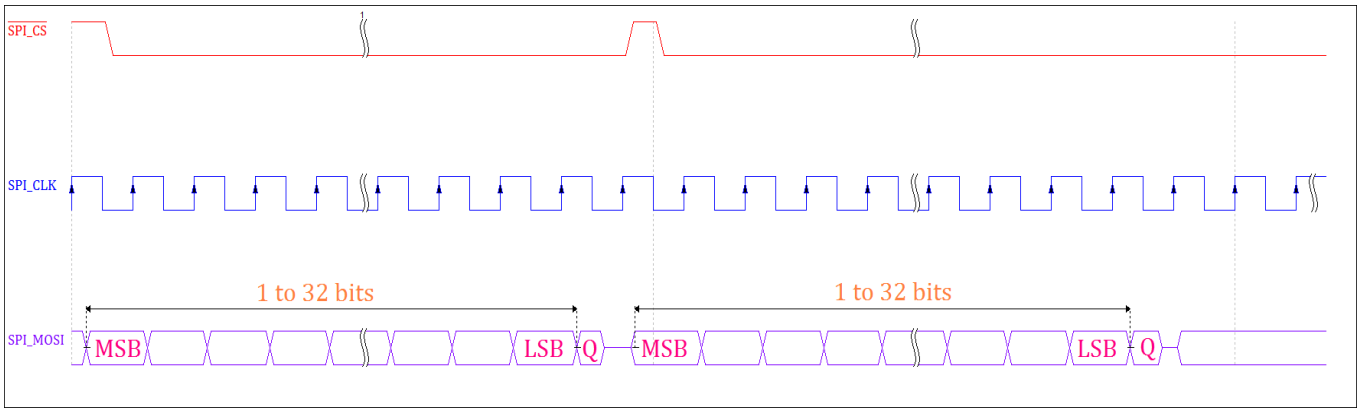


Figure 10- 23. SPI 3-Wire Mode

10.3.3.7. SPI Dual-Input/Dual-Output and Dual I/O Mode

The dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI(Figure 10-24) and the dual I/O SPI(Figure 10-25).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

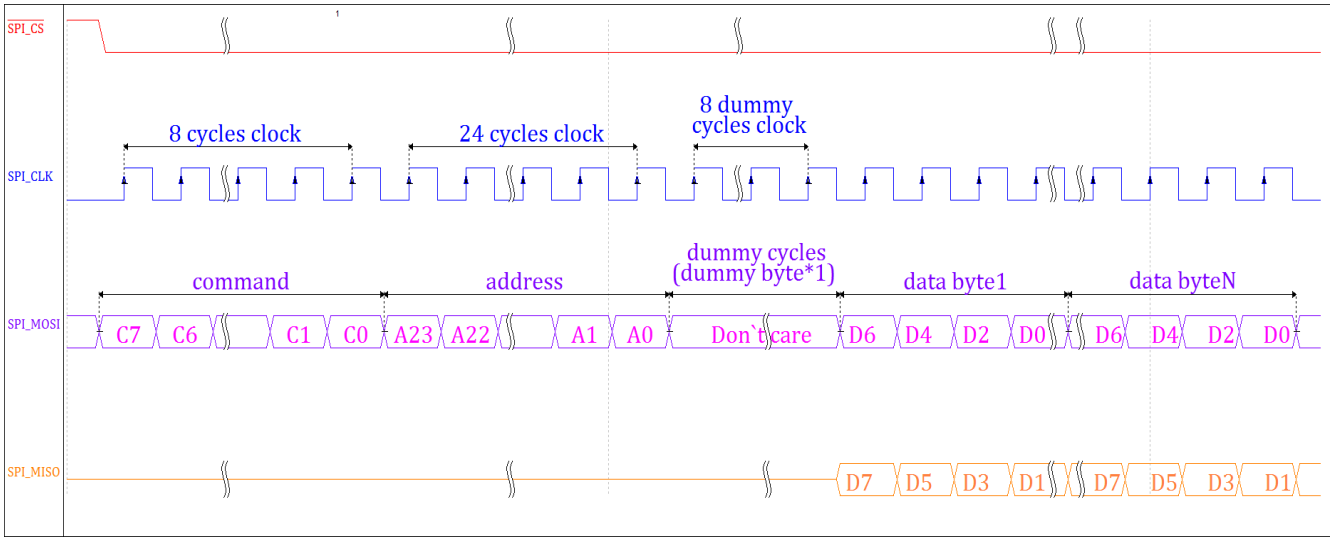


Figure 10- 24. SPI Dual-Input/Dual-Output Mode

In the dual-input/dual-output SPI, the command, address, and the dummy bytes output in unit of a single bit in serial mode through SPI_MOSI line, only the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

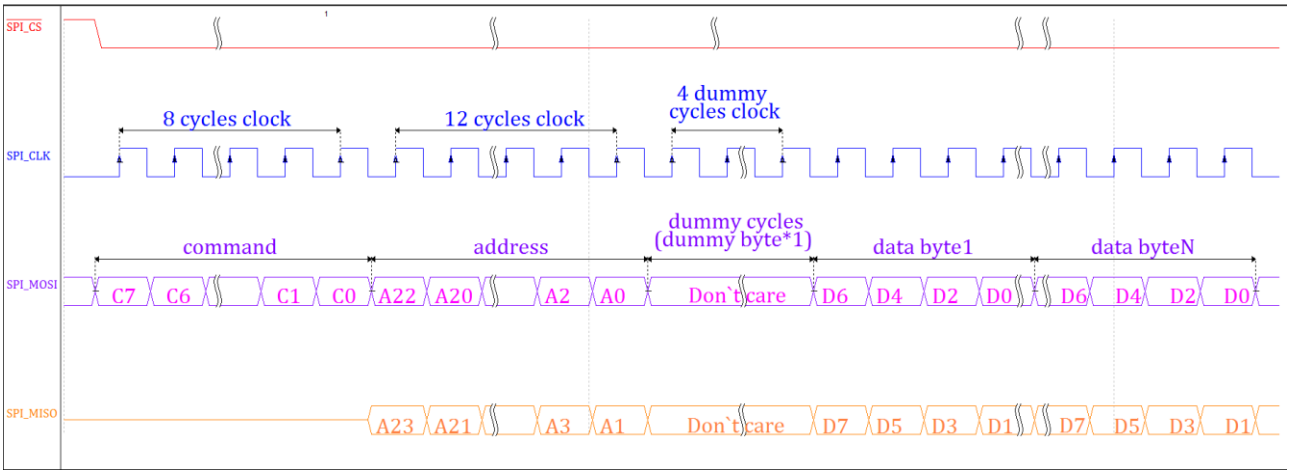


Figure 10- 25. SPI Dual I/O Mode

In the dual I/O SPI, only the command bytes are output in unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

10.3.3.8. SPI Quad-Input/Quad-Output Mode

The quad read mode(SPI x4) is selected when the **Quad_EN**(bit29) is set in the **SPI Master Burst Control Counter Register**. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits(MOSI, MISO, IO2(WP#)and IO3(HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

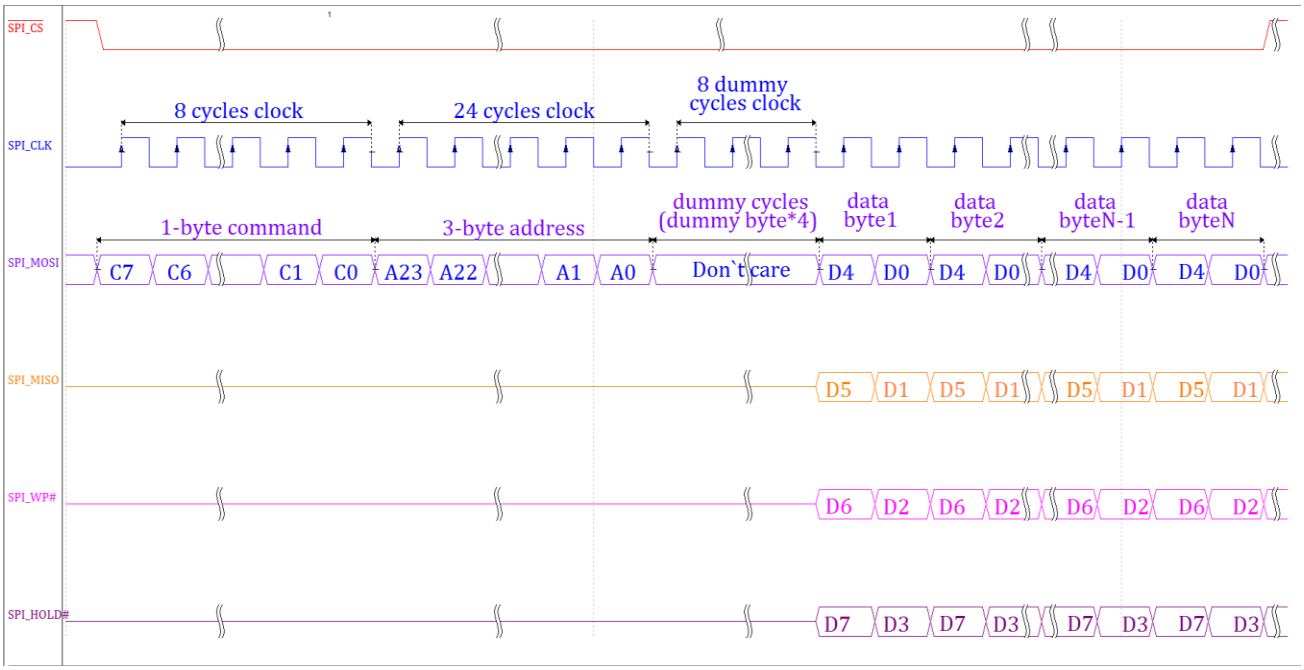


Figure 10- 26. SPI Quad-Input/Quad-Output Mode

In the quad-input/quad-output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output(write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

10.3.3.9. Transmit/Receive Burst in Master Mode

In SPI master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit bursts are written in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** The transmit bursts in single mode before automatically sending dummy burst are written in STC(bit[23:0]) of **SPI Master Burst Control Counter Register.** For dummy data, SPI controller can automatically sent before receiving by writing DBC(bit[27:24]) in **SPI Master Burst Control Counter Register**. If users donot use SPI controller to sent dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** In master mode, the total burst numbers are written in MBC(bit[23:0]) of **SPI Master Burst Counter Register.** When all transmit burst and receive burst are transferred, SPI controller will send an completed interrupt, at the same time, SPI controller will clear DBC,MWTC and MBC.

10.3.3.10. SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz~100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must configure different work mode. There are three work modes: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. The different configuration of SPI sample mode shows in Table 10-11.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 10- 11. SPI Old Sample Mode

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=60 MHz

Table 10- 12. SPI New Sample Mode

SPI Sample Mode	SDM(bit13)	SDC(bit11)	SDC1(bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

10.3.3.11. Calibrate Delay Chain

There is one delay chain in SPI controller, which is used to generate delay to make proper timing between internal SPI clock signal and data signals. Delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SPI. In order to calibrate delay chain by operation registers in SPI, SPI must be enabled through AHB reset and AHB clock gating control registers.

Step2: Configure a proper clock for SPI. Calibration delay chain is based on the clock for SPI from CCU module.

Step3: Set proper initial delay value. Write 0xA0 to delay control register to set initial delay value 0x20 to delay chain. Then write 0x0 to delay control register to clear this value.

Step4: Write 0x8000 to delay control register to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in delay control register) of calibration done is set. The number of delay cells is shown at Bit8~Bit14 in delay control register. The delay time generated by these delay cells is equal to the clock cycle of SPI nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the clock cycle of SPI and the result of calibration.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.3.3.12. SPI Error Conditions

If any error conditions occur, hardware will set the corresponding status bits in the **SPI Interrupt Status Register** and stop the transfer. For the SPI controller, the following error scenarios can happen.

(1) TX_FIFO Underrun

TX_FIFO underrun happens when the CPU/DMA reads from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_UDF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(2) TX_FIFO Overflow

TX_FIFO overflow happens when the CPU/DMA writes into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_OVF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(3) RX_FIFO Underrun

RX_FIFO underrun happens when the CPU/DMA reads from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_UDF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(4) RX_FIFO Overflow

RX_FIFO overflow happens when the CPU/DMA writes into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_OVF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

10.3.4. Programming Guidelines

10.3.4.1. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

(1).CPU Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

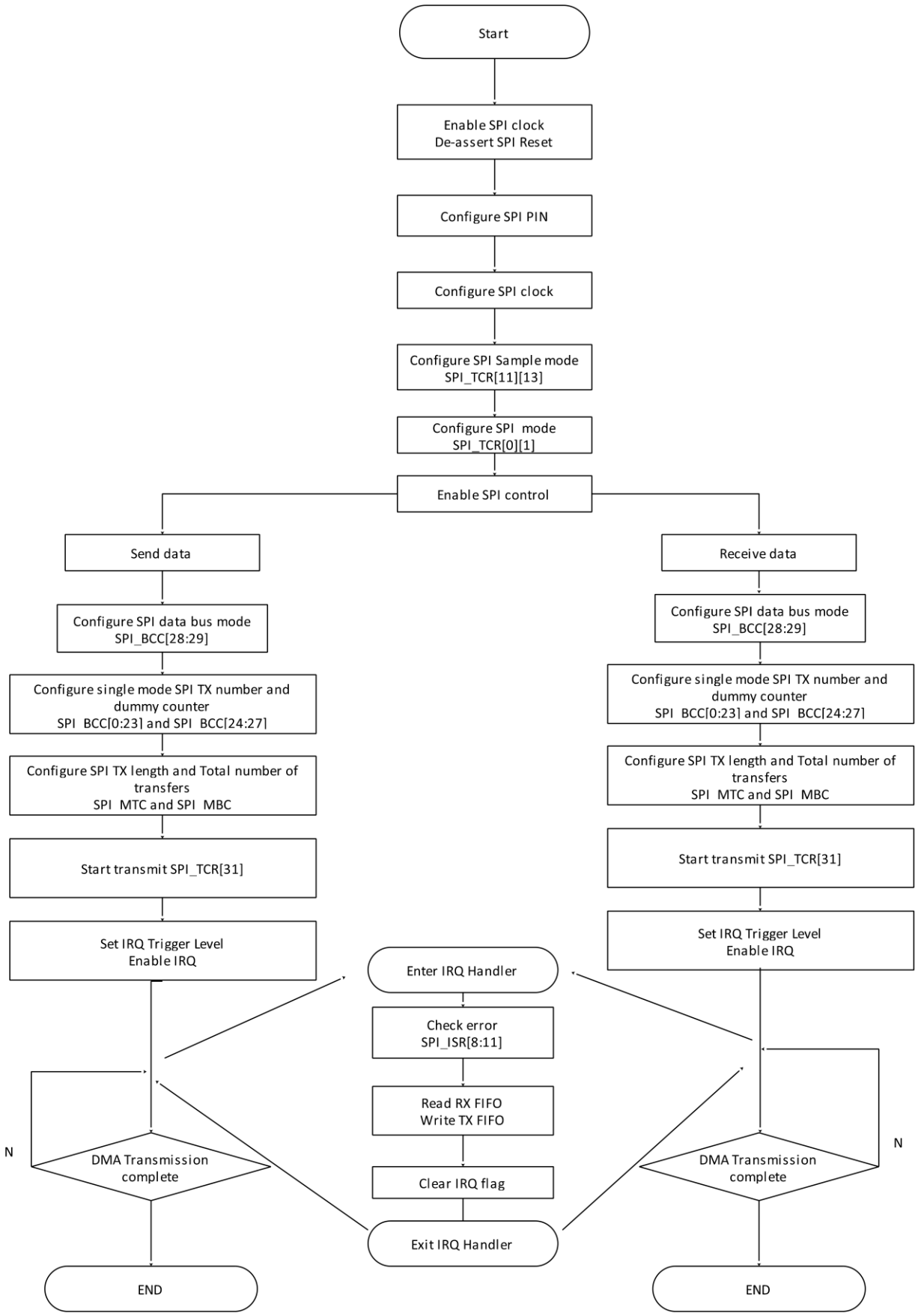


Figure 10- 27. SPI Write/Read Data in CPU Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

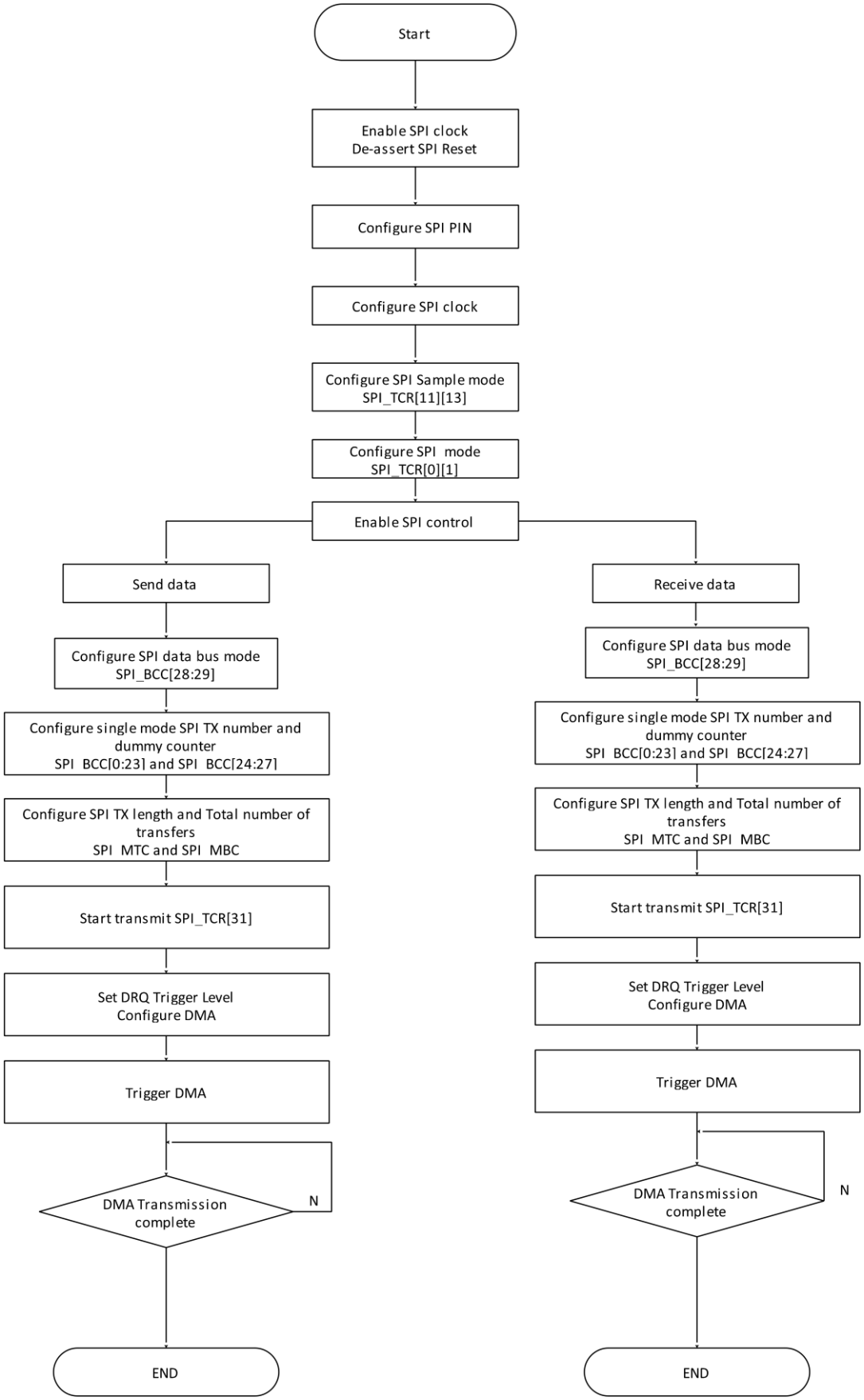


Figure 10- 28. SPI Write/Read Data in DMA Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.3.4.2. Calibrate Delay Chain

The SPI has one delay chain, which is used to generate delay to make proper timing between internal SPI clock signal and data signals. Delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SPI. In order to calibrate delay chain by operation registers in SPI, SPI must be enabled through AHB reset and AHB clock gating control registers.

Step2: Configure a proper clock for SPI. Calibration delay chain is based on the clock for SPI from CCU.

Step3: Set proper initial delay value. Write 0xA0 to delay control register to set initial delay value 0x20 to delay chain. Then write 0x0 to delay control register to clear this value.

Step4: Write 0x8000 to delay control register to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in delay control register) of calibration done is set. The number of delay cells is shown at Bit8~Bit14 in delay control register. The delay time generated by these delay cells is equal to the cycle of SPI clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SPI clock and the result of calibration.

10.3.5. Register List

Module Name	Base Address
SPI0	0x05010000
SPI1	0x05011000
SPI2	0x05012000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Burst Counter Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configuration Register
SPI_3W_CCR	0x0044	SPI Bit-Aligned Clock Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

10.3.6. Register Description

10.3.6.1. 0x0004 SPI Global Control Register(Default Value: 0x0000_0080)

Offset:0x0004			**Register Name: SPI_GCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing ‘1’ to this bit will clear the SPI controller, and auto clear to ‘0’ when reset operation completes. Writing ‘0’ has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full Cannot be written when XCH=1
6:3	/	/	/
2	R/W	0x0	MODE_SELECT 0: Old mode of Sample Timing 1: New mode of Sample Timing Note: Can’t be written when XCH=1
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave mode 1: Master mode Cannot be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			After transforming from bit_mode to byte_mode, it must enable the SPI module again.

10.3.6.2. 0x0008 SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Writing “1” to SRST will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0 – normal operation, do not delay internal read sample point 1 – delay internal read sample point Cannot be written when XCH=1.
14	R/W	0x0	SDDM Sending Data Delay Mode 0:Normal sending 1:Delay sending Set the bit to "1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0. Cannot be written when XCH=1.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode. Cannot be written when XCH=1.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: LSB first Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write. 0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Cannot be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Cannot be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

10.3.6.3. 0x0010 SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: SPI_IER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

10.3.6.4. 0x0014 SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC have been exchanged. In other condition, when set, this bit indicates that all the datas in TXFIFO have been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. TX_WL is the water level of TXFIFO.
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. RX_WL is the water level of RXFIFO.

10.3.6.5. 0x0018 SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			**Register Name: SPI_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable **Note: In normal mode, TX FIFO can only be read by SPI controller, writing ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.**
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, writing '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable **Note: In normal mode, RX FIFO can only be written by SPI controller, writing '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.**
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

10.3.6.6. 0x001C SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

10.3.6.7. 0x0020 SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: SPI_WCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). Cannot be written when XCH=1. 0: No wait states inserted n: n SPI_SCLK wait states inserted **Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer.**
15:0	R/W	0x0	WCC Wait Clock Counter (In master mode) Cannot be written when XCH=1. These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

10.3.6.8. 0x0028 SPI Sample Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

10.3.6.9. 0x0030 SPI Master Burst Counter Register(Default Value: 0x0000_0000)

Offset: 0x0030			**Register Name: SPI_MBC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter Cannot be written when XCH=1. In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1. **Note: Total transfer data, includes the TXD, RXD and dummy burst.**

10.3.6.10. 0x0034 SPI Master Transmit Counter Register(Default Value: 0x0000_0000)

Offset: 0x0034			**Register Name: SPI_MTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.3.6.11. 0x0038 SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: SPI_BCC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable Cannot be written when XCH=1. **Note: Quad mode includes Quad-Input and Quad-Output.**
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Cannot be written when XCH=1. It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			… N: N bursts Cannot be written when XCH=1.

10.3.6.12. 0x0040 SPI Bit-Aligned Transfer Configuration Register(Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when ***Work Mode Select==0x10/0x11.*** 0: Idle 1: Initiates transfer Writing “1” to this bit will start to transfer serial bits frame(the value comes from the ***SPI TX Bit Register*** or ***SPI RX Bit Register***), and will auto clear after the bursts transfer completely. Writing ‘0’ to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Delay Sample Mode 1: Standard Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode. In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in ***SPI TX Bit Register****(or* ***SPI RX Bit Register****)* has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when ***Work Mode Select==0x10/0x11.***
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when ***Work Mode Select==0x10/0x11.***
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit …

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually , set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when ***Work Mode Select= =0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in standard SPI, dual-output/dual input SPI, dual IO SPI and quad-output/quad-input SPI. 01: Reserved 10: Data frame is bit aligned in 3-wire SPI 11: Data frame is bit aligned in standard SPI

10.3.6.13. 0x0044 SPI Bit-Aligned Clock Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

10.3.6.14. 0x0048 SPI TX Bit Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

10.3.6.15. 0x004C SPI RX Bit Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

This register is only valid when *Work Mode Select==0x10/0x11*.

10.3.6.16. 0x0088 SPI Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	Delay Cycles The counts of hold cycles from DMA last signal high to dma_active high

10.3.6.17. 0x0200 SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

10.3.6.18. 0x0300 SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In word

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.4. USB2.0 OTG

10.4.1. Overview

The USB2.0 OTG is a dual-role device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB2.0 Specification. It can support high-speed (HS, 480 Mbit/s), full-speed (FS, 12 Mbit/s), and low-speed (LS, 1.5 Mbit/s) transfers in Host mode. It can support high-speed (HS, 480 Mbit/s), and full-speed (FS, 12 Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

The USB2.0 OTG has the following features:

- Complies with USB2.0 Specification
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) in Host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 10 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfer
- Supports up to (8 KB+64 Bytes) FIFO for all EPs (including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Includes interface to an external Normal DMA controller for every EPs
- Device and Host controller share a 4 KB sram and a physical PHY

10.4.2. Block Diagram

Figure 10-29 shows the block diagram of USB2.0 OTG Controller.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

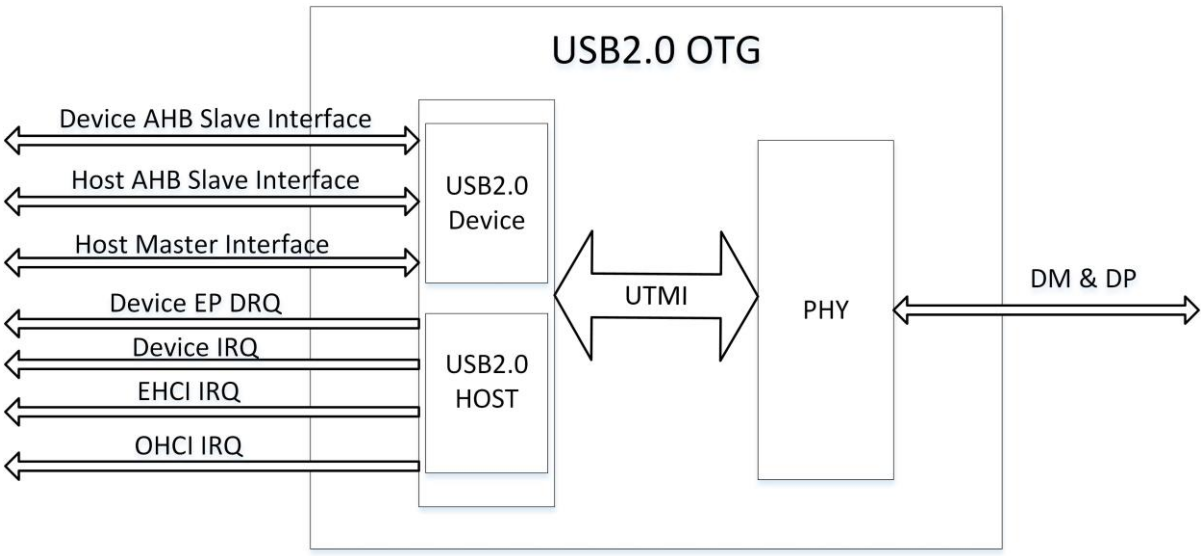


Figure 10- 29. USB2.0 OTG Controller Block Diagram

10.4.3. Operations and Functional Descriptions

10.4.3.1. External Signals

Table 10- 13. USB2.0 OTG External Signals

Signal	Description	Type
USB0_DP	USB2.0 OTG differential signal positive	A I/O
USB0_DM	USB2.0 OTG differential signal negative	A I/O
VCC_USB	USB analog power supply	P
VDD_USB	USB digital power supply	P

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.4.3.2. Controller and PHY Connection Diagram

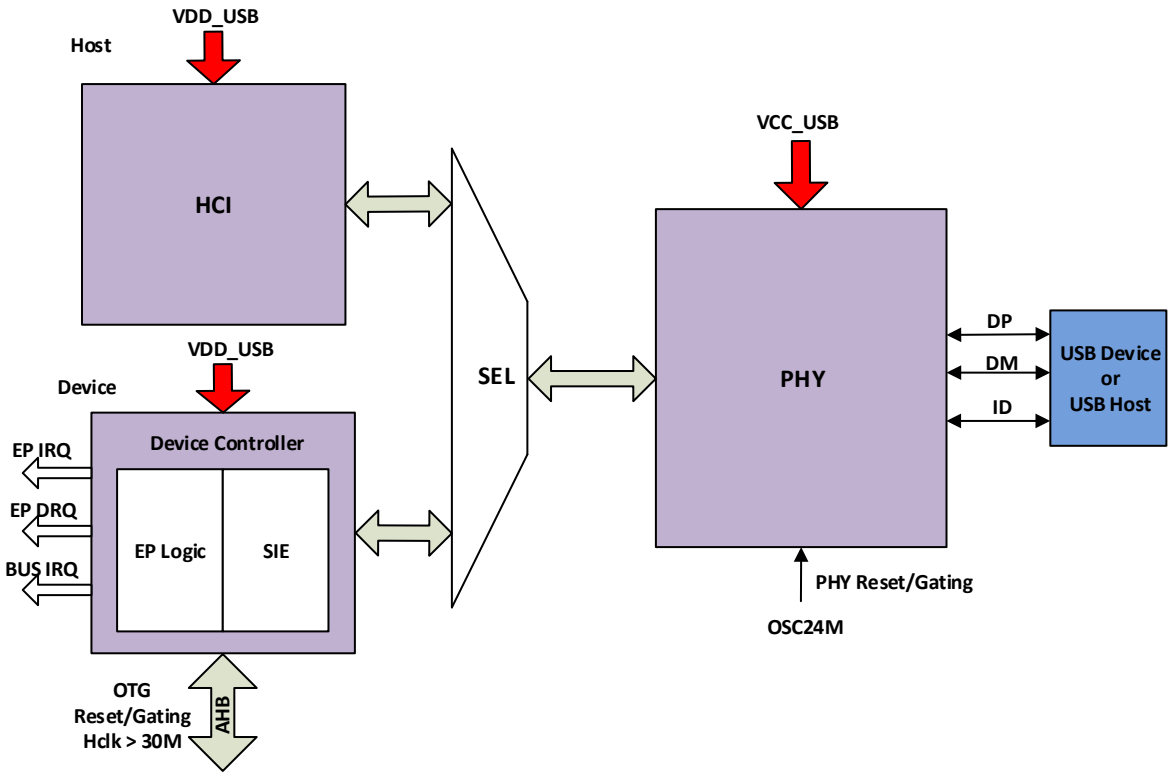


Figure 10- 30. USB2.0 OTG Controller and PHY Connection Diagram

10.4.3.3. Function Implementation

Refer to USB2.0 Specification.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5. USB2.0 Host Controller

10.5.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480Mbit/s transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

The USB2.0 host controller includes the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports 32-bit Little Endian AMBA AHB Slave Bus for Register Access
- Supports 32-bit Little Endian AMBA AHB Master Bus for Memory Access
- Including an internal DMA Controller for data transfer with memory
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) Device
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports only 1 USB Root Port shared between EHCI and OHCI

10.5.2. Block Diagram

Figure 10-31 shows the block diagram of USB2.0 HOST Controller.

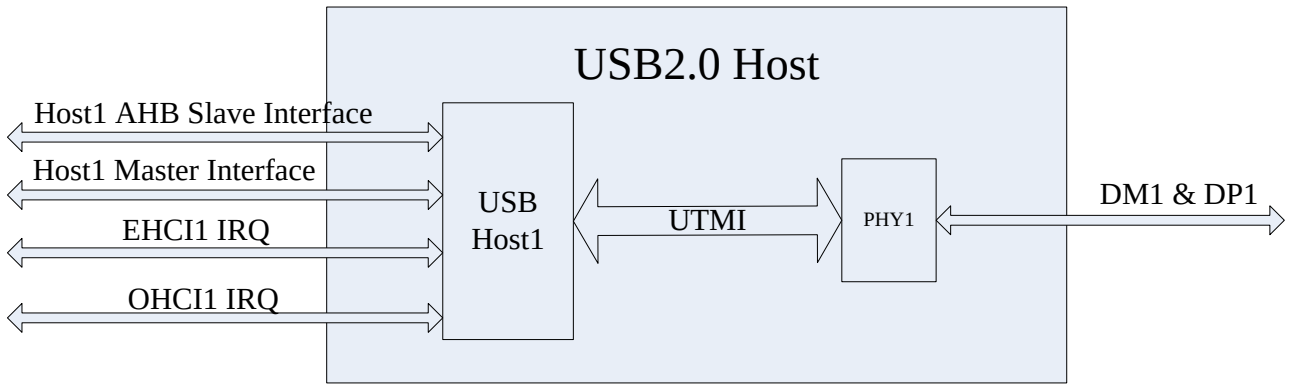


Figure 10- 31. USB2.0 Host Controller Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.3. Operations and Functional Descriptions

10.5.3.1. External Signals

Table 10- 14. USB2.0 HOST External Signals

Signal	Description	Type
USB1_DP	USB2.0 HOST differential signal positive	AI/O
USB1_DM	USB2.0 HOST differential signal negative	AI/O
VCC_USB	USB analog power supply	P
VDD_USB	USB digital power supply	P

10.5.3.2. Controller and PHY Connection Diagram

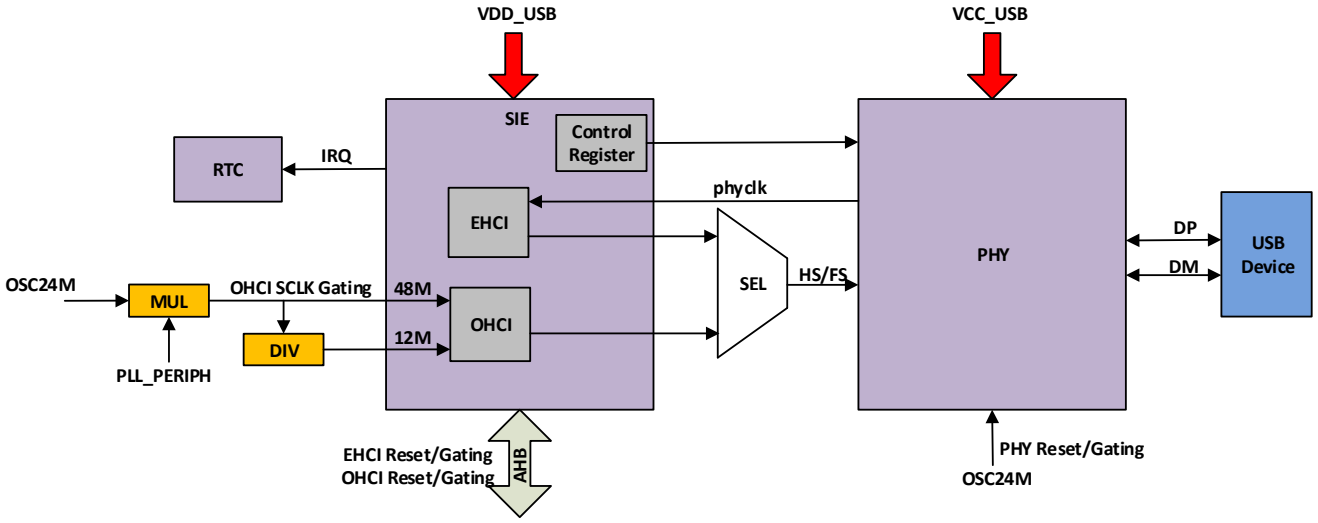


Figure 10- 32. USB2.0 HOST Controller and PHY Connection Diagram

10.5.3.3. Function Implementation

Refer to USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

10.5.4. USB Host Register List

Module Name	Base Address
USB1	0x05200000

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x0000	EHCI Capability Register Length Register
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000C	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x0020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x0024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x0400	OHCI Revision Register
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x0418	OHCI HCCA Base
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Base
O_HcControlHeadED	0x0420	OHCI Control Head ED Base
O_HcControlCurrentED	0x0424	OHCI Control Current ED Base
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Base
O_HcDoneHead	0x0430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x0448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x044C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register
HCI Controller and PHY Interface Register		

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

HCI_Interface	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control Register
PHY_Control	0x0810	PHY Control Register
HSIC_PHY_Tune1	0x081C	HSIC PHY Tune1 Register
HSIC_PHY_Tune2	0x0820	HSIC PHY Tune2 Register
HSIC_PHY_Tune3	0x0824	HSIC PHY Tune3 Register
HCI SIE Port Disable Control	0x0828	HCI SIE Port Disable Control Register

10.5.5. EHCI Register Description

10.5.5.1. 0x0000 EHCI Identification Register(Default Value:0x10)

Offset:0x0000			Register Name: CAPLENGTH
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x10	**CAPLENGTH** The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

10.5.5.2. 0x0002 EHCI Host Interface Version Number Register(Default Value:0x0100)

Offset: 0x0002			Register Name: HCIVERSION
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R	0x0100	**HCIVERSION** This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

10.5.5.3. 0x0004 EHCI Host Control Structural Parameter Register(Default Value:0x0000_0004)

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R	0x0	**Debug Port Number** This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x0	**Number of Companion Controller (N_CC)** This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x0	**Number of Port per Companion Controller(N_PCC)** This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0x0	**Port Routing Rules** This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value / Meaning 0 / The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. 1 / The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	/	/
3:0	R	0x1	**N_PORTS** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

10.5.5.4. 0x0008 EHCI Host Control Capability Parameter Register(Default Value:0x0000_0008)

Offset: 0x0008			**Register Name: HCCPARAMS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R	0x0	**EHCI Extended Capabilities Pointer (EECP)** This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R	0x0	**Isochronous Scheduling Threshold** This field indicates, relative to the current position of the executing host

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	R	0x1	/
2	R	0x0	**Asynchronous Schedule Park Capability** If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x0	**Programmable Frame List Flag** If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

10.5.5.5. 0x000C EHCI Companion Port Route Description(Default Value:0x0000_0000)

Offset: 0x000C			**Register Name: HCSP-PORTROUTE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**HCSP-PORTROUTE** This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.5.6. 0x0010 EHCI USB Command Register(Default Value:0x0008_0000)

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:24</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table><tr><td>Value</td><td>Minimum Interrupt Interval</td></tr><tr><td>0x00</td><td>Reserved</td></tr><tr><td>0x01</td><td>1 micro-frame</td></tr><tr><td>0x02</td><td>2 micro-frame</td></tr><tr><td>0x04</td><td>4 micro-frame</td></tr><tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr><tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr><tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr><tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr></table>Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11</td><td>R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9:8</td><td>R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Light Host Controller Reset(OPTIONAL)
This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td></td><td></td><td></td><td>default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:
<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R/W	0x0	**Host Controller Reset** This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	**Run/Stop** When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

10.5.5.7. 0x0014 EHCI USB Status Register(Default Value:0x0000_1000)

Offset: 0x0014			**Register Name: USBSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	**Asynchronous Schedule Status** The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	**Periodic Schedule Status**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	**Reclamation** This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	**HC Halted** This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	**Interrupt on Async Advance** System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	**Host System Error** The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0x0	**Frame List Rollover** The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	**Port Change Detect** The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	**USB Error Interrupt(USBERRINT)** The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	**USB Interrupt(USBINT)** The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

10.5.5.8. 0x0018 EHCI USB Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0018			**Register Name: USBINTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	**Interrupt on Async Advance Enable** When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	**Host System Error Enable** When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	**Frame List Rollover Enable** When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	**Port Change Interrupt Enable** When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	**USB Error Interrupt Enable** When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	**USB Interrupt Enable** When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.5.9. 0x001C EHCI Frame Index Register(Default Value:0x0000_0000)

<table>
<tr><td colspan="3">Offset: 0x001C</td><td>Register Name: FRINDEX</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13:0</td><td>R/W</td><td>0</td><td>Frame Index
The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register.
<table>
<tr><td>USBCMD[Frame List Size]</td><td>Number Elements</td><td>N</td></tr>
<tr><td>00b</td><td>1024</td><td>12</td></tr>
<tr><td>01b</td><td>512</td><td>11</td></tr>
<tr><td>10b</td><td>256</td><td>10</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
</table>

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

10.5.5.10. 0x0024 EHCI Periodic Frame List Base Address Register(Default Value:0x0000_0000)

<table>
<tr><td colspan="3">Offset: 0x0024</td><td>Register Name: PERIODICLISTBASE</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:12</td><td>R/W</td><td>0x0</td><td>Base Address
These bits correspond to memory address signals [31:12], respectively.
This register contains the beginning address of the Periodic Frame List in the system memory.
System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4 Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.</td></tr>
<tr><td>11:0</td><td>/</td><td>/</td><td>/</td></tr>
</table>

NOTE

Writes must be Dword Writes.

10.5.5.11. 0x0028 EHCI Current Asynchronous List Address Register(Default Value:0x0000_0000)

Offset: 0x0028	Register Name: ASYNCLISTADDR

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:5	R/W	0x0	**Link Pointer (LP)** This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

10.5.5.12. 0x0050 EHCI Configure Flag Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	**Configure Flag(CF)** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not used in the normal implementation.

10.5.5.13. 0x0054 EHCI Port Status and Control Register(Default Value:0x0000_2000)

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	**Wake on Disconnect Enable(WKDSCNNT_E)** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	**Wake on Connect Enable(WKCNNT_E)** Writing this bit to a one enable the port to be sensitive to device connects as wake-up events.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td></td><td></td><td></td><td>This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0x0</td><td>Port Test Control
The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follows:
<table>
<tr><td>Bits</td><td>Test Mode</td></tr>
<tr><td>0000b</td><td>The port is NOT operating in a test mode.</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.</td></tr>
<tr><td>15:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
Note: When software writes this bit to a one , it must also write a zero to the Port Enable bit.

Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr><tr><td>0x</td><td>Disable</td></tr><tr><td>10</td><td>Enable</td></tr><tr><td>11</td><td>Suspend</td></tr></table>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
① Software sets the Force Port Resume bit to a zero(from a one).
② Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The default value in this field is '0'.
6	R/W	0x0	**Force Port Resume** 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	**Over-current Change** Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	**Over-current Active** 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0x0	**Port Enable/Disable Change** Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	**Port Enabled/Disabled** 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	**Connect Status Change** 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	**Current Connect Status** Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

10.5.6. OHCI Register Description

10.5.6.1. 0x0400 HcRevision Register(Default Value:0x0000_0010)

Offset: 0x0400			Register Name: HcRevision
Bit	Read/Write	Default/Hex	Description
	HCD HC		
31:8	/ /	/	/
7:0	R R	0x10	**Revision** This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

10.5.6.2. 0x0404 HcControl Register(Default Value:0x0000_0000)

Offset: 0x0404			Register Name: HcRevision
Bit	Read/Write	Default/Hex	Description

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td></td><td>HCD</td><td>HC</td><td></td><td></td></tr>
<tr><td>31:11</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>10</td><td>R/W</td><td>R</td><td>0x0</td><td>RemoteWakeupEnable
This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>RemoteWakeupConnected
This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of
HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters
USBRESET after a hardware reset. The latter also resets the Root
Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next
Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.
Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</td></tr>
<tr><td>2</td><td>R/W</td><td>R</td><td>0x0</td><td>PeriodicListEnable
This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlBulkServiceRatio
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

10.5.6.3. 0x0408 HcCommandStatus Register(Default Value:0x0000_0000)

<table>
<tr><td colspan="4">Offset: 0x0408</td><td>Register Name: HcCommandStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td>31:18</td><td>/</td><td>/</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>17:16</td><td>R</td><td>R/W</td><td>0x0</td><td>SchedulingOverrunCount
These bits are incremented on each scheduling overrun error. It is</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if **SchedulingOverrun** in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	**OwershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the **OwnershipChange** field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	**BulklListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as **BulkListFilled** is 0, HC will not start processing the Bulk list. If **BulkListFilled** is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set **BulkListFilled** to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set **BulkListFilled**, then **BulkListFilled** will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as **ControlListFilled** is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set **ControlListFilled** to 0. If HC finds a TD on the list, then HC will set **ControlListFilled** to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set **ControlListFilled**, then **ControlListFilled** will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	**HostControllerReset** This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

10.5.6.4. 0x040C HcInterruptStatus Register(Default Value:0x0000_0000)

Offset: 0x040C	Register Name: HcInterruptStatus

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	**RootHubStatusChange** This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[**NumberofDownstreamPort**] has changed.
5	R/W	R/W	0x0	**FrameNumberOverflow** This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	**StartofFrame** This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	**WritebackDoneHead** This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the **SchedulingOverrunCount** of *HcCommandStatus* to be incremented.

10.5.6.5. 0x0410 HcInterruptEnable Register(Default Value:0x0000_0000)

Offset: 0x0410				Register Name: HcInterruptEnable Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	**MasterInterruptEnable** A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	**RootHubStatusChange Interrupt Enable**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	**FrameNumberOverflow Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	**UnrecoverableError Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	**ResumeDetected Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	**StartofFrame Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	**WritebackDoneHead Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	**SchedulingOverrun Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

10.5.6.6. 0x0414 HcInterruptDisable Register(Default Value:0x0000_0000)

Offset: 0x0414				**Register Name: HcInterruptDisable Register**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	**MasterInterruptEnable** A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	**RootHubStatusChange Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	**FrameNumberOverflow Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	**UnrecoverableError Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	**ResumeDetected Interrupt Disable**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	**StartofFrame Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W	R	0x0	**WritebackDoneHead Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	**SchedulingOverrun Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Scheduling Overrun;

10.5.6.7. 0x0418 HcHCCA Register(Default Value:0x0000_0000)

Offset: 0x0418				Register Name: HcHCCA
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:8	R/W	R	0x0	**HCCA[31:8]** This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	**HCCA[7:0]** The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

10.5.6.8. 0x041C HcPeriodCurrentED Register(Default Value:0x0000_0000)

Offset: 0x041C				Register Name: HcPeriodCurrentED(PCED)
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R	R/W	0x0	**PCED[31:4]** This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	**PCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.6.9. 0x0420 HcControlHeadED Register(Default Value:0x0000_0000)

Offset: 0x0420				Register Name: HcControlHeadED[CHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	**EHCD[31:4]** The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	**EHCD[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.6.10. 0x0424 HcControlCurrentED Register

Offset: 0x0424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	**CCED[31:4]** The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	**CCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.6.11. 0x0428 HcBulkHeadED Register(Default Value:0x0000_0000)

Offset: 0x0428				Register Name: HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	**BHED[31:4]** The HcBulkHeadED register contains the physical address of the first

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	**BHED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.6.12. 0x042C HcBulkCurrentED Register(Default Value:0x0000_0000)

Offset: 0x042C				Register Name: HcBulkCurrentED [BCED]
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R/W	R/W	0x0	**BulkCurrentED[31:4]** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the **ControlListFilled** of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the **BulkListEnable** of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	**BulkCurrentED [3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.6.13. 0x0430 HcDoneHead Register(Default Value:0x0000_0000)

Offset: 0x0430				Register Name: HcDoneHead
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R	R/W	0x0	**HcDoneHead[31:4]** When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the **WritebackDoneHead** of *HcInterruptStatus*.
3:0	R	R	0x0	**HcDoneHead[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.6.14. 0x0434 HcFmInterval Register(Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	**FrameIntervalToggler** HCD toggles this bit whenever it loads a new value to **FrameInterval**.
30:16	R/W	R	0x0	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the **HostControllerReset** field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

10.5.6.15. 0x0438 HcFmRemaining Register(Default Value:0x0000_0000)

Offset: 0x0438				Register Name: HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	**FrameRemaining Toggle** This bit is loaded from the **FrameIntervalToggle** field of *HcFmInterval* whenever **FrameRemaining** reaches 0. This bit is used by HCD for the synchronization between **FrameInterval** and **FrameRemaining**.
30:14	/	/	/	/
13:0	R	RW	0x0	**FramRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.6.16. 0x043C HcFmNumber Register(Default Value:0x0000_0000)

Offset: 0x043C				Register Name: HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/
15:0	R	R/W	0x0	**FrameNumber** This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the **FrameNumber** at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the **StartofFrame** in *HcInterruptStatus.*

10.5.6.17. 0x0440 HcPeriodicStart Register(Default Value:0x0000_0000)

Offset: 0x0440				Register Name: HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (0x3e67??). When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

10.5.6.18. 0x0444 HcLSThreshold Register(Default Value:0x0000_0628)

Offset: 0x0444				Register Name: HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/
11:0	R/W	R	0x0628	**LSThreshold** This field contains a value which is compared to the **FrameRemaining** field prior to initiating a Low Speed transaction. The transaction is started only if **FrameRemaining** [3] this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.6.19. 0x0448 HcRhDescriptorA Register(Default Value:0x0200_1201)

Offset: 0x0448				Register Name: HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	**PowerOnToPowerGoodTime[POTPGT]** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the **OverCurrentProtectionMode** field specifies global or per-port reporting. **0** Over-current status is reported collectively for all downstream ports. **1** No overcurrent protection supported.
11	R/W	R	0x0	**OverCurrentProtectionMode** This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as **PowerSwitchingMode**. This field is valid only if the **NoOverCurrentProtection** field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	**Device Type** This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the **NoPowerSwitching** field is cleared. 0 All ports are powered at the same time. 1 Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the **PortPowerControlMask** bit is set, the port responds only to port power commands (**Set/ClearPortPower**). If the port mask is cleared, then the port is controlled only by the global power switch (**Set/ClearGlobalPower**).

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8	R/W	R	0x0	**NoPowerSwithcing** These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the **PowerSwitchingMode** specifies global or per-port switching. **0** Ports are power switched. **1** Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

10.5.6.20. 0x044C HcRhDescriptorB Register (Default Value:0x0000_0000)

Offset: 0x044C				**Register Name: HcRhDescriptorB Register**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:16	R/W	R	0x0	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when **PowerSwitchingMode** is set. When set, the port's power state is only affected by per-port power control (**Set/ClearPortPower**). When cleared, the port is controlled by the global power switch (**Set/ClearGlobalPower**). If the device is configured to global switching mode (**PowerSwitchingMode** = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. … Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. … Bit15 Device attached to Port #15.

10.5.6.21. 0x0450 HcRhStatus Register(Default Value:0x0000_0000)

Offset: 0x0450	**Register Name: HcRhStatus Register**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	**(write)ClearRemoteWakeupEnable** Write a '1' clears **DeviceRemoteWakeupEnable.** Writing a '0' has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	**OverCurrentIndicatorChang** This bit is set by hardware when a change has occurred to the **OverCurrentIndicator** field of this register. The HCD clears this bit by writing a '1'. Writing a '0' has no effect.
16	R/W	R	0x0	**(read)LocalPowerStartusChange** The Root Hub does not support the local power status features, thus, this bit is always read as '0'. **(write)SetGlobalPower** In global power mode (**PowerSwitchingMode**=0), This bit is written to '1' to turn on power to all ports (clear **PortPowerStatus**). In per-port power mode, it sets **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a '0' has no effect.
15	R/W	R	0x0	**(read)DeviceRemoteWakeupEnable** This bit enables a **ConnectStatusChange** bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the **ResumeDetected** interrupt. 0 – **ConnectStatusChange** is not a remote wakeup event. 1 – **ConnectStatusChange** is a remote wakeup event. **(write)SetRemoteWakeupEnable** Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	R	0x0	**(Read)LocalPowerStatus** When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. **(Write)ClearGlobalPower** When write, this bit is operated as the ClearGlobalPower. In global power mode (**PowerSwitchingMode**=0), This bit is written to '1' to turn off power to all ports (clear **PortPowerStatus**). In per-port power mode, it clears **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a '0' has no effect.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.5.6.22. 0x0454 HcRhPortStatus Register(Default Value:0x0000_0100)

Offset: 0x0454				Register Name: HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	/	/
20	R/W	R/W	0x0	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the **PortOverCurrentIndicator** bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in **PortOverCurrentIndicator** 1 **PortOverCurrentIndicator** has changed
18	R/W	R/W	0x0	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when **ResetStatusChange** is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	**PortEnableStatusChange** This bit is set when hardware events cause the **PortEnableStatus** bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in **PortEnableStatus** 1 change in **PortEnableStatus**
16	R/W	R/W	0x0	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared when a **SetPortReset,SetPortEnable**, or **SetPortSuspend** write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 no change in **PortEnableStatus** 1 change in **PortEnableStatus** **Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.**
15:10	/	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

Note: This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a</td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td></td><td></td><td></td><td></td><td>‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table>
<tr><td>0</td><td>no overcurrent condition.</td></tr>
<tr><td>1</td><td>overcurrent condition detected.</td></tr>
</table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table>
<tr><td>0</td><td>port is not suspended</td></tr>
<tr><td>1</td><td>port is suspended</td></tr>
</table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
<table>
<tr><td>0</td><td>port is disabled</td></tr>
<tr><td>1</td><td>port is enabled</td></tr>
</table></td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				(write)**SetPortEnable** The HCD sets **PortEnableStatus** by writing a '1'. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared, this write does not set **PortEnableStatus**, but instead sets **ConnectStatusChange**. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)**CurrentConnectStatus** This bit reflects the current state of the downstream port. 0 – No device connected 1 – Device connected (write)**ClearPortEnable** The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. **Note: This bit is always read '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).**

10.5.7. HCI Contgroller and PHY Interface Description

10.5.7.1. 0x0800 HCI Interface Register(Default Value:0x1000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USB Standby Clock Select 0: Normal mode usb clock as usual 1: Standby mode usb clock switch to RC 16M clock
30:29	/	/	/.
28	R	0x1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0x0	OHCI count select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0x0	Simulation mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0x0	EHCI HS force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19	/	/	/
18	R/W	0x0	1: within 2us of the resume-K to SE0 transition

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0x0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0x0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: Do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0x0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: Do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0x0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: Do not use INCR4,use other enabled INCRX or unspecified length burst INCR
8	R/W	0x0	AHB Master interface INCRX align enable 1: Start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of 11:9 is enabled
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0: Clock gated 1: Clock ungated
2	R/W	0x0	RC Generation Enable 0: Disable 1: Enable
1	/	/	/
0	R/W	0x0	ULPI Bypass Enable 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

10.5.7.2. 0x0808 HCI Control 3 Register(Default Value:0x0000_0000)

Offset: 0x808			**Register Name: HCI_CTRL3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	Reserved
16	R/W1C	0x1	Linestate Change Detect 0: Linestate change not dected. 1: Linestate change dected.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to clear.
15:4	/	/	Reserved
3	R/W	0x0	Remote Wakeup Enable 1: Enable 0: Disable
2	/	/	Reserved
1	R/W	0x0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0x0	Linestate Change Detect Enable 1: Enable 0: Disable

10.5.7.3. 0x0810 PHY Control Register(Default Value: 0x0000_0008)

Offset: 0x0810			Register Name: PHY_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	FSEL PHY Clock Selection 0: PHY Clock is 24MHz 1: PHY Clock is 19.2MHz
15:8	/	/	/
7	R/W	0x0	LOOPBACKENB
6	R/W	0x0	IDPULLUP
5	R/W	0x0	VBUSVLDEXT (for phy vbus) 0: Invalid 1: Valid
4	R/W	0x0	VBUSVLDEXTSEL Internal signal has been tied to ‘1’. This bit has no effect.
3	R/W	0x0	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0x0	COMMONONN
1:0	R/W	0x0	VATESTENB

10.5.7.4. 0x081C HSIC PHY Tune1 Register(Default Value: 0x0000_0010)

Offset: 0x081C			Register Name: HSIC_PHY_Tune1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:5	/	/	TXRPUTUNE

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5:4	R/W	0x1	TXRPDTUNE
3:0	R/W	0x0	TXSRTUNE

10.5.7.5. 0x0820 HSIC PHY Tune2 Register(Default Value: 0x0000_0010)

Offset: 0x0820			Register Name: HSIC_PHY_Tune2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	bist_en
30	R/W	0x0	TESTBURNIN
29	R/W	0x0	TESTDATAOUTSEL
28	R/W	0x0	TESTCLK
27:24	R/W	0x0	TESTADDR
23:16	R/W	0x0	TESTDATAIN
15:4	R/W	0x1	siddq
3:0	R/W	0x0	refclk div

10.5.7.6. 0x0824 HSIC PHY Tune3 Register(Default Value: 0x0000_0010)

Offset: 0x0824			Register Name: HSIC_PHY_Tune3
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
5	R/W	0x0	hsic bist_error
4	R/W	0x0	hsic bist_done
3:2	R/W	0x0	hsic testdata out[3:2]
1	R/W	0x1	Non-hsic mode bist_error testdata out[1]
0	R/W	0x0	Non-hsic mode bist_done testdata out[0]

10.5.7.7. 0x0828 HCI SIE Port Disable Control Register(Default Value:0x1000_0000)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b.
15:5	/	/	/
4	R/W	0x0	resume_sel When set k-se0 transition 2us, setting this bit to 1, which is cooperated with ss_utmi_backward_enb_i.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:2	/	/	/
1:0	R/W	0x0	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11:Port Disable when no-se0 3 time detect before SOF during 8 frames

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6. Port Controller

10.6.1. Overview

The Port Controller can be configured with multi-functional input/output pins. All these ports can be configured as GPIO only if multiplexed functions are not used. The total 8 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

The Port Controller has the following features:

- 8 ports(PB,PC,PD,PE,PF,PG,PH,PL)
- Software control for each signal pin
- GPIO peripheral can produce interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 115 interrupts
- Configurable interrupt edges

10.6.2. Block Diagram

The block diagram of port controller is shown in Figure 10-33.

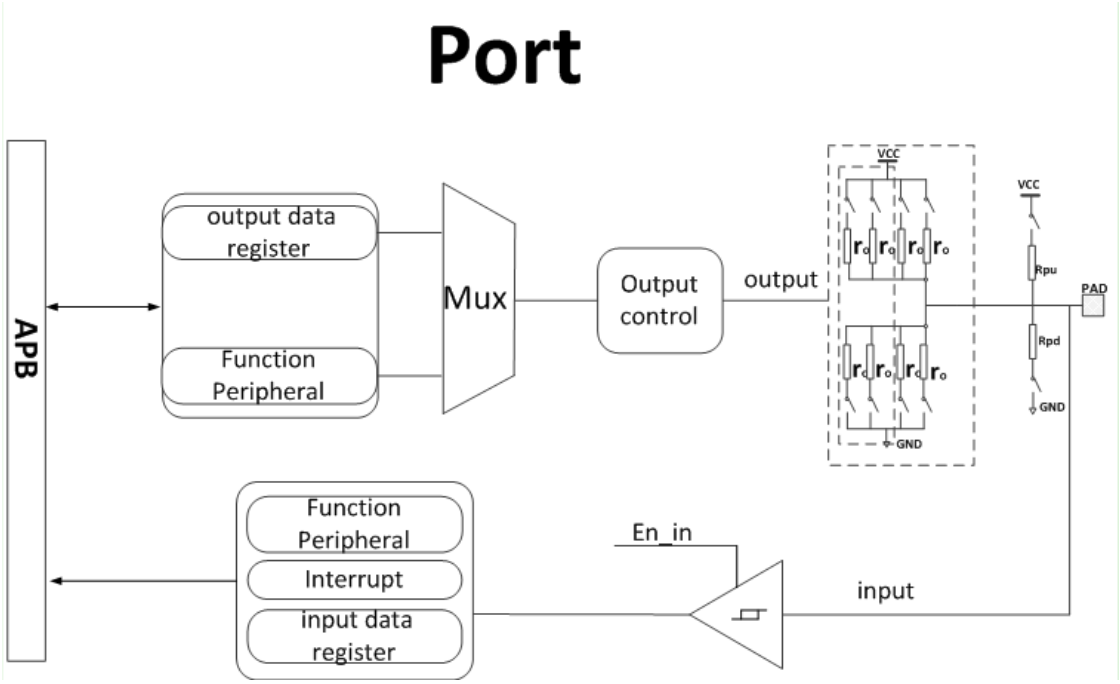


Figure 10- 33. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad, etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

10.6.3. Operations and Functional Descriptions

10.6.3.1. Multi-function Port Table

The A133 includes 115 multi-functional input/output port pins. There are 8 ports as listed below:

Table 10- 15. A133 Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PB	11	Schmitt	CMOS	UART/TWI/OWA/SPI/I2S/JTAG/PWM/PB_EINT	3.3 V
PC	17	Schmitt	CMOS	NAND/SMHC/SPI/PC_EINT	1.8 V/3.3 V
PD	24	Schmitt	CMOS	LCD/LVDS/PWM/DSI/SPI/UART/TWI/PD_EINT	1.8 V/3.3 V
PE	10	Schmitt	CMOS	MIPI/TWI/CSI/PLL_LOCK_DBG/BIST_RESULT/ I2S/LEDC/TCON/PE_EINT	1.8 V/3.3 V
PF	7	Schmitt	CMOS	SMHC/UART/JTAG/PF_EINT	1.8 V/3.3 V
PG	14	Schmitt	CMOS	SMHC/UART/I2S/PG_EINT	1.8 V/3.3 V
PH	20	Schmitt	CMOS	TWI/UART/DMIC/CIR/SPI/TWI/I2S/EMAC/LEDC /PH_EINT	3.3 V
PL	12	Schmitt	CMOS	UART/PWM/TWI/JTAG/S_CPU_CUR_W/ PL_EINT	1.8 V/3.3 V

The multiplex function pins are shown in Table 10-16 to Table 10-23.

Table 10- 16. PB Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PB0	UART2_TX	SPI2_CS	JTAG_MS		PB_EINT0
PB1	UART2_RX	SPI2_CLK	JTAG_CK		PB_EINT1
PB2	UART2_RTS	SPI2_MOSI	JTAG_DO		PB_EINT2
PB3	UART2_CTS	SPI2_MISO	JTAG_DI		PB_EINT3
PB4	TWI1_SCK	I2S0_MCLK	JTAG_MS_GPU		PB_EINT4
PB5	TWI1_SDA	I2S0_BCLK	JTAG_CK_GPU		PB_EINT5
PB6		I2S0_LRCK	JTAG_DO_GPU		PB_EINT6
PB7		I2S0_DOUT0	I2S0_DIN1		PB_EINT7
PB8	OWA_OUT	I2S0_DIN0	I2S0_DOUT1		PB_EINT8
PB9	UART0_TX	TWI0_SCK	JTAG_DI_GPU		PB_EINT9
PB10	UART0_RX	TWI0_SDA	PWM1		PB_EINT10

Table 10- 17. PC Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PC0	NAND_WE	SDC2_DS			PC_EINT0
PC1	NAND_ALE	SDC2_RST			PC_EINT1
PC2	NAND_CLE		SPI0_MOSI		PC_EINT2
PC3	NAND_CE1		SPI0_CS0		PC_EINT3
PC4	NAND_CE0		SPI0_MISO		PC_EINT4
PC5	NAND_RE	SDC2_CLK			PC_EINT5
PC6	NAND_RB0	SDC2_CMD			PC_EINT6
PC7	NAND_RB1		SPI0_CS1		PC_EINT7
PC8	NAND_DQ7	SDC2_D3			PC_EINT8
PC9	NAND_DQ6	SDC2_D4			PC_EINT9
PC10	NAND_DQ5	SDC2_D0			PC_EINT10
PC11	NAND_DQ4	SDC2_D5			PC_EINT11
PC12	NAND_DQS		SPI0_CLK		PC_EINT12
PC13	NAND_DQ3	SDC2_D1			PC_EINT13
PC14	NAND_DQ2	SDC2_D6			PC_EINT14
PC15	NAND_DQ1	SDC2_D2	SPI0_WP		PC_EINT15
PC16	NAND_DQ0	SDC2_D7	SPI0_HOLD		PC_EINT16

Table 10- 18. PD Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PD0	LCD0_D2	LVDS0_D0P	DSI_DP0		PD_EINT0
PD1	LCD0_D3	LVDS0_D0N	DSI_DM0		PD_EINT1
PD2	LCD0_D4	LVDS0_D1P	DSI_DP1		PD_EINT2
PD3	LCD0_D5	LVDS0_D1N	DSI_DM1		PD_EINT3
PD4	LCD0_D6	LVDS0_D2P	DSI_CKP		PD_EINT4
PD5	LCD0_D7	LVDS0_D2N	DSI_CKM		PD_EINT5
PD6	LCD0_D10	LVDS0_CKP	DSI_DP2		PD_EINT6
PD7	LCD0_D11	LVDS0_CKN	DSI_DM2		PD_EINT7
PD8	LCD0_D12	LVDS0_D3P	DSI_DP3		PD_EINT8
PD9	LCD0_D13	LVDS0_D3N	DSI_DM3		PD_EINT9
PD10	LCD0_D14	LVDS1_D0P	SPI1_CS		PD_EINT10
PD11	LCD0_D15	LVDS1_D0N	SPI1_CLK		PD_EINT11
PD12	LCD0_D18	LVDS1_D1P	SPI1_MOSI		PD_EINT12
PD13	LCD0_D19	LVDS1_D1N	SPI1_MISO		PD_EINT13
PD14	LCD0_D20	LVDS1_D2P	UART3_TX		PD_EINT14
PD15	LCD0_D21	LVDS1_D2N	UART3_RX		PD_EINT15
PD16	LCD0_D22	LVDS1_CKP/ PLL_TEST_CKP	UART3_RTS		PD_EINT16
PD17	LCD0_D23	LVDS1_CKN/ PLL_TEST_CKN	UART3_CTS		PD_EINT17
PD18	LCD0_CLK	LVDS1_D3P	UART4_TX		PD_EINT18
PD19	LCD0_DE	LVDS1_D3N	UART4_RX		PD_EINT19
PD20	LCD0_HSYNC	PWM2	UART4_RTS		PD_EINT20

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PD21	LCD0_VSYNC	PWM3	UART4_CTS		PD_EINT21
PD22	PWM1		TWI0_SCK		PD_EINT22
PD23	PWM0		TWI0_SDA		PD_EINT23

Table 10- 19. PE Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PE0	MIPI_MCLK0				PE_EINT0
PE1	TWI2_SCK				PE_EINT1
PE2	TWI2_SDA				PE_EINT2
PE3	TWI3_SCK				PE_EINT3
PE4	TWI3_SDA				PE_EINT4
PE5	MIPI_MCLK1	PLL_LOCK_DBG	I2S2_MCLK	LEDC	PE_EINT5
PE6		BIST_RESULT0	I2S2_BCLK		PE_EINT6
PE7	CSI_SM_VS	BIST_RESULT1	I2S2_LRCK		PE_EINT7
PE8		BIST_RESULT2	I2S2_DOUT0		PE_EINT8
PE9		BIST_RESULT3	I2S2_DIN0		PE_EINT9

Table 10- 20. PF Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PF0	SDC0_D1	JTAG_MS	JTAG_MS_GPU		PF_EINT0
PF1	SDC0_D0	JTAG_DI	JTAG_DI_GPU		PF_EINT1
PF2	SDC0_CLK	UART0_TX			PF_EINT2
PF3	SDC0_CMD	JTAG_DO	JTAG_DO_GPU		PF_EINT3
PF4	SDC0_D3	UART0_RX			PF_EINT4
PF5	SDC0_D2	JTAG_CK	JTAG_CK_GPU		PF_EINT5
PF6					PF_EINT6

Table 10- 21. PG Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PG0	SDC1_CLK				PG_EINT0
PG1	SDC1_CMD				PG_EINT1
PG2	SDC1_D0				PG_EINT2
PG3	SDC1_D1				PG_EINT3
PG4	SDC1_D2				PG_EINT4
PG5	SDC1_D3				PG_EINT5
PG6	UART1_TX				PG_EINT6
PG7	UART1_RX				PG_EINT7
PG8	UART1_RTS				PG_EINT8
PG9	UART1_CTS	I2S1_MCLK			PG_EINT9
PG10		I2S1_BCLK			PG_EINT10
PG11		I2S1_LRCK			PG_EINT11

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PG12		I2S1_DOUT0	I2S1_DIN1		PG_EINT12
PG13		I2S1_DIN0	I2S1_DOUT1		PG_EINT13

Table 10- 22. PH Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PH0	TWI0_SCK			RGMII0_RXD1/ RMII0_RXD1	PH_EINT0
PH1	TWI0_SDA			RGMII0_RXD0/ RMII0_RXD0	PH_EINT1
PH2	TWI1_SCK	CPU_CUR_W		RGMII0_RXCTL/ RMII0_CRS_DV	PH_EINT2
PH3	TWI1_SDA	CIR_OUT		RGMII0_CLKIN/ RMII0_RXER	PH_EINT3
PH4	UART3_TX	SPI1_CS	CPU_CUR_W	RGMII0_TXD1/ RMII0_TXD1	PH_EINT4
PH5	UART3_RX	SPI1_CLK	LEDC	RGMII0_TXD0/ RMII0_TXD0	PH_EINT5
PH6	UART3_RTS	SPI1_MOSI		RGMII0_TXCK/ RMII0_TXCK	PH_EINT6
PH7	UART3_CTS	SPI1_MISO	OWA_OUT	RGMII0_TXCTL/ RMII0_TXEN	PH_EINT7
PH8	DMIC_CLK	SPI2_CS	I2S2_MCLK	I2S2_DIN2	PH_EINT8
PH9	DMIC_DATA0	SPI2_CLK	I2S2_BCLK	MDC0	PH_EINT9
PH10	DMIC_DATA1	SPI2_MOSI	I2S2_LRCK	MDIO0	PH_EINT10
PH11	DMIC_DATA2	SPI2_MISO	I2S2_DOUT0	I2S2_DIN1	PH_EINT11
PH12	DMIC_DATA3	TWI3_SCK	I2S2_DIN0	I2S2_DOUT1	PH_EINT12
PH13		TWI3_SDA	I2S3_MCLK	EPHY0_25	PH_EINT13
PH14			I2S3_BCLK	RGMII0_RXD3/ RMII0_NULL	PH_EINT14
PH15			I2S3_LRCK	RGMII0_RXD2/ RMII0_NULL	PH_EINT15
PH16		I2S3_DOUT0	I2S3_DIN1	RGMII0_RXCK/ RMII0_NULL	PH_EINT16
PH17		I2S3_DOUT1	I2S3_DIN0	RGMII0_TXD3/ RMII0_NULL	PH_EINT17
PH18	CIR_OUT	I2S3_DOUT2	I2S3_DIN2	RGMII0_TXD2/ RMII0_NULL	PH_EINT18
PH19	CIR_IN	I2S3_DOUT3	I2S3_DIN3	LEDC	PH_EINT19

Table 10- 23. PL Multiplex Function Select

GPIO Port	Function2	Function3	Function4	Function5	Function6
PL0	S_TWI0_SCK				S_PL_EINT0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

PL1	S_TWI0_SDA				S_PL_EINT1
PL2	S_UART_TX				S_PL_EINT2
PL3	S_UART_RX				S_PL_EINT3
PL4	S_JTAG_MS				S_PL_EINT4
PL5	S_JTAG_CK				S_PL_EINT5
PL6	S_JTAG_DO				S_PL_EINT6
PL7	S_JTAG_DI				S_PL_EINT7
PL8	S_TWI1_SCK				S_PL_EINT8
PL9	S_TWI1_SDA				S_PL_EINT9
PL10	S_PWM				S_PL_EINT10
PL11	S_CPU_CUR_W	S_CIR_IN			S_PL_EINT11

10.6.3.2. Port Function

Port Controller supports 8 GPIOs, every GPIO can configure as Input, Output, Functional Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 10- 24. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	Input function, default input is 0	/	N	Y
	Input function, default input is 1	/	Y	N
Output	Output function	Y	X	X
Disable	Pull-up	/	Y	N
	Pulll-down	/	N	Y
	High-impedance	/	N	N
Interrupt	Trigger mode	/	X	X

/: Non-configure, configuration is invalid

Y: Need configure

X: Select configuration according to actual situation

N: Forbid to configure.

10.6.3.3. Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

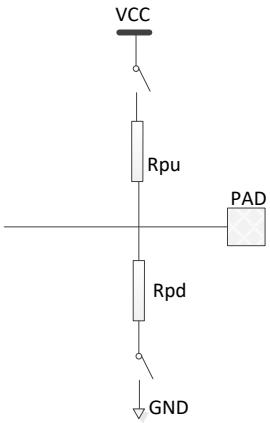


Figure 10- 34. Pull up/down Logic

High-impedance, the output is float state, all buffers are off, the level is decided by external high/low level. When high-impedance, software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the resistance value is about 100 kΩ.

The setting of pull-down input, pull-up input, high-impledance input is decided by external circuit.

10.6.3.4. Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

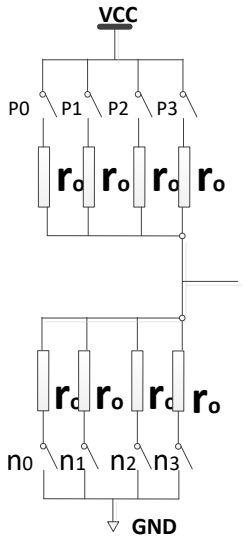


Figure 10- 35. IO Buffer Strength Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

When output high level, the n0,n1,n2,n3 of NMOS are off, the p0,p1,p2,p3 of PMOS are on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum, the impedance value is r0 (on-resistance). When buffer strength is set to 1, only p0 and p1 are on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only p0,p1 and p2 are on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, p0,p1,p2 and p3 are on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum, the impedance value is r0. When buffer strength is set to 1, only n0 and n1 are on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 are on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 are on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between the output driver circuit and the port is unconnected, the driver configuration is invalid.

10.6.3.5. Interrupt

Each group IO has independent interrupt number. IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge: When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.
- High Level : Just keep high level and the interrupt will always generate.
- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

10.6.4. Register List

Module Name	Base Address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

GPIO(PB,PC,PD,PE,PF,PG,PH)	0x0300B000

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n =1,2,3,4,5,6,7)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n =1,2,3,4,5,6,7)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n =1,2,3,4,5,6,7)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n =1,2,3,4,5,6,7)
Pn_DAT	n*0x24+0x10	Port n Data Register (n =1,2,3,4,5,6,7)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n =1,2,3,4,5,6,7)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n =1,2,3,4,5,6,7)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n =1,2,3,4,5,6,7)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n =1,2,3,4,5,6,7)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n =1,2,3,4,5,6,7)
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1 (n =1,2,3,4,5,6,7)
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2 (n =1,2,3,4,5,6,7)
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3 (n =1,2,3,4,5,6,7)
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register (n =1,2,3,4,5,6,7)
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register (n =1,2,3,4,5,6,7)
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register (n =1,2,3,4,5,6,7)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

Module Name	Base Address
GPIO(PL)	0x07022000

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n =0)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n =0)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n =0)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n =0)
Pn_DAT	n*0x24+0x10	Port n Data Register (n =0)
Pn_DRV0	n*0x24+0x14	Port n Multi_Driving Register 0 (n =0)
Pn_DRV1	n*0x24+0x18	Port n Multi_Driving Register 1 (n =0)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n =0)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n =0)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n =0)
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1 (n =0)
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2 (n =0)
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3 (n =0)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register (n =0)
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register (n =0)
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register (n =0)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

10.6.5. GPIO(PB,PC,PD,PE,PF,PG,PH) Register Description

10.6.5.1. 0x0024 PB Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0024			Register Name: PB_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PB7_SELECT 000:Input 001:Output 010:Reserved 011:I2S0_DOUT0 100:I2S0_DIN1 101:Reserved 110:PB_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PB6_SELECT 000:Input 001:Output 010:Reserved 011:I2S0_LRCK 100:JTAG_DO_GPU 101:Reserved 110:PB_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PB5_SELECT 000:Input 001:Output 010:TWI1_SDA 011:I2S0_BCLK 100:JTAG_CK_GPU 101:Reserved 110:PB_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PB4_SELECT 000:Input 001:Output 010:TWI1_SCK 011:I2S0_MCLK 100:JTAG_MS_GPU 101:Reserved 110:PB_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PB3_SELECT 000:Input 001:Output 010:UART2_CTS 011:SPI2_MISO 100:JTAG_DI 101:Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			110:PB_EINT3	111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PB2_SELECT 000:Input 010:UART2_RTS 100:JTAG_DO 110:PB_EINT2	 001:Output 011:SPI2_MOSI 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PB1_SELECT 000:Input 010:UART2_RX 100:JTAG_CK 110:PB_EINT1	 001:Output 011:SPI2_CLK 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PB0_SELECT 000:Input 010:UART2_TX 100:JTAG_MS 110:PB_EINT0	 001:Output 011:SPI2_CS 101:Reserved 111:IO Disable

10.6.5.2. 0x0028 PB Configure Register 1 (Default Value: 0x0000_0777)

Offset: 0x0028			**Register Name: PB_CFG1**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:11	/	/	/	
10:8	R/W	0x7	PB10_SELECT 000:Input 010:UART0_RX 100:PWM1 110:PB_EINT10	 001:Output 011:TWI0_SDA 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PB9_SELECT 000:Input 010:UART0_TX 100:JTAG_DI_GPU 110:PB_EINT9	 001:Output 011:TWI0_SCK 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PB8_SELECT 000:Input 010:OWA_OUT 100:I2S0_DOUT1 110:PB_EINT8	 001:Output 011:I2S0_DIN0 101:Reserved 111:IO Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.3. 0x0034 PB Data Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PB_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.4. 0x0038 PB Multi-Driving Register 0 (Default Value: 0x0015_5555)

Offset: 0x0038			Register Name: PB_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PB10_DRV PB10 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PB9_DRV PB9 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PB8_DRV PB8 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PB7_DRV PB7 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PB6_DRV PB6 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PB5_DRV PB5 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PB4_DRV PB4 Multi_Driving Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Level 0 10: Level 2	01: Level 1 11: Level 3
7:6	R/W	0x1	PB3_DRV PB3 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PB2_DRV PB2 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PB1_DRV PB1 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PB0_DRV PB0 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.6.5.5. 0x0040 PB Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PB_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:22	/	/	/	
21:20	R/W	0x0	PB10_PULL PB10 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
19:18	R/W	0x0	PB9_PULL PB9 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
17:16	R/W	0x0	PB8_PULL PB8 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
15:14	R/W	0x0	PB7_PULL PB7 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
13:12	R/W	0x0	PB6_PULL PB6 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:10	R/W	0x0	PB5_PULL PB5 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PB4_PULL PB4 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PB3_PULL PB3 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PB2_PULL PB2 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PB1_PULL PB1 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PB0_PULL PB0 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

10.6.5.6. 0x0048 PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:SPI0_CS1 101:Reserved 110:PC_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT 000:Input 001:Output 010:NAND_RB0 011:SDC2_CMD 100:Reserved 101:Reserved 110:PC_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			000:Input	001:Output
			010:NAND_RE	011:SDC2_CLK
			100:Reserved	101:Reserved
			110:PC_EINT5	111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000:Input 010:NAND_CE0 100:SPI0_MISO 110:PC_EINT4	 001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000:Input 010:NAND_CE1 100:SPI0_CS0 110:PC_EINT3	 001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:NAND_CLE 100:SPI0_MOSI 110:PC_EINT2	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:NAND_ALE 100:Reserved 110:PC_EINT1	 001:Output 011:SDC2_RST 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input 010:NAND_WE 100:Reserved 110:PC_EINT0	 001:Output 011:SDC2_DS 101:Reserved 111:IO Disable

10.6.5.7. 0x004C PC Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x004C			**Register Name: PC_CFG1**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC15_SELECT 000:Input 010:NAND_DQ1	 001:Output 011:SDC2_D2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100:SPI0_WP	101:Reserved
			110:PC_EINT15	111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC14_SELECT 000:Input 010:NAND_DQ2 100:Reserved 110:PC_EINT14	 001:Output 011:SDC2_D6 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC13_SELECT 000:Input 010:NAND_DQ3 100:Reserved 110:PC_EINT13	 001:Output 011:SDC2_D1 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC12_SELECT 000:Input 010:NAND_DQS 100:SPI0_CLK 110:PC_EINT12	 001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC11_SELECT 000:Input 010:NAND_DQ4 100:Reserved 110:PC_EINT11	 001:Output 011:SDC2_D5 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC10_SELECT 000:Input 010:NAND_DQ5 100:Reserved 110:PC_EINT10	 001:Output 011:SDC2_D0 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC9_SELECT 000:Input 010:NAND_DQ6 100:Reserved 110:PC_EINT9	 001:Output 011:SDC2_D4 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC8_SELECT 000:Input 010:NAND_DQ7 100:Reserved 110:PC_EINT8	 001:Output 011:SDC2_D3 101:Reserved 111:IO Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.8. 0x0050 PC Configure Register 2 (Default Value: 0x0000_0007)

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_DQ0 011:SDC2_D7 100:SPI0_HOLD 101:Reserved 110:PC_EINT16 111:IO Disable

10.6.5.9. 0x0058 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.10. 0x005C PC Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PC15_DRV PC15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PC14_DRV PC14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PC13_DRV PC13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PC12_DRV PC12 Multi-Driving Select 00: Level 0 01: Level 1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Level 2	11: Level 3
23:22	R/W	0x1	PC11_DRV PC11 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
21:20	R/W	0x1	PC10_DRV PC10 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
19:18	R/W	0x1	PC9_DRV PC9 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
17:16	R/W	0x1	PC8_DRV PC8 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	PC7_DRV PC7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PC6_DRV PC6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PC5_DRV PC5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PC2_DRV PC2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.6.5.11. 0x0060 PC Multi-Driving Register 1 (Default Value: 0x0000_0001)

Offset: 0x0060			Register Name: PC_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	PC16_DRV PC16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.6.5.12. 0x0064 PC Pull Register 0 (Default Value: 0x0000_5140)

Offset: 0x0064			Register Name: PC_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PC15_PULL PC15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PC14_PULL PC14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Pull-down	11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x1	PC7_PULL PC7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x1	PC6_PULL PC6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PC5_PULL PC5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.13. 0x0068 PC Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: PC_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	PC16_PULL PC16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.6.5.14. 0x006C PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000:Input 001:Output 010:LCD_D11 011:LVDS0_CKN 100:DSI_DM2 101:Reserved 110:PD_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:LCD_D10 011:LVDS0_CKP 100:DSI_DP2 101:Reserved 110:PD_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000:Input 001:Output 010:LCD_D7 011:LVDS0_D2N 100:DSI_CKM 101:Reserved 110:PD_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000:Input 001:Output 010:LCD_D6 011:LVDS0_D2P 100:DSI_CKP 101:Reserved 110:PD_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD3_SELECT 000:Input 001:Output 010:LCD_D5 011:LVDS0_D1N 100:DSI_DM1 101:Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			110:PD_EINT3	111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000:Input 010:LCD_D4 100:DSI_DP1 110:PD_EINT2	 001:Output 011:LVDS0_D1P 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000:Input 010:LCD_D3 100:DSI_DM0 110:PD_EINT1	 001:Output 011:LVDS0_D0N 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000:Input 010:LCD_D2 100:DSI_DP0 110:PD_EINT0	 001:Output 011:LVDS0_D0P 101:Reserved 111:IO Disable

10.6.5.15. 0x0070 PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD15_SELECT 000:Input 010:LCD0_D21 100:UART3_RX 110:PD_EINT15	 001:Output 011:LVDS1_D2N 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD14_SELECT 000:Input 010:LCD0_D20 100:UART3_TX 110:PD_EINT14	 001:Output 011:LVDS1_D2P 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000:Input 010:LCD0_D19 100:SPI1_MISO 110:PD_EINT13	 001:Output 011:LVDS1_D1N 101:Reserved 111:IO Disable
19	/	/	/	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

18:16	R/W	0x7	PD12_SELECT 000:Input 010:LCD_D18 100:SPI1_MOSI 110:PD_EINT12	 001:Output 011:LVDS1_D1P 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000:Input 010:LCD0_D15 100:SPI1_CLK 110:PD_EINT11	 001:Output 011:LVDS1_D0N 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD10_SELECT 000:Input 010:LCD0_D14 100:SPI1_CS 110:PD_EINT10	 001:Output 011:LVDS1_D0P 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD9_SELECT 000:Input 010:LCD0_D13 100:DSI_DM3 110:PD_EINT9	 001:Output 011: LVDS0_D3N 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD8_SELECT 000:Input 010:LCD0_D12 100:DSI_DP3 110:PD_EINT8	 001:Output 011:LVDS0_D3P 101:Reserved 111:IO Disable

10.6.5.16. 0x0074 PD Configure Register 2 (Default Value: 0x7777_7777)

Offset: 0x0074			**Register Name: PD_CFG2**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD23_SELECT 000:Input 010:PWM0 100:TWI0_SDA 110:PD_EINT23	 001:Output 011:Reserved 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000:Input	 001:Output

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010:PWM1 100:TWI0_SCK 110:PD_EINT22	011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000:Input 010:LCD0_VSYNC 100:UART4_CTS 110:PD_EINT21	 001:Output 011:PWM3 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000:Input 010:LCD0_HSYNC 100:UART4_RTS 110:PD_EINT20	 001:Output 011:PWM2 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000:Input 010:LCD0_DE 100:UART4_RX 110:PD_EINT19	 001:Output 011:LVDS1_D3N 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000:Input 010:LCD0_CLK 100:UART4_TX 110:PD_EINT18	 001:Output 011:LVDS1_D3P 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000:Input 010:LCD0_D23 100:UART3_CTS 110:PD_EINT17	 001:Output 011:LVDS1_CKN/PLL_TEST_CKN 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD16_SELECT 000:Input 010:LCD0_D22 100:UART3_RTS 110:PD_EINT16	 001:Output 011:LVDS1_CKP/PLL_TEST_CKP 101:Reserved 111:IO Disable

10.6.5.17. 0x007C PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C	Register Name: PD_DAT

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.18. 0x0080 PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PD15_DRV PD15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PD14_DRV PD14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PD13_DRV PD13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PD12_DRV PD12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PD11_DRV PD11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PD10_DRV PD10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PD9_DRV PD9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 01: Level 1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Level 2 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD5_DRV PD5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD3_DRV PD3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD0_DRV PD0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.6.5.19. 0x0084 PD Multi-Driving Register 1 (Default Value: 0x0000_5555)

Offset: 0x0084			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x1	PD23_DRV PD23 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD22_DRV

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			PD22 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD17_DRV PD17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD16_DRV PD16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.6.5.20. 0x0088 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PD15_PULL PD15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

25:24	R/W	0x0	PD12_PULL PD12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD1_PULL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.6.5.21. 0x008C PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x0	PD23_PULL PD23 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD22_PULL PD22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Pull-down	11: Reserved

10.6.5.22. 0x0090 PE Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE7_SELECT 000:Input 010:CSI_SM_VS 100:I2S2_LRCK 110:PE_EINT7	 001:Output 011:BIST_RESULT1 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PE6_SELECT 000:Input 010:Reserved 100:I2S2_BCLK 110:PE_EINT6	 001:Output 011:BIST_RESULT0 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PE5_SELECT 000:Input 010:MIPI_MCLK1 100:I2S2_MCLK 110:PE_EINT5	 001:Output 011:PLL_LOCK_DBG 101:LEDC 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PE4_SELECT 000:Input 010:TWI3_SDA 100:Reserved 110:PE_EINT4	 001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PE3_SELECT 000:Input 010:TWI3_SCK 100:Reserved 110:PE_EINT3	 001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PE2_SELECT 000:Input 010:TWI2_SDA 100:Reserved 110:PE_EINT2	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

6:4	R/W	0x7	PE1_SELECT 000:Input 010:TWI2_SCK 100:Reserved 110:PE_EINT1	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PE0_SELECT 000:Input 010:MIPI_MCLK0 100:Reserved 110:PE_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

10.6.5.23. 0x0094 PE Configure Register 1 (Default Value: 0x0000_0077)

Offset: 0x0094			Register Name: PE_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:7	/	/	/	
6:4	R/W	0x7	PE9_SELECT 000:Input 010:Reserved 100:I2S2_DIN0 110:PE_EINT9	 001:Output 011:BIST_RESULT3 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PE8_SELECT 000:Input 010:Reserved 100:I2S2_DOUT0 110:PE_EINT8	 001:Output 011:BIST_RESULT2 101:Reserved 111:IO Disable

10.6.5.24. 0x00A0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.25. 0x00A4 PE Multi-Driving Register 0 (Default Value: 0x0005_5555)

Offset: 0x00A4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x1	PE9_DRV PE9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PE8_DRV PE8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PE7_DRV PE7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PE6_DRV PE6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PE5_DRV PE5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE4_DRV PE4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE3_DRV PE3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PE2_DRV PE2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PE1_DRV PE1 Multi-Driving Select 00: Level 0--180Ω 01: Level 1--120Ω 10: Level 2--100Ω 11: Level 3--50Ω
1:0	R/W	0x1	PE0_DRV PE0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.26. 0x00AC PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	PE9_PULL PE9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull-up/down Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Pull-up/down disable	01: Pull-up
			10: Pull-down	11: Reserved

10.6.5.27. 0x00B4 PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PF6_SELECT 000:Input 010:Reserved 100:Reserved 110:PF_EINT6	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PF5_SELECT 000:Input 010:SDC0_D2 100:JTAG_CK_GPU 110:PF_EINT5	 001:Output 011:JTAG_CK 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PF4_SELECT 000:Input 010:SDC0_D3 100:Reserved 110:PF_EINT4	 001:Output 011:UART0_RX 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PF3_SELECT 000:Input 010:SDC0_CMD 100:JTAG_DO_GPU 110:PF_EINT3	 001:Output 011:JTAG_DO 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000:Input 010:SDC0_CLK 100:Reserved 110:PF_EINT2	 001:Output 011:UART0_TX 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000:Input 010:SDC0_D0 100:JTAG_DI_GPU 110:PF_EINT1	 001:Output 011:JTAG_DI 101:Reserved 111:IO Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS 100:JTAG_MS_GPU 101:Reserved 110:PF_EINT0 111:IO Disable

10.6.5.28. 0x00C4 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.29. 0x00C8 PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV PF2 Multi-Driving Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Level 0--180Ω 10: Level 2--100Ω	01: Level 1--120Ω 11: Level 3--50Ω
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PF0_DRV PF0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.6.5.30. 0x00D0 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:14	/	/	/	
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.31. 0x00D8 PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PG7_SELECT 000:Input 010:UART1_RX 100:Reserved 110:PG_EINT7	001:Output 011:Reserved 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PG6_SELECT 000:Input 010:UART1_TX 100:Reserved 110:PG_EINT6	001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PG5_SELECT 000:Input 010:SDC1_D3 100:Reserved 110:PG_EINT5	001:Output 011:Reserved 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG4_SELECT 000:Input 010:SDC1_D2 100:Reserved 110:PG_EINT4	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG3_SELECT 000:Input 010:SDC1_D1 100:Reserved 110:PG_EINT3	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG2_SELECT 000:Input 010:SDC1_D0 100:Reserved 110:PG_EINT2	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG1_SELECT	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			000:Input	001:Output
			010:SDC1_CMD	011:Reserved
			100:Reserved	101:Reserved
			110:PG_EINT1	111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000:Input 010:SDC1_CLK 100:Reserved 110:PG_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

10.6.5.32. 0x00DC PG Configure Register 1 (Default Value: 0x0077_7777)

Offset: 0x00DC			Register Name: PG_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
22:20	R/W	0x7	PG13_SELECT 000:Input 010:Reserved 100:I2S1_DOUT1 110:PG_EINT13	 001:Output 011:I2S1_DIN0 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG12_SELECT 000:Input 010:Reserved 100:I2S1_DIN1 110:PG_EINT12	 001:Output 011:I2S1_DOUT0 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG11_SELECT 000:Input 010:Reserved 100:Reserved 110:PG_EINT11	 001:Output 011:I2S1_LRCK 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG10_SELECT 000:Input 010:Reserved 100:Reserved 110:PG_EINT10	 001:Output 011:I2S1_BCLK 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG9_SELECT 000:Input 010:UART1_CTS	 001:Output 011:I2S1_MCLK

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100:Reserved 110:PG_EINT9	101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG8_SELECT 000:Input 010:UART1_RTS 100:Reserved 110:PG_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

10.6.5.33. 0x00E8 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.34. 0x00EC PG Multi-Driving Register 0 (Default Value: 0x0555_5555)

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:26	R/W	0x1	PG13_DRV PG13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PG12_DRV PG12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PG11_DRV PG11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PG10_DRV PG10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

19:18	R/W	0x1	PG9_DRV PG9 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
17:16	R/W	0x1	PG8_DRV PG8 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PG6_DRV PG6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PG5_DRV PG5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PG3_DRV PG3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0--180Ω 10: Level 2--100Ω	 01: Level 1--120Ω 11: Level 3--50Ω

10.6.5.35. 0x00F4 PG Pull Register 0 (Default Value: 0x0000_0554)

Offset: 0x00F4	Register Name: PG_PULL0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x0	PG13_PULL PG13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x1	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x1	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x1	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Pull-down	11: Reserved
5:4	R/W	0x1	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.6.5.36. 0x00FC PH Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00FC			Register Name: PH_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH7_SELECT 000:Input 010:UART3_CTS 100:OWA_OUT 110:PH_EINT7	 001:Output 011:SPI1_MISO 101:RGMII0_TXCTL/RMII0_TXEN 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH6_SELECT 000:Input 010:UART3_RTS 100:Reserved 110:PH_EINT6	 001:Output 011:SPI1_MOSI 101:RGMII0_TXCK/RMII0_TXCK 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH5_SELECT 000:Input 010:UART3_RX 100:LEDC 110:PH_EINT5	 001:Output 011:SPI1_CLK 101:RGMII0_TXD0/RMII_TXD0 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH4_SELECT 000:Input 010:UART3_TX 100:CPU_CUR_W 110:PH_EINT4	 001:Output 011:SPI1_CS 101:RGMII0_TXD1/RMII0_TXD1 111:IO Disable
15	/	/	/	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

14:12	R/W	0x7	PH3_SELECT 000:Input 010:TWI1_SDA 100:Reserved 110:PH_EINT3	001:Output 011:CIR_OUT 101:RGMII0_CLKIN/RMII0_RXER 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000:Input 010:TWI1_SCK 100:Reserved 110:PH_EINT2	001:Output 011:CPU_CUR_W 101:RGMII0_RXCTL/RMII0_CRS_DV 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000:Input 010:TWI0_SDA 100:Reserved 110:PH_EINT1	001:Output 011:Reserved 101:RGMII0_RXD0/RMII0_RXD0 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000:Input 010:TWI0_SCK 100:Reserved 110:PH_EINT0	001:Output 011:Reserved 101:RGMII0_RXD1/RMII0_RXD1 111:IO Disable

10.6.5.37. 0x0100 PH Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0100			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH15_SELECT 000:Input 010:Reserved 100:I2S3_LRCK 110:PH_EINT15	001:Output 011:Reserved 101:RGMII0_RXD2/RMII0_NULL 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH14_SELECT 000:Input 010:Reserved 100:I2S3_BCLK 110:PH_EINT14	001:Output 011:Reserved 101:RGMII0_RXD3/RMII0_NULL 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH13_SELECT 000:Input	001:Output

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010:Reserved 100:I2S3_MCLK 110:PH_EINT13	011:TWI3_SDA 101:EPHY0_25 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH12_SELECT 000:Input 010:DMIC_DATA3 100:I2S2_DIN0 110:PH_EINT12	 001:Output 011:TWI3_SCK 101:I2S2_DOUT1 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH11_SELECT 000:Input 010:DMIC_DATA2 100:I2S2_DOUT0 110:PH_EINT11	 001:Output 011:SPI2_MISO 101:I2S2_DIN1 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000:Input 010:DMIC_DATA1 100:I2S2_LRCK 110:PH_EINT10	 001:Output 011:SPI2_MOSI 101:MDIO0 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000:Input 010:DMIC_DATA0 100:I2S2_BCLK 110:PH_EINT9	 001:Output 011:SPI2_CLK 101:MDC0 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000:Input 010:DMIC_CLK 100:I2S2_MCLK 110:PH_EINT8	 001:Output 011:SPI2_CS 101:I2S2_DIN2 111:IO Disable

10.6.5.38. 0x0104 PH Configure Register 2 (Default Value: 0x0000_7777)

Offset: 0x0104			Register Name: PH_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:15	/	/	/	
14:12	R/W	0x7	PH19_SELECT 000:Input 010:CIR_IN 100:I2S3_DIN3	 001:Output 011:I2S3_DOUT3 101:LEDC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			110:PH_EINT19	111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH18_SELECT 000:Input 010:CIR_OUT 100:I2S3_DIN2 110:PH_EINT18	 001:Output 011:I2S3_DOUT2 101:RGMII0_TXD2/RMII0_NULL 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH17_SELECT 000:Input 010:Reserved 100:I2S3_DIN0 110:PH_EINT17	 001:Output 011:I2S3_DOUT1 101:RGMII0_TXD3/RMII0_NULL 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH16_SELECT 000:Input 010:Reserved 100:I2S3_DIN1 110:PH_EINT16	 001:Output 011:I2S3_DOUT0 101:RGMII0_RXCK/RMII0_NULL 111:IO Disable

10.6.5.39. 0x010C PH Data Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.40. 0x0110 PH Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0110			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PH15_DRV PH15 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PH14_DRV PH14 Multi_Driving Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Level 0 10: Level 2	01: Level 1 11: Level 3
27:26	R/W	0x1	PH13_DRV PH13 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
25:24	R/W	0x1	PH12_DRV PH12 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
23:22	R/W	0x1	PH11_DRV PH11 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	PH7_DRV PH7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PH3_DRV PH3 Multi-Driving Select 00: Level 0	 01: Level 1

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Level 2	11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.6.5.41. 0x0114 PH Multi-Driving Register 0 (Default Value: 0x0000_0055)

Offset: 0x0114			Register Name: PH_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:8	/	/	/	
7:6	R/W	0x1	PH19_DRV PH19 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PH18_DRV PH18 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH17_DRV PH17 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PH16_DRV PH16 Multi_Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.6.5.42. 0x0118 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PH_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PH15_PULL PH15 Pull_up/down Select

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: Pull-down	11: Reserved
7:6	R/W	0x1	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x1	PH2_PULL PH2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.6.5.43. 0x011C PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PH_PULL1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:8	/	/	/	
7:6	R/W	0x0	PH19_PULL PH19 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
5:4	R/W	0x0	PH18_PULL PH18 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
3:2	R/W	0x0	PH17_PULL PH17 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved
1:0	R/W	0x0	PH16_PULL PH16 Pull_up/down Select 00: Pull_up/down disable 10: Pull_down	 01: Pull_up 11: Reserved

10.6.5.44. 0x0220 PB External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220	Register Name: PB_EINT_CFG0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

10.6.5.45. 0x0224 PB External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PB_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

10.6.5.46. 0x0230 PB External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PB_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.47. 0x0234 PB External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PB_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

10.6.5.48. 0x0218 PB External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PB_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.49. 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.50. 0x0244 PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PC_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.51. 0x0248 PC External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PC_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

10.6.5.52. 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.53. 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

10.6.5.54. 0x0258 PC External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.5.55. 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.56. 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: PD_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.57. 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			**Register Name: PD_EINT_CFG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.58. 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.59. 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.60. 0x0278 PD External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.5.61. 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PD_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.62. 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.63. 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.64. 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.65. 0x0298 PE External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.5.66. 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.67. 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.68. 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.69. 0x02B8 PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.5.70. 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.71. 0x02C4 PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: PG_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.72. 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.73. 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.74. 0x02D8 PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.75. 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.76. 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.5.77. 0x02E8 PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PH_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.5.78. 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.5.79. 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4	Register Name: PH_EINT_STATUS

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: IRQ pending Write ‘1’ to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.80. 0x02F8 PH External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.5.81. 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC_IO POWER MODE Select 0: 3.3 V 1: 1.8 V
11:10	/	/	/
9	R/W	0x0	PJ_POWER MODE Select 0: 3.3 V 1: 1.8 V If PJ_Port Power Source select VCC_IO, this bit is invalid
8	R/W	0x0	PI_POWER MODE Select 0: 3.3 V

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: 1.8 V If PI_Port Power Source select VCC_IO, this bit is invalid
7	/	/	/
6	R/W	0x0	PG_POWER MODE Select 0: 3.3 V 1: 1.8 V If PG_Port Power Source select VCC_IO, this bit is invalid
5	R/W	0x0	PF_POWER MODE Select 0: 3.3 V 1: 1.8 V If PF_Port Power Source select VCC_IO, this bit is invalid
4	R/W	0x0	PE_POWER MODE Select 0: 3.3 V 1: 1.8 V If PE_Port Power Source select VCC_IO, this bit is invalid
3	R/W	0x0	PD_POWER MODE Select 0: 3.3 V 1: 1.8 V If PD_Port Power Source select VCC_IO, this bit is invalid
2	R/W	0x0	PC_POWER MODE Select 0: 3.3 V 1: 1.8 V If PC_Port Power Source select VCC_IO, this bit is invalid
1:0	/	/	/

NOTE

When the power domain of GPIO is larger than 1.8 V, the withstand voltage is set to 3.3 V mode, the corresponding value in 0x0340 register is set to 0.

When the power domain of GPIO is 1.8 V, the withstand voltage is set to 1.8 V mode, the corresponding value in 0x0340 register is set to 1.

10.6.5.82. 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC_IO Withstand Voltage Mode Select Control 0: Enable 1: Disable
11:10	/	/	/
9	R/W	0x0	VCC_PJ Withstand Voltage Mode Select Control 0: Enable 1: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

8	R/W	0x0	VCC_PI Withstand Voltage Mode Select Control 0: Enable 1: Disable
7	/	/	/
6	R/W	0x0	VCC_PG Withstand Voltage Mode Select Control 0: Enable 1: Disable
5	R/W	0x0	VCC_PF Withstand Voltage Mode Select Control 0: Enable 1: Disable
4	R/W	0x0	VCC_PE Withstand Voltage Mode Select Control 0: Enable 1: Disable
3	R/W	0x0	VCC_PD Withstand Voltage Mode Select Control 0: Enable 1: Disable
2	R/W	0x0	VCC_PC Withstand Voltage Mode Select Control 0: Enable 1: Disable
1:0	/	/	/

NOTE

For 1.8 V and 3.3 V power, the withstand function is enabled by default, the corresponding bit in 0x0344 register is set to 0.

For 2.5 V power, the withstand function is disabled, the corresponding bit in 0x0344 register is set to 1, and the withstand mode in 0x0340 register needs be set to 3.3 V.

10.6.5.83. 0x0348 PIO Group Power Value Register(Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	VCC_IO Power Value
15:10	/	/	/
9	R	0x0	PJ_Port Power Value If PJ_Port Power Source selects VCC_IO, this bit is invalid
8	R	0x0	PI_Port Power Value If PI_Port Power Source selects VCC_IO, this bit is invalid
7	/	/	/
6	R	0x0	PG_Port Power Value If PG_Port Power Source selects VCC_IO, this bit is invalid
5	R	0x0	PF_Port Power Value

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			If PF_Port Power Source selects VCC_IO, this bit is invalid
4	R	0x0	PE_Port Power Value If PE_Port Power Source selects VCC_IO, this bit is invalid
3	R	0x0	PD_Port Power Value If PD_Port Power Source selects VCC_IO, this bit is invalid
2	R	0x0	PC_Port Power Value If PC_Port Power Source selects VCC_IO, this bit is invalid
1:0	/	/	/

NOTE

When the reading value of the 0x0348 register is 0, it indicates that IO power voltage is greater than 2.5 V.
When the reading value of the 0x0348 register is 1, it indicates that IO power voltage is less than 2.0 V.

10.6.5.84. 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: PIO_PV_SEL_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	VCC-PF Power Voltage Select Control 0: 1.8 V 1: 3.3 V

10.6.6. GPIO(PL) Register Description

10.6.6.1. 0x0000 PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			Register Name: PL_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PL7_SELECT 000:Input 010:S_JTAG_DI 100:Reserved 110:S_PL_EINT7	 001:Output 011:Reserved 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PL6_SELECT 000:Input 010:S_JTAG_DO 100:Reserved 110:S_PL_EINT6	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

22:20	R/W	0x7	PL5_SELECT 000:Input 010:S_JTAG_CK 100:Reserved 110:S_PL_EINT5	001:Output 011:Reserved 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PL4_SELECT 000:Input 010:S_JTAG_MS 100:Reserved 110:S_PL_EINT4	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PL3_SELECT 000:Input 010:S_UART_RX 100:Reserved 110:S_PL_EINT3	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL2_SELECT 000:Input 010:S_UART_TX 100:Reserved 110:S_PL_EINT2	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL1_SELECT 000:Input 010:S_TWI0_SDA 100:Reserved 110:S_PL_EINT1	001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL0_SELECT 000:Input 010:S_TWI0_SCK 100:Reserved 110:S_PL_EINT0	001:Output 011:Reserved 101:Reserved 111:IO Disable

10.6.6.2. 0x0004 PL Configure Register 1 (Default Value: 0x0000_7777)

Offset: 0x0004			Register Name: PL_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:15	/	/	/	
14:12	R/W	0x7	PL11_SELECT 000:Input	001:Output

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010:S_CPU_CUR_W 100:Reserved 110:S_PL_EINT11	011:S_CIR_IN 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL10_SELECT 000:Input 010:S_PWM 100:Reserved 110:S_PL_EINT10	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL9_SELECT 000:Input 010:S_TWI1_SDA 100:Reserved 110:S_PL_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL8_SELECT 000:Input 010:S_TWI1_SCK 100:Reserved 110:S_PL_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

10.6.6.3. 0x0010 PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.4. 0x0014 PL Multi-Driving Register 0 (Default Value: 0x0055_5555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x1	PL11_DRV PL11 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

21:20	R/W	0x1	PL10_DRV PL10 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PL9_DRV PL9 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PL8_DRV PL8 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PL7_DRV PL7 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PL6_DRV PL6 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PL5_DRV PL5 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PL4_DRV PL4 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PL3_DRV PL3 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PL2_DRV PL2 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PL1_DRV PL1 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PL0_DRV PL0 Multi_Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.6.6.5. 0x001C PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x0	PL11_PULL PL11 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PL10_PULL PL10 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:2	R/W	0x1	PL1_PULL PL1 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull_up/down Select 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved

10.6.6.6. 0x0200 PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name:PL_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative)

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.6.7. 0x0204 PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/Negative) Others: Reserved

10.6.6.8. 0x0210 PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.6.6.9. 0x0214 PL External Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.10. 0x0218 PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz(OSC24M)

10.6.6.11. 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC_IO POWER MODE Select 0: 3.3 V 1: 1.8 V
11:1	/	/	/
0	R/W	0x0	PL_POWER MODE Select 0: 3.3 V 1: 1.8 V

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			If PL_Port Power Source selects VCC_IO, this bit is invalid.

NOTE

When the power domain of GPIO is larger than 1.8 V, the withstand voltage is set to 3.3 V mode, the corresponding value in 0x0340 register is set to 0.

When the power domain of GPIO is 1.8 V, the withstand voltage is set to 1.8 V mode, the corresponding value in 0x0340 register is set to 1.

10.6.6.12. 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	VCC_PL Withstand Voltage Mode Select Control 0: Enable 1: Disable

NOTE

For 1.8 V and 3.3 V power, the withstand function is enabled by default, the corresponding bit in 0x0344 register is set to 0.

For 2.5 V power, the withstand function is disabled, the corresponding bit in 0x0344 register is set to 1, and the withstand mode in 0x0340 register needs be set to 3.3 V.

10.6.6.13. 0x0348 PIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	VCC_IO Power Value
15:1	/	/	/
0	R	0x0	PL_Port Power Value If PL_Port Power Source select VCC_IO,this bit is invalid

NOTE

When the reading value of the 0x0348 register is 0, it indicates that IO power voltage is greater than 2.5 V.

When the reading value of the 0x0348 register is 1, it indicates that IO power voltage is less than 2.0 V.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.7. GPADC

10.7.1. Overview

The General Purpose ADC(GPADC) is one analog to digital converter with 12-bit sampling resolution. This ADC is a type of successive approximation register (SAR) converter.

The GPADC has the following features:

- 12-bit resolution
- 8-bit effective SAR type A/D converter
- 64 FIFO depth of data register
- Power reference voltage: 1.8 V, analog input voltage range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports DMA transport
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

10.7.2. Block Diagram

Figure 10-36 shows the block diagram of the GPADC.

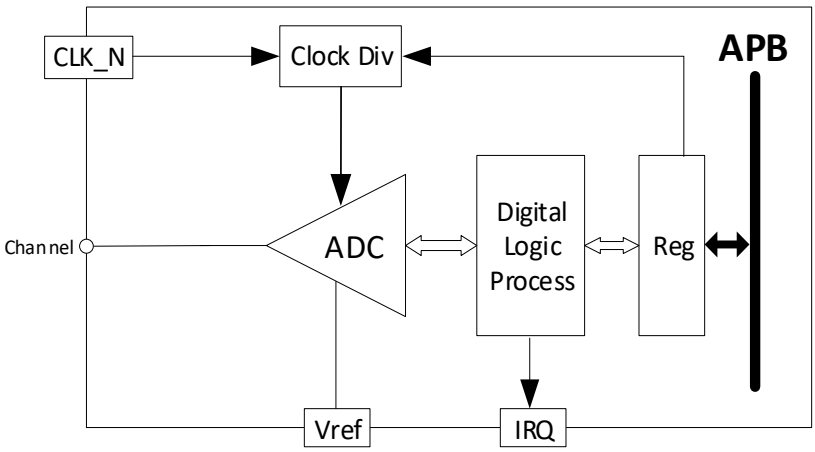


Figure 10- 36. GPADC Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.7.3. Operations and Functional Descriptions

10.7.3.1. External Signals

Table 10-25 describes the external signals of GPADC.

Table 10- 25. GPADC External Signals

Signal	Description	Type
GPADC1	ADC Input Channel	AI

10.7.3.2. Clock Sources

GPADC has one clock source. Table 10-26 describes the clock source for GPADC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 10- 26. GPADC Clock Sources

Clock Sources	Description
OSC24M	24MHz

10.7.3.3. GPADC Work Mode

(1).Single conversion mode

GPADC completes one conversion in specified channel, the converted data is updated at the data register of corresponding channel.

(2).Continuous conversion mode

GPADC has continuous conversion in specified channel until the software stops, the converted data is updated at the data register of corresponding channel.

(3).Burst conversion mode

GPADC samples and converts in the specified channel, and sequentially stores the results in FIFO.

10.7.3.4. Clock and Timing Requirements

CLK_IN = 24 MHz
CONV_TIME(Conversion Time) = 1/(24 MHz/14 Cycles) =0.583 (us)
TACQ> 10RC (R is output impedance of ADC sample circuit, C= 6.4 pF)
ADC Sample Frequency > TACQ+CONV_TIME

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

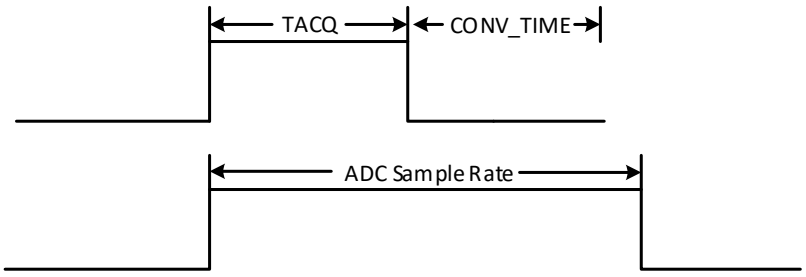


Figure 10- 37. GPADC Clock and Timing Requirement

10.7.3.5. GPADC Calculate Formula

GPADC calculate formula: GPADC_DATA = Vin/V_{REF}*4096
Where:
V_{REF}=1.8 V

10.7.4. Programming Guidelines

The GPADC initial process is as follows.

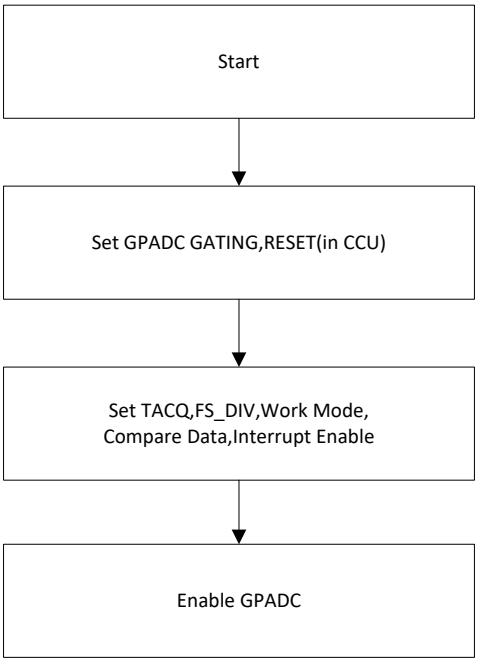


Figure 10- 38. GPADC Initial Process

10.7.5. Register List

Module Name	Base Address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

GPADC	0x05070000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register

10.7.6. Register Description

10.7.6.1. 0x0000 GPADC Sample Rate Configure Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF	FS_DIV ADC sample frequency divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC acquire time CLK_IN/(N+1) Default value: 2us

10.7.6.2. 0x0004 GPADC Control Register (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/ W	0x0	ADC_FIRST_DLY ADC First Convert Delay Setting ADC conversion of each channel is delayed by N samples.
23	R/ W	0x1	ADC_AUTOCALI_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 01: Reserved 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: Start Calibration, it is cleared to 0 after calibration
16	R/W	0x0	ADC_EN ADC Function Enable Before the bit is enabled, configure ADC parameters including the work mode and channel number,etc. 0: Disable 1: Enable **Note: If selecting single conversion mode, when the conversion is completed, the bit can clear to 0 automatically.**
15:0	/	/	/

10.7.6.3. 0x0008 GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: GP_CS_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16:2	/	/	/
1	R/W	0x0	ADC_CH1_SELECT Analog Input Channel 1 Select 0: Disable 1: Enable
0	/	/	/

10.7.6.4. 0x000C GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)

Offset: 0x000C	**Register Name: GP_FIFO_INTC**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	FIFO_DATA_DRQ_EN ADC FIFO Date DRQ Enable 0: Disable 1: Enable
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/WAC	0x0	FIFO_FLUSH ADC FIFO Flush Write ‘1’ to flush TX FIFO, clear automatically to ‘0’.
3:0	/	/	/

10.7.6.5. 0x0010 GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING ADC FIFO Overrun IRQ Pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt.
16	R/W1C	0x0	FIFO_DATA_PENDING ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write ‘1’ to clear this interrupt.
15:14	/	/	/
13:8	R	0x0	RXA_CNT ADC FIFO Available Sample Word Counter
7:0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.7.6.6. 0x0014 GPADC FIFO Data Register

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	UDF	GP_FIFO_DATA GPADC Data in FIFO

10.7.6.7. 0x0018 GPADC Calibration Data Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	GP_CDATA GPADC Calibration Data

10.7.6.8. 0x0020 GPADC Low Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_LOW_IRQ_EN 0: Disable 1: Enable
0	/	/	/

10.7.6.9. 0x0024 GPADC High Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_HIG_IRQ_EN 0: Disable 1: Enable
0	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.7.6.10. 0x0028 GPADC DATA Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_DATA_IRQ_EN 0: Disable 1: Enable
0	/	/	/

10.7.6.11. 0x0030 GPADC Low Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_LOW_PENGDING 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	/	/	/

10.7.6.12. 0x0034 GPADC High Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_HIG_PENGDING 0: No Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	/	/	/

10.7.6.13. 0x0038 GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_DATA_PENGDING 0: No Pending IRQ 1: Channel 1 Data Available Pending IRQ

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
0	/	/	/

10.7.6.14. 0x0044 GPADC CH1 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

10.7.6.15. 0x0084 GPADC CH1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.8. LRADC

10.8.1. Overview

The Low Rate ADC(LRADC) is 6-bit resolution for Key application. The LRADC can work up to maximum conversion rate of 2 kHz.

- Power supply voltage:1.8 V; reference voltage:1.35 V
- Interrupt support
- Support Hold Key and General Key
- Support normal, continue and single work mode
- 6-bits resolution, sample rate up to 2 kHz
- Voltage input range between 0 to 1.35 V

10.8.2. Block Diagram

Figure 10-39 shows a block diagram of the LRADC.

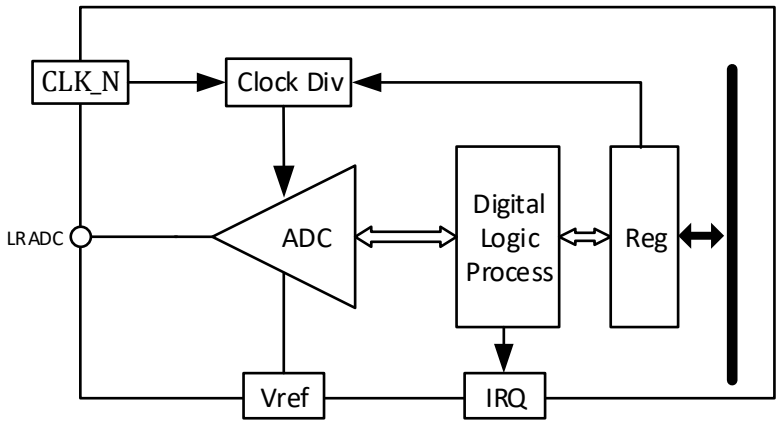


Figure 10- 39. LRADC Block Diagram

10.8.3. Operations and Functional Descriptions

10.8.3.1. External Signals

Table 10-27 describes the external signal of LRADC.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 10- 27. LRADC External Signals

Signal	Description	Type
LRADC	ADC Input	AI

10.8.3.2. Clock Sources

Table 10-28 describes the clock source for LRADC.

Table 10- 28. LRADC Clock Sources

Clock Sources	Description
LOSC	32.768 kHz LOSC

10.8.3.3. LRADC Work Mode

(1). Normal Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled. It is sampled repeatedly according to this mode until ADC stop.

(2). Continue Mode

ADC gathers 8 samples every other 8*(N+1) sample cycle. The average of every 8 samples is updated in the data register, and the data interrupt sign is enabled. (N is defined in the bit[19:16] of **LRADC_CTRL_REG**).

(3).Single Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled, since then ADC stops sample.

10.8.3.4. Interrupt

Each LRADC channel has five interrupt sources and five interrupt enable controls.

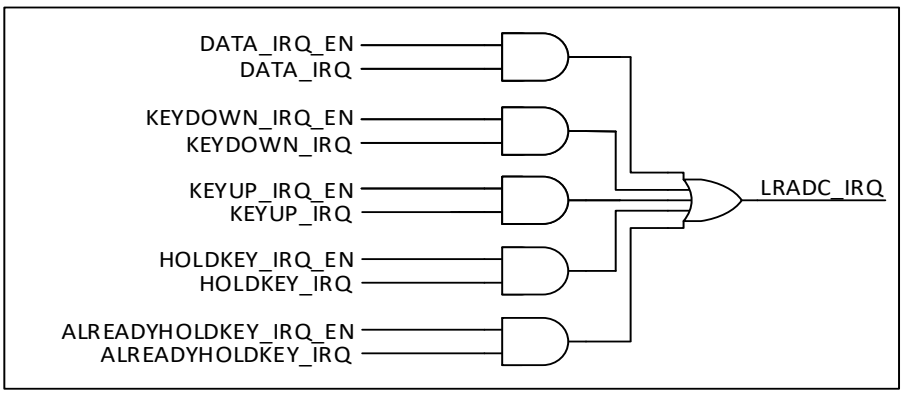


Figure 10- 40. LRADC Interrupt

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

When input voltage is between LEVELA(1.35V) and LEVELB(control by the bit[5:4] of LRADC_CTRL), IRQ1 can be generated. When input voltage is lower than LEVELB, IRQ2 can be generated.

If the controller receives IRQ1, and does not receive IRQ2 at some time, then the controller will generate Hold KEY Interrupt, otherwise DATA_IRQ Interrupt.

Hold KEY usually is used for self-locking key. When self-locking key holds locking status, the controller receives IRQ2, then the controller will generate Already Hold Key Interrupt.

10.8.4. Programming Guidelines

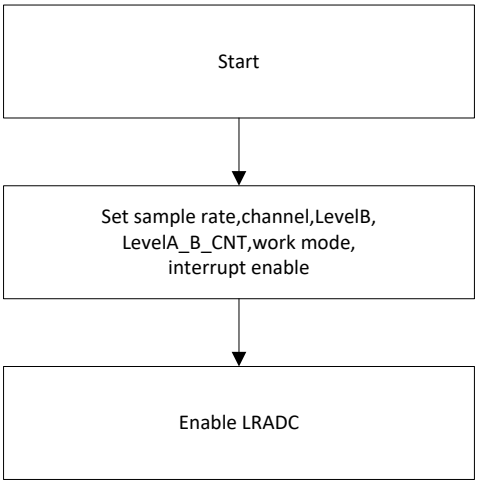


Figure 10- 41. LRADC Initial Process

(1) Set CONTINUE_TIME_SELECT(the bit[11:8] of LRADC_CTRL) when LRADC works in continue mode.

(2) The range of input voltage is from 0 to LEVELB(the bit[5:4] of LRADC_CTRL).

(3) Calculation formula: LRADC_DATA = Vin/V_{REF}*64, V_{REF}=1.35 V

(4) LRADC has 6-bit resolution, 1-bit offset error, 1-bit quantizing error. After LRADC calibrates 1-bit offset error, LRADC has 5-bit resolution.

10.8.5. Register List

Module Name	Base Address
LRADC	0x05070800

Register Name	Offset	Description
LRADC_CTRL	0x0000	LRADC Control Register
LRADC_INTC	0x0004	LRADC Interrupt Control Register
LRADC_INTS	0x0008	LRADC Interrupt Status Register
LRADC_DATA0	0x000C	LRADC Data Register0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.8.6. Register Description

10.8.6.1. 0x0000 LRADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 24	R/W	0x1	FIRST_CONVERT_DLY ADC First Convert Delay Setting ADC conversion is delayed by n samples.
23:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT Continue Mode Time Select One of 8*(N+1) sample as a valuable sample data.
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT Key Mode Select 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples.
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC Hold KEY Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_CHANNEL_EN LRADC Channel Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value Setting (the real voltage value) 00: 0x3C (1.266 V) 01: 0x39 (1.202 V) 10: 0x36 (1.139 V) 11: 0x33 (1.076 V)
3: 2	R/W	0x2	LRADC_SAMPLE_RATE LRADC Sample Rate 00: 2 kHz 01: 1 kHz 10: 500 Hz 11: 250 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN LRADC Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable

10.8.6.2. 0x0004 LRADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LRADC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold Key IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable

10.8.6.3. 0x0008 LRADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LRADC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When general key is pulled up, and the corresponding interrupt is enabled, the status bit is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When general key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING ADC0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

10.8.6.4. 0x000C LRADC Data Register0 (Default Value: 0x0000_003F)

Offset: 0x000C			**Register Name: LRADC_DATA0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x3F	LRADC0_DATA LRADC0 Data

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9. CIR Receiver

10.9.1. Overview

The Consumer Infrared(CIR) receiver is a capturer of the pulse from IR Receiver module and uses Run-Length Code (RLC) to encode the pulse. The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

In the air, there is always some noise. One threshold can be set to filter the noise to reduce system loading and improve the system stability.

The CIR receiver has the following features:

- Full physical layer implementation
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Programmable FIFO thresholds
- Interrupt support
- Sample clock up to 1 MHz

10.9.2. Block Diagram

Figure 10-42 shows a block diagram of the CIR receiver.

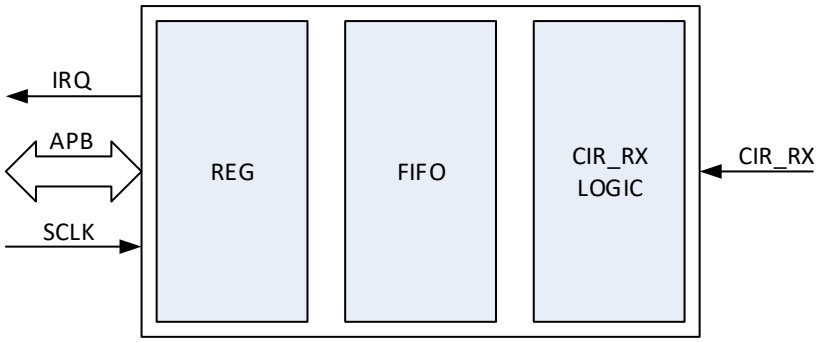


Figure 10- 42. CIR Receiver Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.3. Operations and Functional Descriptions

10.9.3.1. External Signals

Table 10-29 describes the external signals of CIR Receiver.

Table 10- 29. CIR Receiver External Signals

Signal	Description	Type
CIR_IN	Consumer infrared receiver in CPUX	I
S_CIR_IN	Consumer infrared receiver in CPUS	I

10.9.3.2. Clock Sources

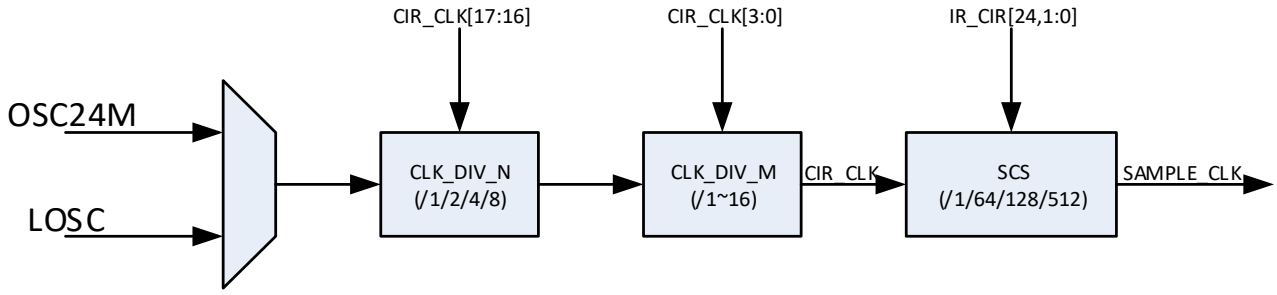


Figure 10- 43. CIR Receiver Clock

10.9.3.3. Typical Application

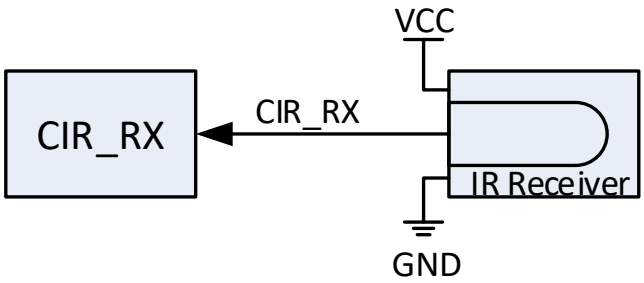


Figure 10- 44. CIR Receiver Application Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.3.4. Function Implementation

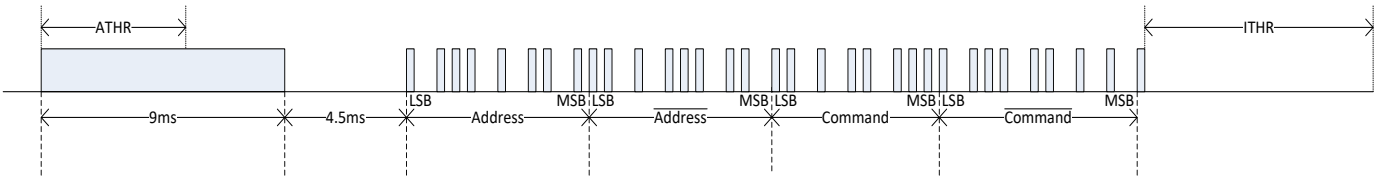


Figure 10- 45. NEC Protocol

In fact, CIR receiver module is a timer with capture function.

When CIR_RX signals satisfy ATHR (Active Threshold), CIR receiver can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. When CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of Run-Length Code. The MSB bit of a byte is polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as basic unit. This is the code form of RLC-Byte. When the level changes or the pulse width counting overflows, RLC-Byte is buffered to FIFO. The CIR_RX module receives infrared signals transmitted by the infrared remote control, the software decodes the signals.

10.9.3.5. Operating Mode

- **Sample Clock**

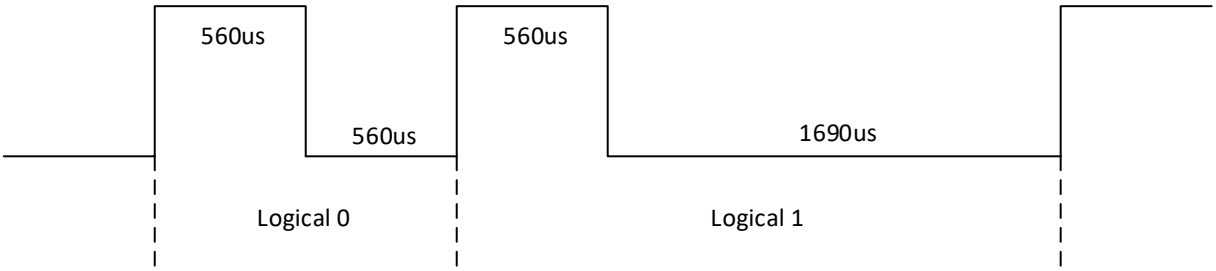


Figure 10- 46. Logical '0' and Logical '1' of NEC Protocol

For NEC protocol, a logical "1" takes 2.25ms(560us+1680us) to transmit, while a logical "0" is only half of that, being 1.12ms(560us+560us). For example, if sample clock is 31.25 kHz, a sample cycle is 32us, then 18 sample cycles are 560us. So the RLC of 560us low level is 0x12(b'00010010), the RLC of 560us high level is 0x92(b' 10010010). Then a logical "1" takes code 0x12(b'00010010) and code 0xb5(b' 10110101) to transmit, a logical "0" takes code 0x12 and code 0x92 to transmit.

- **ATHR(Active Threshold)**

When CIR receiver is in Idle state, if electrical level of CIR_RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then CIR takes the starting of the signal as a lead code, turns into active state and starts to capture CIR_RX signals.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

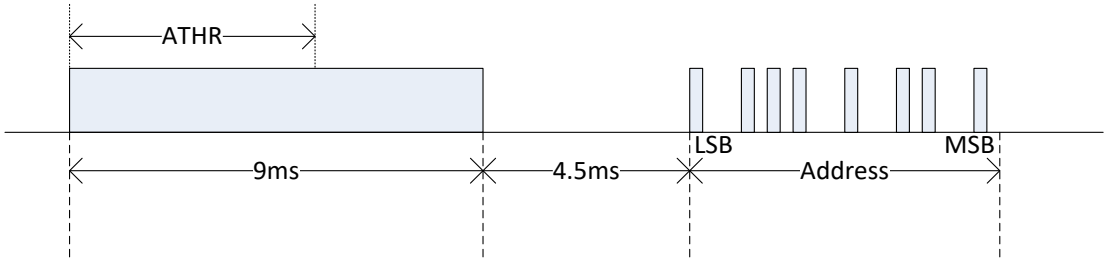


Figure 10- 47. ATHR Definition

- **ITHR(Idle Threshold)**

If electrical level of CIR_RX signals has no change, and the duration reaches this threshold, then CIR receiver enters into Idle state and ends this capture.

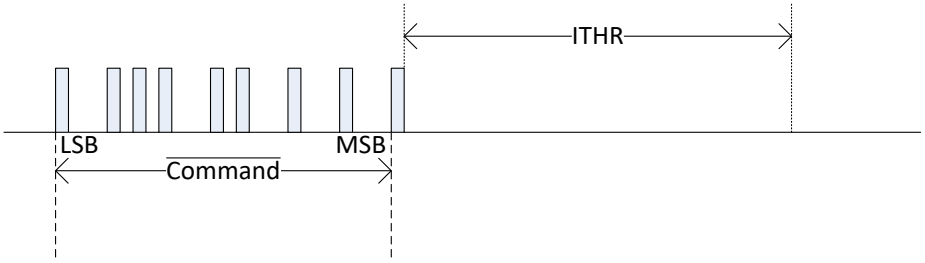


Figure 10- 48. ITHR Definition

- **NTHR(Noise Threshold)**

In capture process,the pulse is ignored if the pulse width is less than Noise Threshold.

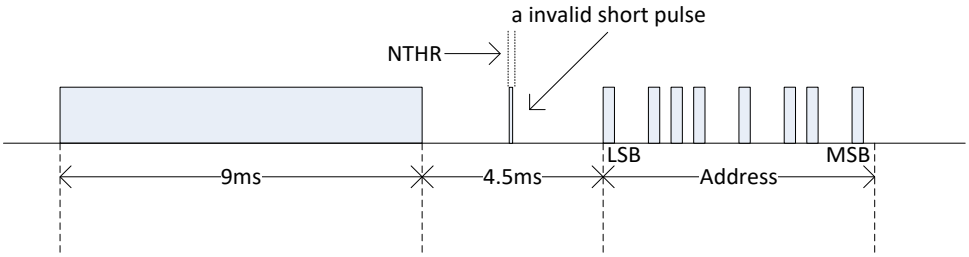


Figure 10- 49. NTHR Definition

- **APAM(Active Pulse Accept Mode)**

APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

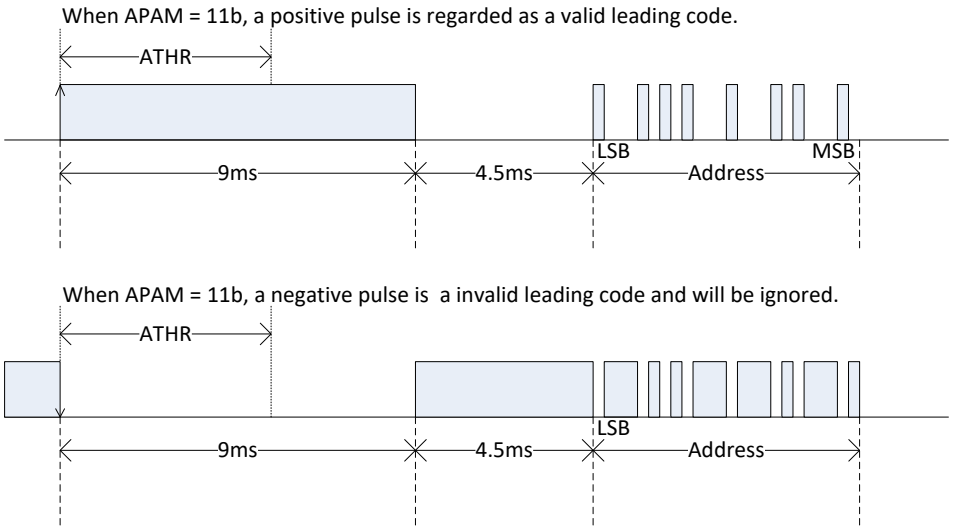


Figure 10- 50. APAM Definition

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.4. Programming Guidelines

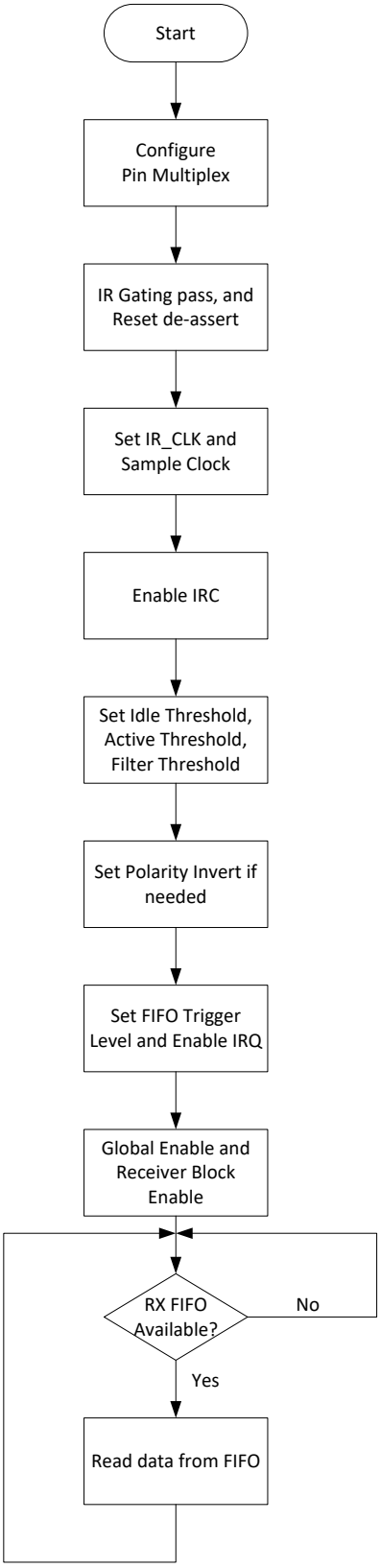


Figure 10- 51. CIR Receiver Process

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.5. Register List

Module Name	Base Address
CIR_RX	0x05071800
R_CIR_RX	0x07040000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXPCFG	0x0010	CIR Receiver Pulse Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_RXCFG	0x0034	CIR Receiver Configure Register

10.9.6. Register Description

10.9.6.1. 0x0000 CIR Receiver Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code 10: Only negative pulse is valid as a leading code 11: Only positive pulse is valid as a leading code
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.6.2. 0x0010 CIR Receiver Pulse Configure Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXPCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

10.9.6.3. 0x0020 CIR Receiver FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

10.9.6.4. 0x002C CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO available received byte level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

10.9.6.5. 0x0030 CIR Receiver Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: Busy
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.9.6.6. 0x0034 CIR Receiver Configure Register(Default Value: 0x0000_1828)

<table>
<tr><td colspan="3">Offset: 0x0034</td><td>Register Name: CIR_RXCFG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:25</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>24</td><td>R/W</td><td>0x0</td><td>SCS2
Bit2 of Sample Clock Select for CIR
This bit is defined by SCS bits below.</td></tr>
<tr><td>23</td><td>R/W</td><td>0x0</td><td>ATHC
Active Threshold Control for CIR
0: ATHR in unit of (Sample Clock)
1: ATHR in unit of (128*Sample Clocks)</td></tr>
<tr><td>22:16</td><td>R/W</td><td>0x0</td><td>ATHR
Active Threshold for CIR
These bits control the duration of CIR from idle to active state. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).</td></tr>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xA</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: All samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: If the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CIR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CIR_CLK /128</td></tr>
</table></td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0	1	0	CIR_CLK /256	
			0	1	1	CIR_CLK /512	
			1	0	0	CIR_CLK	
			1	0	1	Reserved	
			1	1	0	Reserved	
			1	1	1	Reserved	

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.10. CIR Transmitter

10.10.1. Overview

The CIR transmitter(CIR_TX) can transfer arbitrary wave, which is modulated with configurable carrier wave such as 38 kHz. It only uses low 8-bit of a 32-bit register, it stores with 2 register for a 16-bit number, one is high 8-bit, the other is low 8-bit.

The CIR_TX has the following features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Support Interrupt and DMA
- Support DMA shake and wait mode
- Support arbitrary wave generator

10.10.2. Block Diagram

Figure 10-52 shows a block diagram of the CIR_TX.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

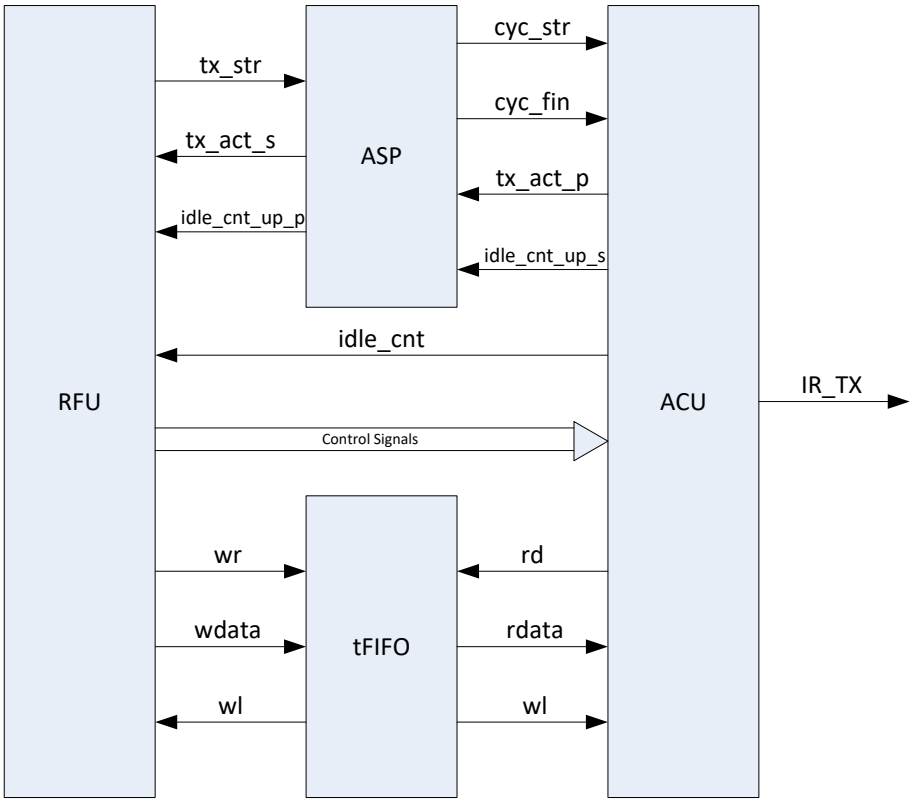


Figure 10- 52. CIR_TX Block Diagram

10.10.3. Operations and Functional Descriptions

10.10.3.1. External Signals

Table 10-30 describes the external signals of CIR_TX.

Table 10- 30. CIR_TX External Signals

Signal	Description	Type
CIR_OUT	Consumer infrared transmitter in CPUX	I

10.10.3.2. Clock and Reset

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

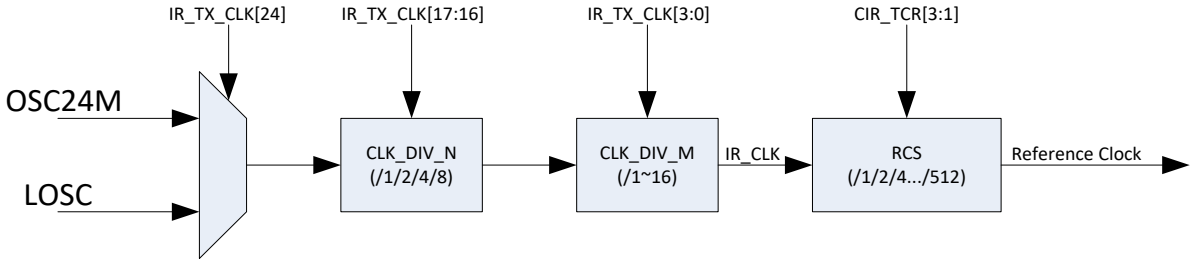


Figure 10- 53. CIR_TX Clock Description

10.10.3.3. Function Implementation

The CIR_TX is used to generate a wave of arbitrary length and shape. It has a low demand for speed, and it can transform data into level sequence of a specific length. Every data is a byte. The Bit[7] of a byte means whether the level of a transmitting wave is high or low. The Bit[6:0] is the length of this wave. If current transmitting frequency division is 1, 0x88 is a high level of 8 cycles, 0x08 is a low level of 8 cycles. If current transmitting frequency division is 4, 0x88 is a high level of 32 cycles, 0x08 is a low level of 32 cycles.

CIR_TX has two transmission modes, one is non-cycle transmission, and another one is cycle transmission. Non-cycle transmission is to transmit all the data in TX_FIFO to FIFO space. Cycle transmission is to transmit all the data in FIFO, until there are no signals. The data recovery in FIFO is implemented by clearing read pointer.

10.10.3.4. Timing Diagram

CIR remote control contains many protocols which designed by different manufacturers. Here to NEC protocol as an example, the CIR-TX module uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote-control applications. A message is started by a 9 ms AGC burst, which was used to set the gain of the earlier CIR receivers. This AGC burst is then followed by a 4.5 ms space, which is then followed by the address and command.

Bit definition: the logical “1” takes 2.25 ms to transmit, while a logical “0” is only 1.12 ms.

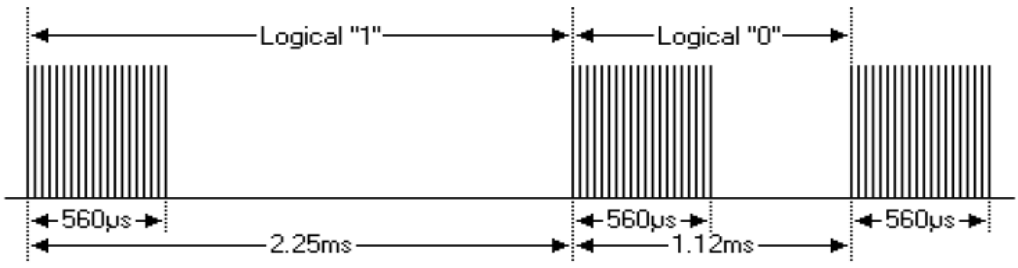


Figure 10- 54. CIR One Bit Definition

Timing for a message:

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

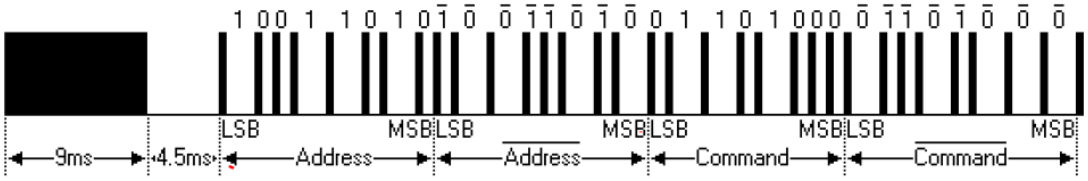
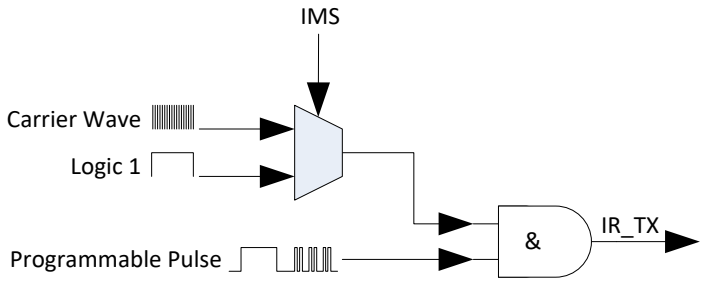


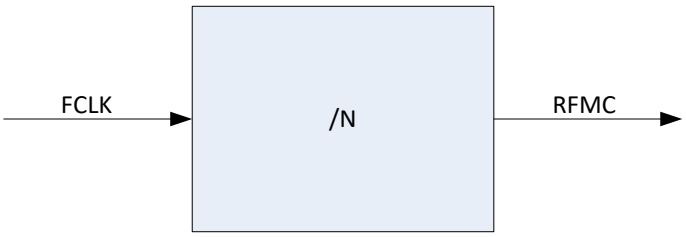
Figure 10- 55. CIR Message Timing Diagram

10.10.3.5. Operating Mode

- IMS: Internal modulation select



- RFMC: Reference frequency of modulated carrier. FCLK, is IR_CLK.



Default: FCLK = 6MHz, DIV = 0x9E
RFMC = FCLK/DIV = 38KHz

- DRMC: Duty ratio of modulated carrier. It can be set to 1/2, 1/3, and 1/4.

- RCS: Reference clock select
  The data in TX_FIFO is used to describe the pulse in Run-Length Code. The basic unit of pulse width is Reference Clock.

- CIR Transmitter Idle Duration Counter
  It is used in cycle transmission mode. When all the data in FIFO is transmitted, signals can be transmitted after a specific time.

- CIR Transmitter Idle Counter
  It is used to count idle duration of CIR transmitter, and it is used for software.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.10.4. Programming Guidelines

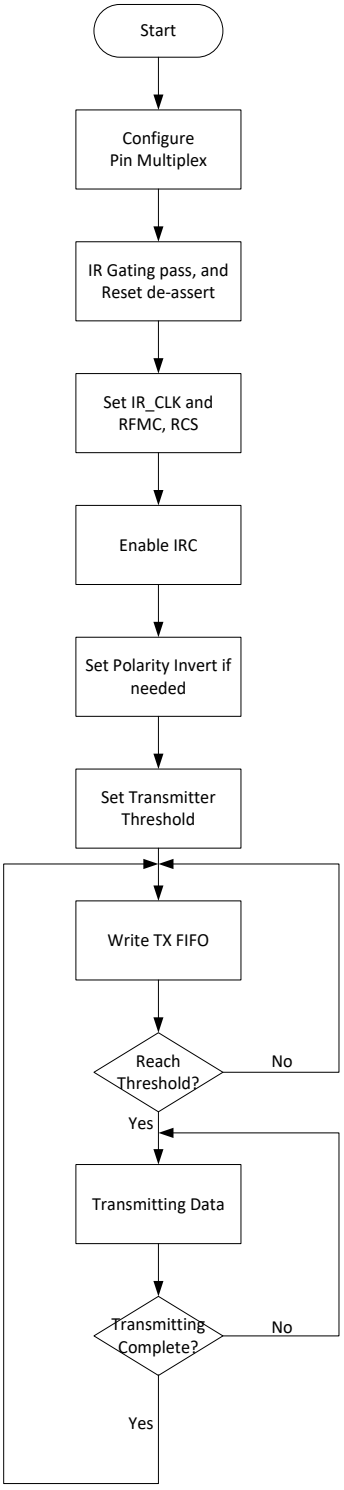


Figure 10- 56. CIR Transmitter Process

10.10.5. Register List

Module Name	Base Address

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CIR_TX	0x05071000

Register Name	Offset	Description
CIR_TGLR	0x0000	CIR Transmit Global Register
CIR_TMCR	0x0004	CIR Transmit Modulation Control Register
CIR_TCR	0x0008	CIR Transmit Control Register
CIR_IDC_H	0x000C	CIR Transmit Idle Duration Threshold Register
CIR_IDC_L	0x0010	CIR Transmit Idle Duration Threshold Register
CIR_TICR_H	0x0014	CIR Transmit Idle Counter Register
CIR_TICR_L	0x0018	CIR Transmit Idle Counter Register
CIR_TEL	0x0020	CIR TX FIFO Empty Level Register
CIR_TXINT	0x0024	CIR Transmit Interrupt Control Register
CIR_TAC	0x0028	CIR Transmit FIFO Available Counter Register
CIR_TXSTA	0x002C	CIR Transmit Status Register
CIR_TXT	0x0030	CIR Transmit Threshold Register
CIR_DMA	0x0034	CIR DMA Control Register
CIR_TXFIFO	0x0080	CIR Transmit FIFO Data Register

10.10.6. Register Description

10.10.6.1. 0x0000 CIR Transmitter Global Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_TGLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0x0	DRMC Duty ratio of modulated carrier is high level/low level. 00: low level is the one time of high level 01: low level is the two times of high level 10: low level is the three times of high level 11: reserved
4:3	/	/	/
2	R/W	0x0	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
1	R/W	0x0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TIC filed and CSS field will be cleared during Transmit Reset. This field will automatically cleared when the Transmit Reset is finished, and the CIR transmitter will state Idle.
0	R/W	0x0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

10.10.6.2. 0x0004 CIR Transmitter Modulation Control Register(Default Value:0x0000_009E)

Offset: 0x0004			Register Name: CIR_TMCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of modulated carrier. Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK). The range of the modulated carrier is usually 30 kHz to 60 kHz. The most consumer electronics is 38 kHz. The default modulated carrier is 38KHz when FCLK is 12 MHz. RFMC= FCLK/((N+1)*(DRMC+2)).

10.10.6.3. 0x0008 CIR Transmitter Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CIR_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	CSS Cyclical Pulse Start/Stop Control 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start. Start to transmit when it is set to '1'.
6:4	/	/	/
3:1	R/W	0x0	RCS Reference Clock Select for CIR Transmit 000: CIR Transmit reference clock is ir_clk 001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8 100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

0	R/W	0x0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

10.10.6.4. 0x000C CIR Transmitter Idle Duration Counter Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CIR_IDC_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
3:0	R/W	0x0	IDC_H Idle Duration Counter threshold(High 4 bits) Idle Duration = 128*IDC*Ts (IDC = 0~4095)

10.10.6.5. 0x0014 CIR Transmitter Idle Counter Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	TIC_H Transmit Idle Counter_H(High 8 bits) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

10.10.6.6. 0x0018 CIR Transmitter Idle Counter Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CIR_TICR_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	TIC_L Transmit Idle Counter_L(Low 8 bits) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.10.6.7. 0x0020 CIR Transmitter FIFO Empty Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_TEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

10.10.6.8. 0x0024 CIR Transmitter Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CIR_TXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0x0	TAI_EN TX FIFO Available Interrupt Enable 0:Disable 1:Enable
0	R/W	0x0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0:Disable 1:Enable TUI_EN Transmitter FIFO Underrun Interrupt Enable for Non-cyclical Pulse 0: Disable 1: Enable

10.10.6.9. 0x0028 CIR Transmitter FIFO Available Counter Register(Default Value: 0x0000_0080)

Offset: 0x0028			Register Name: CIR_TAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x80	TAC TX FIFO Available Space Counter

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x00: No available space in TX FIFO 0x01: 1 byte available space in TX FIFO 0x02: 2 byte available space in TX FIFO … 0x80: 128 byte available space in TX FIFO

10.10.6.10. 0x002C CIR Transmitter Status Register(Default Value: 0x0000_0002)

Offset: 0x002C			Register Name: CIR_TXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	STCT Status of CIR Transmitter 0: Idle 1: Active This bit will automatically set when the controller begins transmit the data in the FIFO. The “1” will last when the data in the FIFO. It will automatically be cleared to “0” when all data in the FIFO is transmitted. The bit is for debug. **Output Level of Idle state determined by level of the last data output.**
2	R	0x0	DRQ DMA Request Flag When set to ‘1’, the Tx FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0x1	TAI TX FIFO Available Interrupt Flag 0: TX FIFO not available by its level 1: TX FIFO available by its level This bit can be cleared by software writing ‘1’.
0	R/W	0x0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a ‘1’.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.10.6.11. 0x0030 CIR Transmitter Threshold Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_TXT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reached the Transmit Threshold set in this field.

10.10.6.12. 0x0034 CIR Transmitter DMA Control Register(Default Value: 0x0000_00A5)

Offset: 0x0034			Register Name: CIR_DMA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	DMA Handshake Configuration 0xA5: DMA wait cycle mode 0xEA: DMA handshake mode

10.10.6.13. 0x0080 CIR Transmitter FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number has been transmitted finished.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11. PWM

10.11.1. Overview

The PWM controller has 4 PWM channels(PWM0,PWM1,PWM2,PWM3), and divides to 2 PWM pairs:PWM01 pair, PWM23 pair. PWM01 pair consists of PWM0 and PWM1, PWM23 pair consists of PWM2 and PWM3.

The PWM has the following features:

- 4 PWM channels(2 PWM pairs)
- Supports pulse(configurable pulse number),cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~ 24 MHz/100 MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

10.11.2. Block Diagram

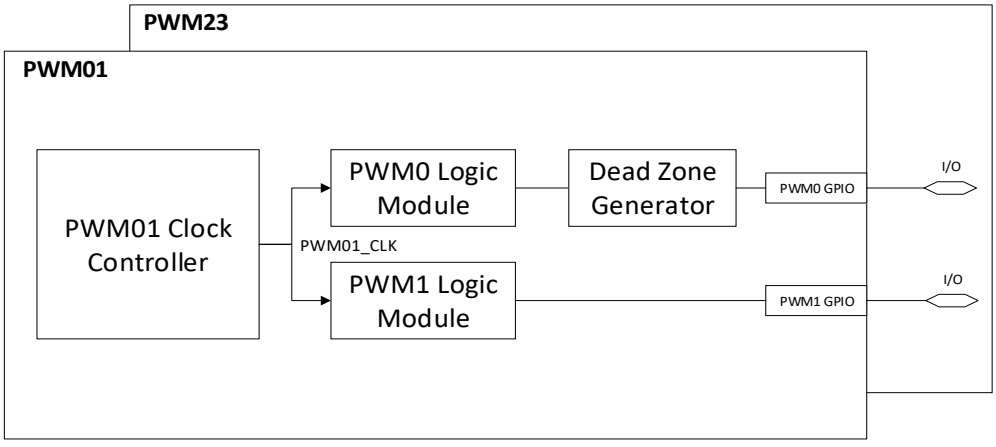


Figure 10- 57. PWM Block Diagram

Each PWM pair consists of 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.3. Operations and Functional Descriptions

10.11.3.1. External Signals

Table 10-31 describes the external signals of the PWM.

Table 10- 31. PWM External Signals

Signal	Description	Type
PWM0	Pulse Width Module Channel0	I/O
PWM1	Pulse Width Module Channel1	I/O
PWM2	Pulse Width Module Channel2	I/O
PWM3	Pulse Width Module Channel3	I/O

10.11.3.2. Typical Application

- Suitable for display device, such as LCD
- Suitable for electric motor control

10.11.3.3. Clock Controller

Using PWM01 as an example, the clock controller diagram is as follows. The clock controller diagram of other PWM pairs is the same as PWM01.

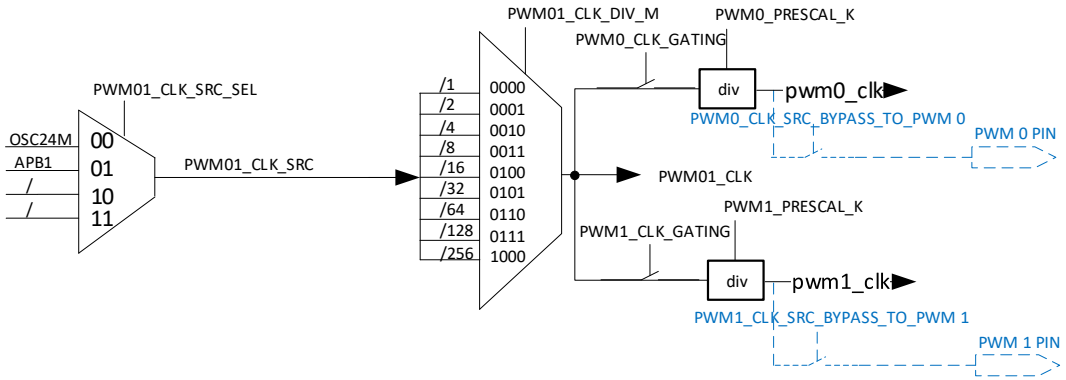


Figure 10- 58. PWM01 Clock Controller Diagram

The clock controller of each PWM pair(for example: PWM01) includes clock source select(PWM01_CLK_SRC_SEL), the first-level exponent divider (PWM01_CLK_DIV_M), the second-level count divider(PRESCAL_K), clock source bypass(CLK_SRC_BYPASS) and clock switch(PWM01_CLK_GATING).

The clock sources of PWM have OSC24M and APB1 Bus. OSC24M comes from external high frequency oscillator, APB1 is APB1 bus clock, usually is 100 MHz.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The clock source bypass function is that clock source directly accesses PWM output, the PWM output waveform is the waveform of clock controller output. The BYPASS gridlines in the above figure indicates clock source bypass function, the details about implement, please see Figure 10-59.

10.11.3.4. PWM Output

Using PWM01 as an example, Figure 10-59 indicates PWM01 output logic module diagram. Other PWM pairs logic module diagrams are the same as PWM01.

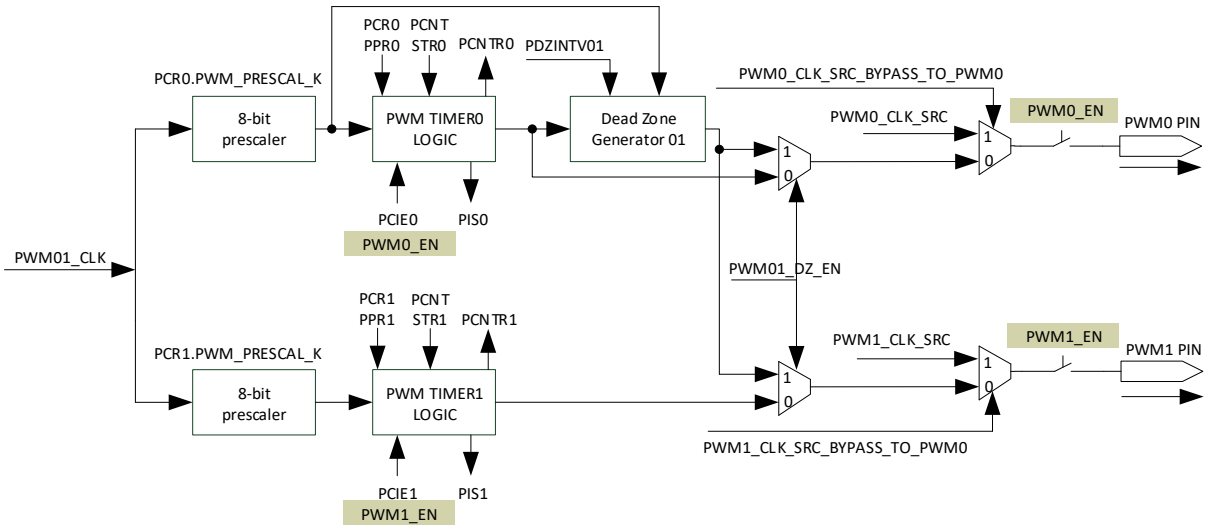


Figure 10- 59. PWM01 Output Logic Module Diagram

The timer logic module of PWM(PWM_TIMER_LOGIC) consists of one 16-bit up-counter(PCNTR) and three 16-bit parameters(PWM_ENTIRE_CYCLE, PWM_ACTIVE_CYCLE, PWM_CNTSTART). The PWM_ENTIRE_CYCLE is used to control PWM cycle, the PWM_ACTIVE_CYCLE is used to control duty-cycle, the PWM_CNTSTART is used to control output phase(multi-channels synchronization work requirements).

The PWM_ENTIRE_CYCLE and the PWM_ACTIVE_CYCLE support cache loading, after PWM output is enabled, the register values of the PWM_ENTIRE_CYCLE and the PWM_ACTIVE_CYCLE can be changed anytime, the changed value caches into the cache register. When PCNTR counter outputs a period of PWM waveform, the value of the cache register can be updated for PCNTR control. Cache-loading is good to avoid unstable PWM output waveform with burred feature when updating the values of the PWM_ENTIRE_CYCLE and the PWM_ACTIVE_CYCLE.

PWM supports cycle and pulse waveform output.
Cycle mode: PWM outputs the setting PWM waveform continually, that is, the output waveform is a continuous PWM square wave.
Pulse mode: After setting PWM_PUL_CNT parameter, PWM outputs (PWM_PULNUM+1) periods of PWM waveform, that is, the waveform with several pulses are output.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.3.5. Period, Duty-cycle and Phase

The period, duty-cycle and phase of PWM output waveform are decided by the PCNTR, PWM_ENTIRE_CYCLE, PWM _ACT_CYCLE and PWM_CNTSTART. The rules are as follows.

- PCNTR=（PCNTR==PWM_ENTIRE_CYCLE）?0 : PCNTR + 1
- PCNTR starts to count by PWM_CNTSTART, the counter of a PWM period is (PWM_ENTIRE_CYCLE+1).
- PCNTR > (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “active state”
- PCNTR <= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “ ~ (active state)”

(1) Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)

When PCNTR0 > (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1(high level).
When PCNTR0 <= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0(low level).

The formula of PWM output period and duty-cycle is as follows.
T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0. PWM_ENTIRE_CYCLE + 1)
$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE
$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)
Duty-cycle = (high level time) / (1 period time) = $T_{high\text{-}level}$ / T_{period}

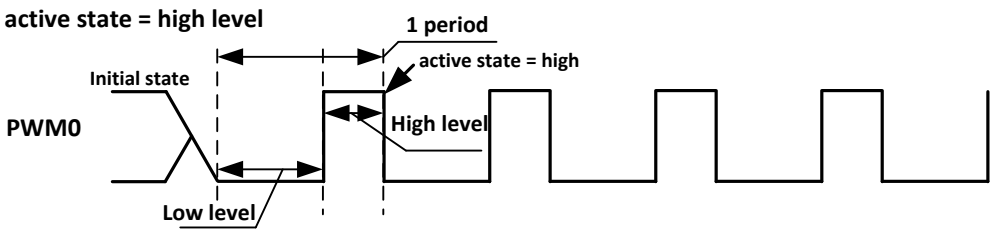


Figure 10- 60. The Period and Duty-cycle of PWM0 High Level Active State

(2) Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)

When PCNTR0 > (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.
When PCNTR0 <= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

The formula of PWM output period and duty-cycle is as follows.
T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0. PWM_ENTIRE_CYCLE + 1)
$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)
$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE
Duty-cycle = (low level time) / (1 period time) = $T_{low\text{-}level}$ / T_{period}

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

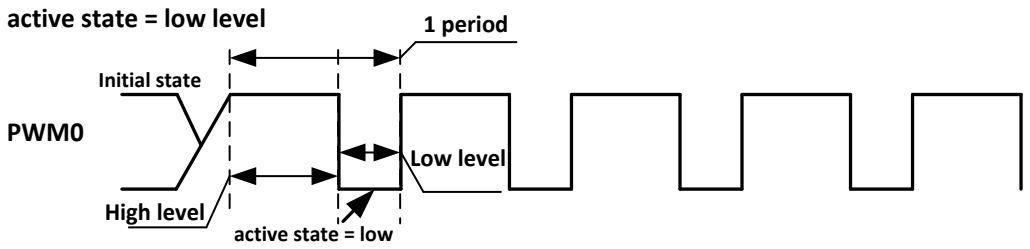


Figure 10- 61. The Period and Duty-cycle of PWM0 Low Level Active State

The counter of PCNTR starts from 0 by default, it can output the pulse control of the waveform by setting PWM_CNTSTART. The figure is as follows.

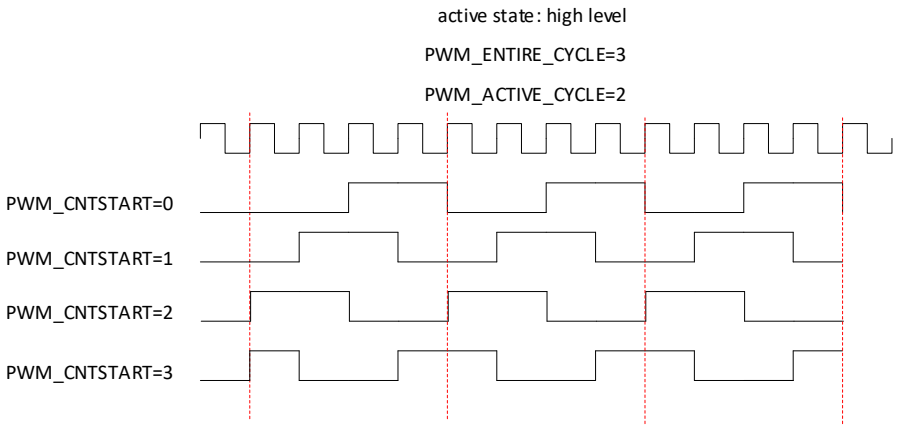


Figure 10- 62. The Phase of PWM0 High Level Active State

10.11.3.6. Pulse Mode and Cycle Mode

PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs one pulse waveform, but PWM in cycle mode outputs continuous waveform. Figure 10-63 shows the PWM output waveform in pulse mode and cycle mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

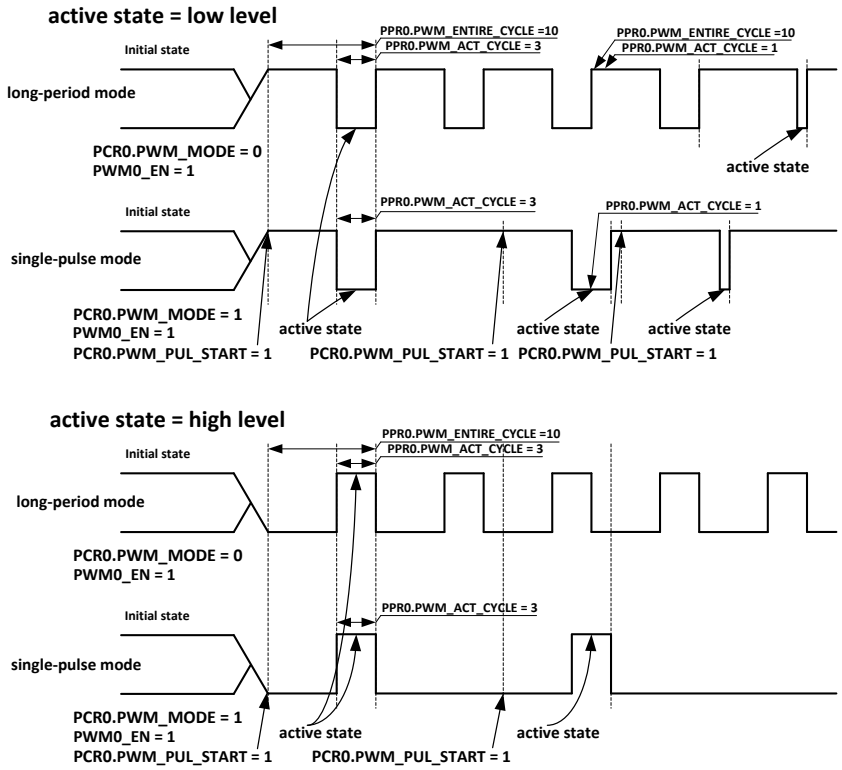


Figure 10- 63. PWM0 Output Waveform in Pulse Mode and Cycle Mode

Each channel of PWM module supports the PWM output of pulse mode and cycle mode, the active state of PWM output waveform can be programmed to control.

When PCR0.PWM_MODE is 0, PWM0 outputs in cycle mode. When PCR0.PWM_MODE is 1, PWM0 outputs in pulse mode.

Specifically, in pulse mode, after PWM0 channel enabled, PCR0. PWM_PUL_START need be set to 1 when PWM0 need output pulse waveform, after completed output, PCR0. PWM_PUL_START can be cleared to 0 by hardware. The next setting 1 can be operated after PCR0. PWM_PUL_START is cleared.

.

10.11.3.7. Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time. Figure 10-64 shows the complementary pair output of PWM01.

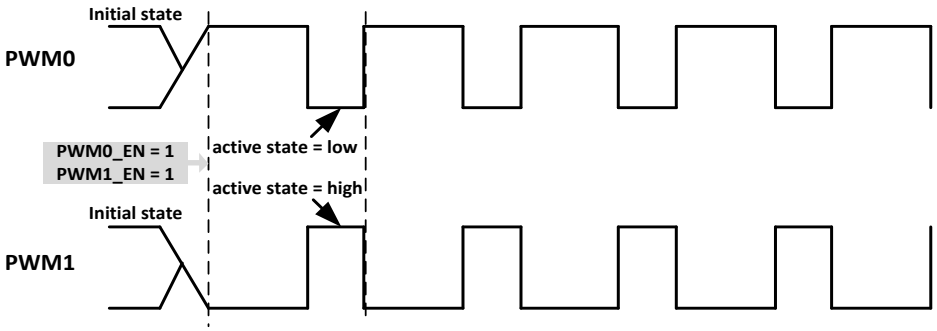


Figure 10- 64. PWM01 Complementary Pair Output

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

The complementary pair output needs to satisfy the following four conditions:

- PWM0 and PWM1 have the same clock divider, frequency, duty-cycle, pulse
- PWM0 and PWM1 have opposite active state
- Enable the clock gating of PWM0 and PWM1 at the same time
- Enable the waveform output of PWM0 and PWM1 at the same time

10.11.3.8. Dead-time Generator

Every PWM pair has a programmable dead-time generator. When the dead-time function of PWM pair enabled, PWM01 pair outputs a pair of PWM waveforms that insert dead-time, PWM01 pair output waveform is decided by PWM0 timer logic module and DeadZone Generator01. Figure 10-65 shows the output waveform.

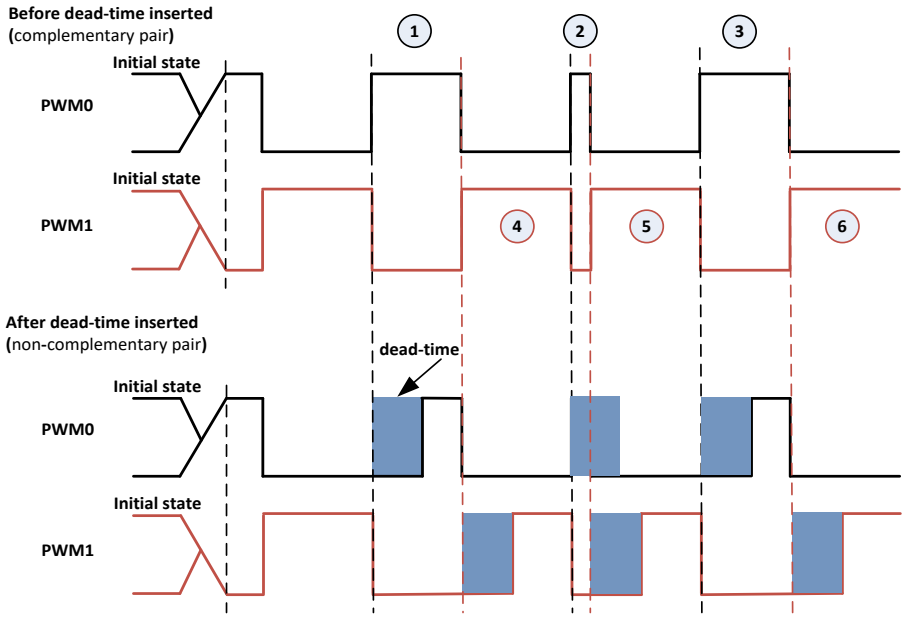


Figure 10- 65. PWM01 Pair Waveform Before/After Insert Dead-time

The PWM waveform before the insertion of dead-time indicates a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.

The PWM waveform after the insertion of dead-time indicates a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01. The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

For complementary pair of Dead Zone Generator 01, the principle of inserting dead-time is that to insert dead-time as soon as the rising edge came. If high level time for mark② in the above figure is less than dead-time, then dead-time will override the high level. The setting of dead-time need consider the period and duty-cycle of output waveform. Dead-time formula is defined as follows:

Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.3.9. PWM Group Mode

Using PWM Group0 as an example. The same group of PWM channel is selected to work by PGR0.CS; the same PWM_ENTIRE_CYCLE, PWM_ACTIVE_CYCLE are set by the same clock configuration; the different PWM_CNTSTART can output PWM group signals with same duty-cycle, different phase.

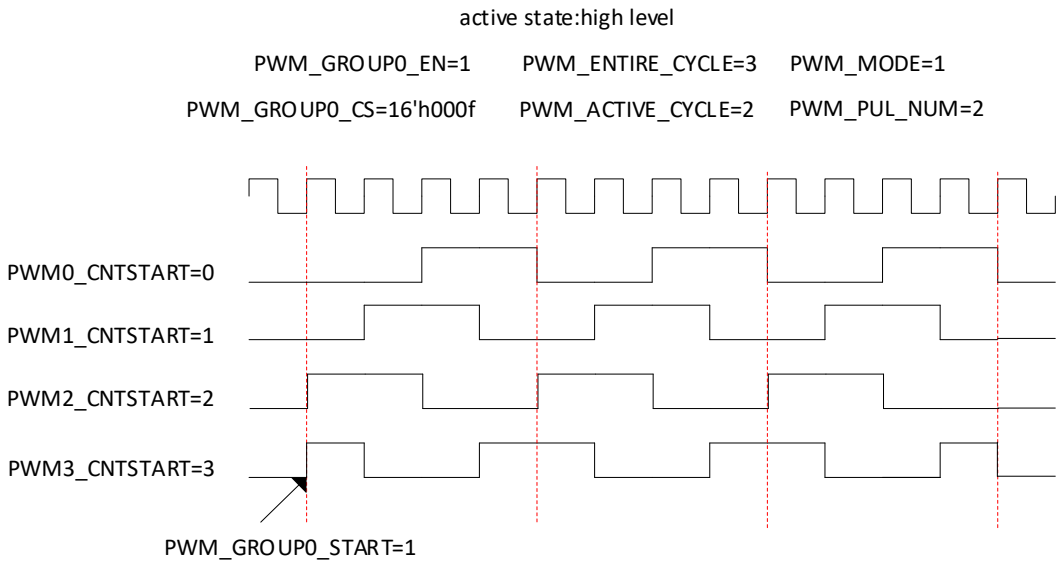


Figure 10- 66. Group 0~3 PWM Signal Output

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.3.10. Capture Input

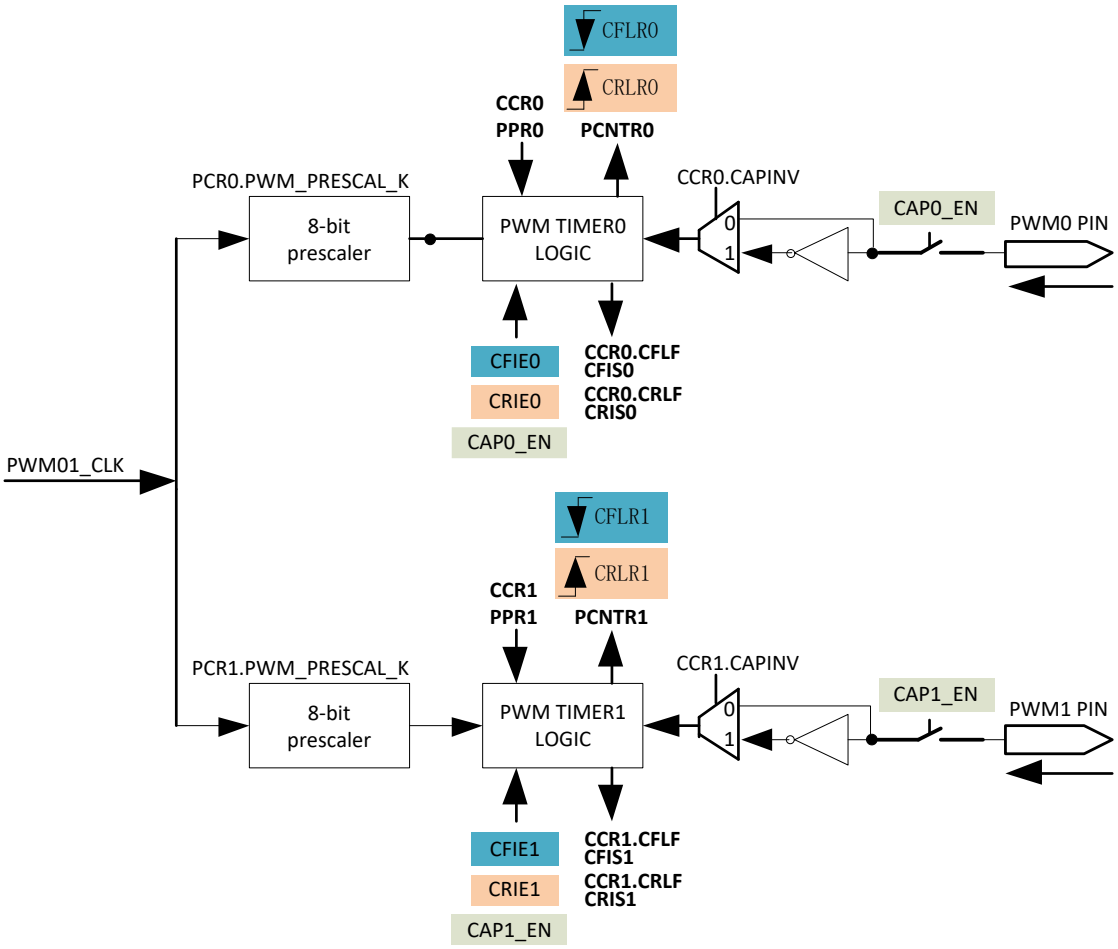


Figure 10- 67. PWM01 Capture Logic Module Diagram

Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture rising edge and falling edge of the external clock. Using PWM0 channel as an example, PWM0 channel has one **CFLR0** and one **CRLR0** for capturing up-counter value in falling edge and rising edge, respectively. You can calculate the period of external clock by **CFLR0** and **CRLR0**.

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

$T_{period} = T_{high\text{-}level} + T_{low\text{-}level}$

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

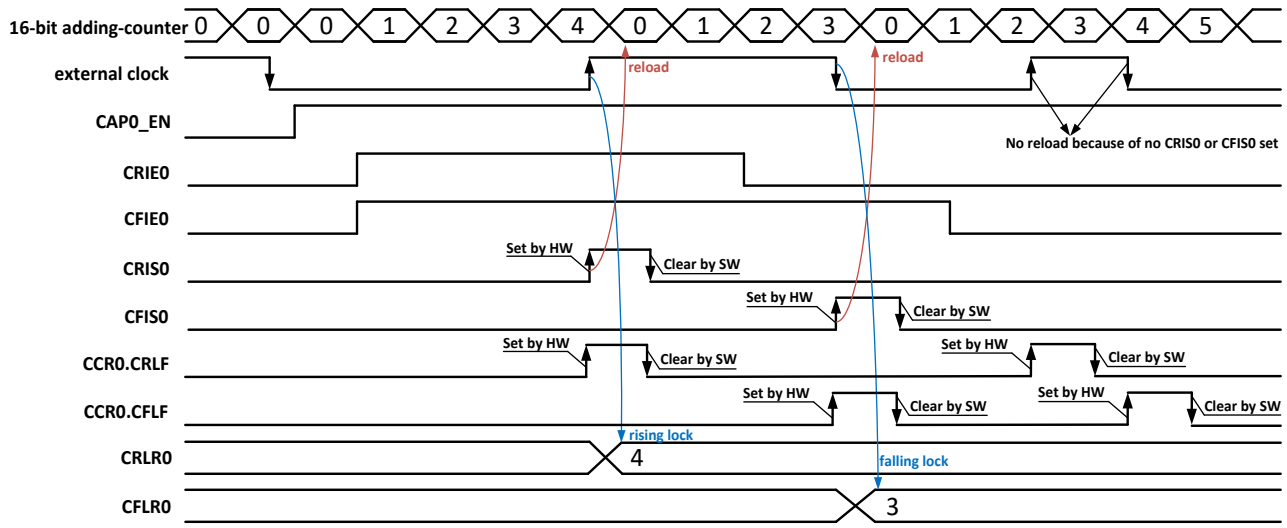


Figure 10- 68. PWM0 Channel Capture Timing

When the capture input function of PWM0 channel is enabled, the PCNTR of PWM0 channel starts to work.

When the timer logic module of PWM0 captures one rising edge, the current value of up-counter is locked to **CRLR0**, and **CCR0.CRLF** is set to 1. If **CRIE0** is 1, then **CRIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CRIE0** is 0, the timer logic module of PWM0 captures rising edge, **CRIS0** can not be set to 1, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of **PCNTR** is locked to **CFLR0**, and **CCR0.CFLF** is set to 1. If **CFIE0** is 1, then **CFIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CFIE0** is 0, the timer logic module of PWM0 captures falling edge, **CFIS0** can not be set to 1, the up-counter is not loaded to 0.

10.11.3.11. Interrupt

PWM supports interrupt generation when PWM channel is configured to PWM output or capture input .

For PWM output function, when one period of PWM waveform is output in cycle mode, the PIS of the corresponding PWM channel is set to 1; when (PWM_PULNUM+1) periods of PWM waveform is outputted in pulse mode, the PIS of the corresponding PWM channel is set to 1.

NOTE

The PIS bit is set to 1 automatically by hardware and cleared by software.

For capture input function, when the timer logic module of the capture channel0 captures rising edge, and **CRIE0** is 1, then **CRIS0** is set to 1; when the timer logic module of the capture channel0 captures falling edge, and **CFIE0** is 1, then **CFIS0** is set to 1.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.4. Working Mode

The following working mode takes PWM01 as an example, other PWM pairs and PWM01 are consistent.

10.11.4.1. Clock Configuration

(1) PWM gating: When using PWM, write 1 to **PCGR[PWMx_CLK_GATING]**.
(2) PWM clock source select: Set **PCCR01[PWM01_CLK_SRC]** to select OSC24M or APB1 clock.
(3) PWM clock divider: Set **PCCR01[PWM01_CLK_DIV_M]** to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).
(4) PWM clock bypass: Set **PCGR[PWM_CLK_SRC_BYPASS_TO_PWM]** to 1, output the PWM clock after the secondary frequency division to the corresponding PWM output pin.
(5) PWM internal clock configuration: Set **PCR[PWM_PRESCAL_K]** to select any frequency division coefficient from 1 to 256.

NOTE

For the channel of complementary output and group mode, firstly, set the same clock configurations(clock source selects APB1, clock division configures the same division factor); secondly, open clock gating at the same time; thirdly, configure PWM parameters; finally, enable PWM output at the same time to ensure each channel sync.
Because PWM pair has the same first level clock division and gating, we suggest that the two channels of the same PWM pair can not subject to two groups, if must allocate based on this way, the first level of clock division of the channel used by all groups needs to set to the same coefficient and open gating at the same time. And the total module needs be reset when group mode regroups.

10.11.4.2. PWM Configuration

(1) PWM mode: Set **PCR[PWM_MODE]** to select cycle mode or pulse mode, if pulse mode, PWM_PUL_NUM needs be configured.
(2) PWM active level: Set **PCR[PWM_ACT_STA]** to select low level or high level.
(3) PWM duty-cycle: Configure **PPR[PWM_ENTIRE_CYCLE]** and **PPR[PWM _ACT_CYCLE]** after clock gating is opened.
(4) Enable PWM: Configure PER to select the corresponding PWM enable bit; when selecting pulse mode, **PCR[PWM_PUL_START]** needs be enabled.

10.11.4.3. Deadzone Control

(1) Deadzone initial value: Set **PDZCR01[PDZINTV01]**.
(2) Deaszone enable: Set **PDZCR01[PWM01_DZ_CN]**.

10.11.4.4. Capture Input

(1) Capture enable: Configure CER to enable the corresponding channel.
(2) Capture mode: Configure **CCR[CRLF]** and **CCR[CFLF]** to select rising edge capture or falling edge capture, configure

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

CCR[CAPINV] to select whether the input signal does reverse processing.

10.11.5. Register List

Module Name	Base Address
PWM	0x0300A000
R_PWM	0x07020C00

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCGR	0x0040	PWM Clock Gating Register
PDZCR01	0x0060	PWM01 Dead Zone Control Register
PDZCR23	0x0064	PWM23 Dead Zone Control Register
PER	0x0080	PWM Enable Register
PGR0	0x0090	PWM Group0 Register
PGR1	0x0094	PWM Group1 Register
PGR2	0x0098	PWM Group2 Register
PGR3	0x009C	PWM Group3 Register
CER	0x00C0	Capture Enable Register
PCR	0x0100+0x0000+N*0x0020(N=0~3)	PWM Control Register
PPR	0x0100+0x0004+N*0x0020(N=0~3)	PWM Period Register
PCNTR	0x0100+0x0008+N*0x0020(N=0~3)	PWM Count Register
PPCNTR	0x0100+0x000C+N*0x0020(N=0~3)	PWM Pulse Count Register
CCR	0x0100+0x0010+N*0x0020(N=0~3)	Capture Control Register
CRLR	0x0100+0x0014+N*0x0020(N=0~3)	Capture Rise Lock Register
CFLR	0x0100+0x0018+N*0x0020(N=0~3)	Capture Fall Lock Register

10.11.6. Register Description

10.11.6.1. 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	PGIE3 PWM Group 3 Interrupt Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
18	R/W	0x0	PGIE2 PWM Group 2 Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PGIE1 PWM Group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM Group 0 Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	PCIE3 PWM Channel 3 Interrupt Enable 0: PWM channel 3 interrupt disable 1: PWM channel 3 interrupt enable
2	R/W	0x0	PCIE2 PWM Channel 2 Interrupt Enable 0: PWM channel 2 interrupt disable 1: PWM channel 2 interrupt enable
1	R/W	0x0	PCIE1 PWM Channel 1 Interrupt Enable 0: PWM channel 1 interrupt disable 1: PWM channel 1 interrupt enable
0	R/W	0x0	PCIE0 PWM Channel 0 Interrupt Enable 0: PWM channel 0 interrupt disable 1: PWM channel 0 interrupt enable

10.11.6.2. 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			**Register Name: PISR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W1C	0x0	PGIS3 PWM Group 3 Interrupt Status
18	R/W1C	0x0	PGIS2 PWM Group 2 Interrupt Status
17	R/W1C	0x0	PGIS1 PWM Group 1 Interrupt Status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16	R/W1C	0x0	PGIS0 PWM Group 0 Interrupt Status
15:4	/	/	/
3	R/W1C	0x0	PIS3 PWM Channel 3 Interrupt Status When the counter of PWM channel 3 reaches Entire Cycle Value, this bit is set to 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. Reads 1: PWM channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2 PWM Channel 2 Interrupt Status When the counter of PWM channel 2 reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. Reads 1: PWM channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM Channel 1 Interrupt Status When the counter of PWM channel 1 reaches Entire Cycle Value, this bit is set to 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. Reads 1: PWM channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM Channel 0 Interrupt Status When the counter of PWM channel 0 reaches Entire Cycle Value, this bit is set to 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. Reads 1: PWM channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 0 interrupt status.

10.11.6.3. 0x0010 PWM Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0010			**Register Name: CIER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	CFIE3 If the bit is set to 1, when capturing channel 3 captures falling edge, it generates a capturing channel 3 pending.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Capturing channel 3 fall lock interrupt disable 1: Capturing channel 3 fall lock interrupt enable
6	R/W	0x0	CRIE3 If the bit is set to 1, when capturing channel 3 captures rising edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 rise lock interrupt disable 1: Capturing channel 3 rise lock interrupt enable
5	R/W	0x0	CFIE2 If the bit is set to 1, when capturing channel 2 captures falling edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 fall lock interrupt disable 1: Capturing channel 2 fall lock interrupt enable
4	R/W	0x0	CRIE2 If the bit is set to 1, when capturing channel 2 captures rising edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 rise lock interrupt disable 1: Capturing channel 2 rise lock interrupt enable
3	R/W	0x0	CFIE1 If the bit is set to 1, when capturing channel 1 captures falling edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 fall lock interrupt disable 1: Capturing channel 1 fall lock interrupt enable
2	R/W	0x0	CRIE1 If the bit is set to 1, when capturing channel 1 captures rising edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 rise lock interrupt disable 1: Capturing channel 1 rise lock interrupt enable
1	R/W	0x0	CFIE0 If the bit is set to 1, when capturing channel 0 captures falling edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 fall lock interrupt disable 1: Capturing channel 0 fall lock interrupt enable
0	R/W	0x0	CRIE0 If the bit is set to 1, when capturing channel 0 captures rising edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 rise lock interrupt disable 1: Capturing channel 0 rise lock interrupt enable

10.11.6.4. 0x0014 PWM Capture IRQ Status Register (Default Value: 0x0000_0000) ?

Offset:0x0014			**Register Name: CISR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	**CFISF** Capture channel F falling lock interrupt status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel F captures falling edge, if capture channel F fall lock interrupt (CFIEF) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel F interrupt is not pending. 1: Capture channel F interrupt is pending. Writes 0: no effect. 1: Clear capture channel F interrupt status.
30	R/W1C	0x0	**CRISF** Capture channel F rising lock interrupt status When capture channel F captures rising edge, if capture channel F rise lock interrupt (CRIEF) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel F interrupt is not pending. 1: Capture channel F interrupt is pending. Writes 0: no effect. 1: Clear capture channel F interrupt status.
29	R/W1C	0x0	**CFISE** Capture channel E falling lock interrupt status When capture channel E captures falling edge, if capture channel E fall lock interrupt (CFIEE) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel E interrupt is not pending. 1: Capture channel E interrupt is pending. Writes 0: no effect. 1: Clear capture channel E interrupt status.
28	R/W1C	0x0	**CRISE** Capture channel E rising lock interrupt status When capture channel E captures rising edge, if capture channel E rise lock interrupt (CRIEE) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel E interrupt is not pending. 1: Capture channel E interrupt is pending. Writes 0: no effect. 1: Clear capture channel E interrupt status.
27	R/W1C	0x0	**CFISD** Capture channel D falling lock interrupt status When capture channel D captures falling edge, if capture channel D fall lock interrupt (CFIED) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel D interrupt is not pending. 1: Capture channel D interrupt is pending. Writes 0: no effect. 1: Clear capture channel D interrupt status.
26	R/W1C	0x0	**CRISD** Capture channel D rising lock interrupt status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel D captures rising edge, if capture channel D rise lock interrupt (CRIED) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel D interrupt is not pending. 1: Capture channel D interrupt is pending. Writes 0: no effect. 1: Clear capture channel D interrupt status.
25	R/W1C	0x0	**CFISC** Capture channel C falling lock interrupt status When capture channel C captures falling edge, if capture channel C fall lock interrupt (CFIEC) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel C interrupt is not pending. 1: Capture channel C interrupt is pending. Writes 0: no effect. 1: Clear capture channel C interrupt status.
24	R/W1C	0x0	**CRISC** Capture channel C rising lock interrupt status When capture channel C captures rising edge, if capture channel C rise lock interrupt (CRIEC) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel C interrupt is not pending. 1: Capture channel C interrupt is pending. Writes 0: no effect. 1: Clear capture channel C interrupt status.
23	R/W1C	0x0	**CFISB** Capture channel B falling lock interrupt status When capture channel B captures falling edge, if capture channel B fall lock interrupt (CFIEB) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel B interrupt is not pending. 1: Capture channel B interrupt is pending. Writes 0: no effect. 1: Clear capture channel B interrupt status.
22	R/W1C	0x0	**CRISB** Capture channel B rising lock interrupt status When capture channel B captures rising edge, if capture channel B rise lock interrupt (CRIEB) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel B interrupt is not pending. 1: Capture channel B interrupt is pending. Writes 0: no effect. 1: Clear capture channel B interrupt status.
21	R/W1C	0x0	**CFISA** Capture channel A falling lock interrupt status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel A captures falling edge, if capture channel A fall lock interrupt (CFIEA) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel A interrupt is not pending. 1: Capture channel A interrupt is pending. Writes 0: no effect. 1: Clear capture channel A interrupt status.
20	R/W1C	0x0	**CRISA** Capture channel A rising lock interrupt status When capture channel A captures rising edge, if capture channel A rise lock interrupt (CRIEA) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel A interrupt is not pending. 1: Capture channel A interrupt is pending. Writes 0: no effect. 1: Clear capture channel A interrupt status.
19	R/W1C	0x0	**CFIS9** Capture channel 9 falling lock interrupt status When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (CFIE9) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.
18	R/W1C	0x0	**CRIS9** Capture channel 9 rising lock interrupt status When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (CRIE9) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	**CFIS8** Capture channel 8 falling lock interrupt status When capture channel 8 captures falling edge, if capture channel 8 fall lock interrupt (CFIE8) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.
16	R/W1C	0x0	**CRIS8** Capture channel 8 rising lock interrupt status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (CRIE8) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	**CFIS7** Capture channel 7 falling lock interrupt status When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	**CRIS7** Capture channel 7 rising lock interrupt status When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	**CFIS6** Capture channel 6 falling lock interrupt status When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
12	R/W1C	0x0	**CRIS6** Capture channel 6 rising lock interrupt status When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	**CFIS5** Capture channel 5 falling lock interrupt status

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	**CRIS5** Capture channel 5 rising lock interrupt status When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	**CFIS4** Capture channel 4 falling lock interrupt status When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	**CRIS4** Capture channel 4 rising lock interrupt status When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (**CFIE3**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (**CRIE3**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (**CFIE2**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (**CRIE2**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (**CFIE1**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (**CRIE1**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (**CFIE0**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (**CRIE0**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.

10.11.6.5. 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0020			**Register Name: PCCR01**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM01_CLK_SRC Select PWM01 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM01_CLK_DIV_M PWM01 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.11.6.6. 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: PCCR23
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM23_CLK_SRC_SEL Select PWM23 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM23_CLK_DIV_M PWM23 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.11.6.7. 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PCGR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source(after pre-scale) to PWM3 output 0: not bypass 1: bypass
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source(after pre-scale) to PWM2 output 0: not bypass 1: bypass
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source(after pre-scale) to PWM1 output 0: not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source(after pre-scale) to PWM0 output 0: not bypass

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: bypass
15:4	/	/	/
3	R/W	0x0	PWM3_CLK_GATING Gating clock for PWM3 0: Mask 1: Pass
2	R/W	0x0	PWM2_CLK_GATING Gating clock for PWM2 0: Mask 1: Pass
1	R/W	0x0	PWM1_CLK_GATING Gating clock for PWM1 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING Gating clock for PWM0 0: Mask 1: Pass

10.11.6.8. 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: PDZCR01
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01 PWM01 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable.

10.11.6.9. 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0064			Register Name: PDZCR23
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone Enable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Dead Zone disable 1: Dead Zone enable

10.11.6.10. 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

Offset:0x0080			Register Name: PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	PWM3_EN 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN 0: PWM disable 1: PWM enable
1	R/W	0x0	PWM1_EN 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN 0: PWM disable 1: PWM enable

10.11.6.11. 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable.
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0.

10.11.6.12. 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable.
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1.

10.11.6.13. 0x0098 PWM Group2 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PGR2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PWMG2_START PWM channels selected in PWMG2_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG2_EN PWM Group2 Enable.
15:0	R/W	0x0	PWMG2_CS If bit[i] is set, PWM i is selected as one channel of PWM Group2.

10.11.6.14. 0x009C PWM Group3 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PGR3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PWMG3_START PWM channels selected in PWMG3_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG3_EN PWM Group3 Enable.
15:0	R/W	0x0	PWMG3_CS If bit[i] is set, PWM i is selected as one channel of PWM Group3.

10.11.6.15. 0x00C0 Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: CER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	CAP3_EN When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Capture enable
2	R/W	0x0	CAP2_EN When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When enable capture function, the 16-bit up-counter starts working and capture channel0 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

10.11.6.16. 0x0100 + N*0x20 PWM Control Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0+N*0x20(N=0~3)			Register Name: PCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM Period Register Ready 0: PWM period register is ready to write 1: PWM period register is busy
10	R/W1S	0x0	PWM_PUL_START PWM Pulse Output Start 0: No effect 1: Output pulse for PWM_CYCLE_NUM+1. After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM Output Mode Select 0: Cycle mode 1: Pulse mode
8	R/W	0x0	PWM_ACT_STA PWM Active State 0: Low Level 1: High Level

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

10.11.6.17. 0x0104 + N*0x20 PWM Period Register (Default Value: 0x0000_0000)

Offset:0x0100+0x04+N*0x20(N=0~3)			Register Name: PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock. 0: 1 cycle 1: 2 cycles … N: N+1 cycles If the register needs to be modified dynamically, the PCLK should be faster than the PWM CLK.
15:0	R/W	0x0	PWM_ACT_CYCLE Number of the active cycles in the PWM clock. 0: 0 cycle 1: 1 cycle … N: N cycles

10.11.6.18. 0x0108 + N*0x20 PWM Counter Register (Default Value: 0x0000_0000)

Offset:0x0100+0x08+N*0x20(N=0~3)			Register Name: PCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16-bit up-counter.

10.11.6.19. 0x010C + N*0x20 PWM Pulse Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0C+N*0x20(N=0~3)			Register Name: PPCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

10.11.6.20. 0x0110 + N*0x20 PWM Capture Control Register (Default Value: 0x0000_0000)

Offset:0x0100+0x10+N*0x20(N=0~3)			Register Name: CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	CRLF When capture channel captures rising edge, the current value of the 16-bit up-counter is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
3	R/W1C	0x0	CFLF When capture channel captures falling edge, the current value of the 16-bit up-counter is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE Rising edge capture trigger enable
1	R/W	0x0	CFTE Falling edge capture trigger enable
0	R/W	0x0	CAPINV Inversing the signal input from capture channel before 16-bit counter of capture channel. 0: not inverse 1: inverse

10.11.6.21. 0x0114 + N*0x20 PWM Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset:0x0100+0x14+N*0x20(N=0~3)			Register Name: CRLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	When capture channel captures rising edge, the current value of the 16-bit up-counter is latched to this register.

10.11.6.22. 0x0118 + N*0x20 PWM Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset:0x0100+0x18+N*0x20(N=0~3)			Register Name: CFLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	When the capturing channel captures the falling edge, the current value of

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			the 16-bit up-counter is latched to the register.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.12. LEDC

10.12.1. Overview

The LEDC is used to control external LED lamp.

The LEDC has the following features:

- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LED serial connect
- LED data transfer rate up to 800 kbit/s
- Configurable RGB display mode
- Non-data output default level is configurable

10.12.2. Block Diagram

Figure 10-69 shows a block diagram of the LEDC.

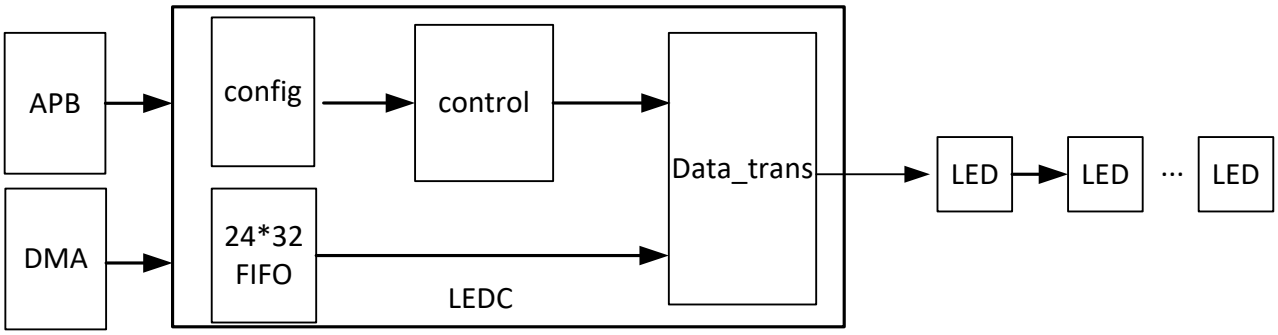


Figure 10- 69. LEDC Block Diagram

config: register configuration

control: LEDC timing control and status control

FIFO: 24*32 data FIFO

Data_trans: input data converts to 0 character and 1 character

10.12.3. Operations and Functional Descriptions

10.12.3.1. External Signals

Table 10-32 describes the external signals of the LEDC.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 10- 32. LEDC External Signals

Signal	Description	Type
LEDC	Intelligent control LED signal output	O

10.12.3.2. Clock Sources

Table 10- 33. LEDC Clock Sources

Clock Sources	Description
LEDC_CLK	24 MHz(fixed)
APB_CLK	250 MHz(changed), support range:24 MHz~250 MHz, typical value:200 MHz

10.12.3.3. LEDC Timing

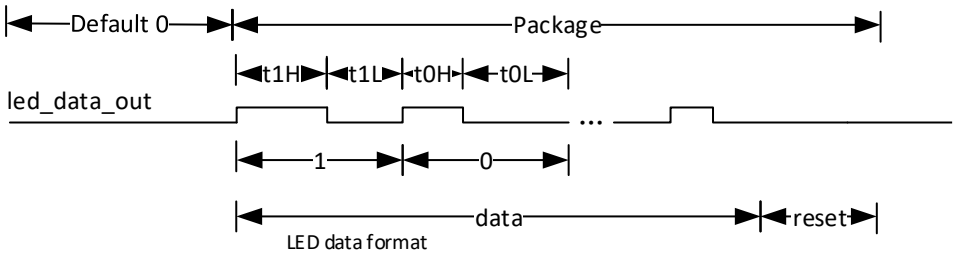


Figure 10- 70. LEDC Package Output Timing Diagram

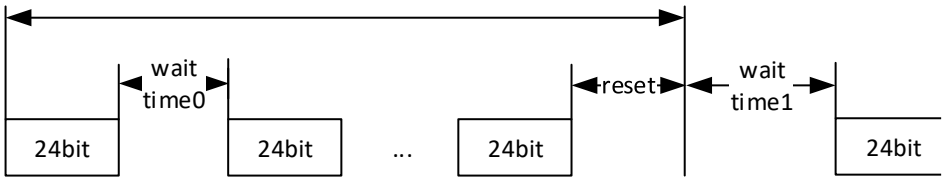


Figure 10- 71. LEDC 1-frame Output Timing Diagram

10.12.3.4. LEDC Input Data Structure

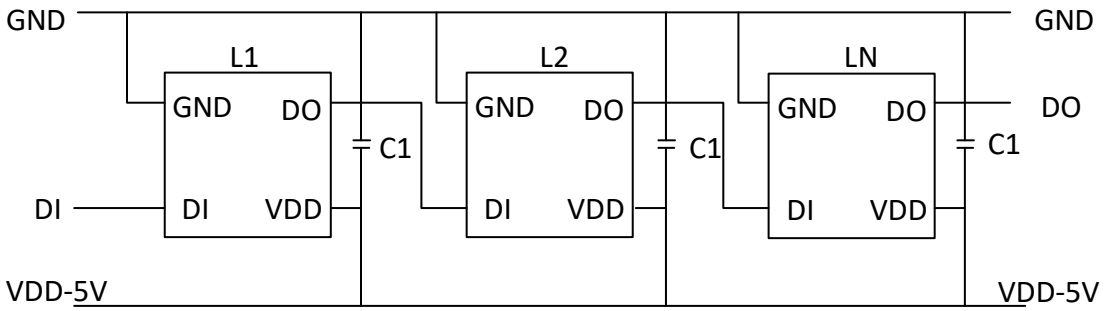
The RGB mode of LEDC data is configurable. By default, the data is sent in GRB order, and the higher bit is transmitted first.

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figure 10- 72. LEDC Input Data Structure

10.12.3.5. LEDC Typical Circuit



C1: filter capacitor of LED , usually is 100nF

Figure 10- 73. LEDC Typical Circuit

10.12.3.6. LEDC Data Input Code

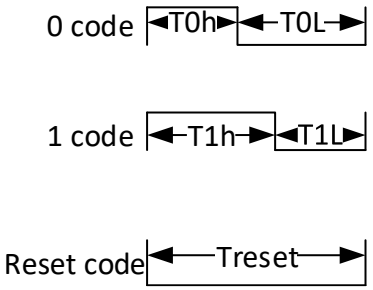


Figure 10- 74. LEDC Data Input Code

10.12.3.7. LEDC Data Transfer Time

The time parameters of typical LED datasheet are as follows.

T0H	0 code, high-level time	220 ns-380 ns
T0L	0 code, low-level time	580 ns-1.6 us
T1H	1 code, high-level time	580 ns-1.6 us
T1L	1 code, low-level time	220 ns-420 ns
RESET	Frame unit, low-level time	> 280 us

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.12.3.8. LEDC Data Transfer Mode

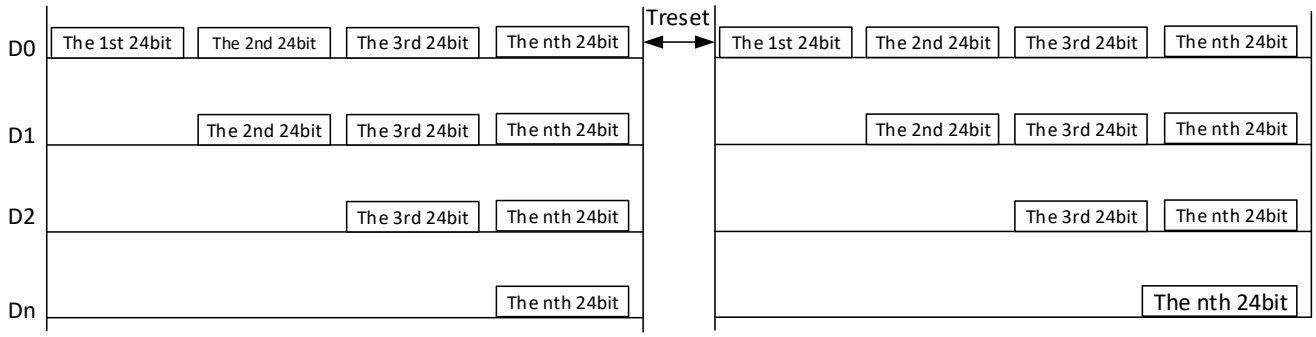


Figure 10- 75. LEDC Data Transfer Mode

10.12.3.9. LEDC Parameter

(1) PAD rate > 800 kbit/s

(2) LED number supported:

$T_{0\text{-code}}$: 800 ns~1980 ns, $T_{1\text{-code}}$: 800 ns~2020 ns

When LED reflesh rate is 30 frame/s, LED number supported is (1s/30-280 us)/((800 ns~2020 ns)*24) =1024~681.

When LED reflesh rate is 60 frame/s, LED number supported is (1s/60-280 us)/((800 ns~2020 ns)*24) =853~338.

10.12.3.10. LEDC Data Transfer

LEDC supports DMA data transfer mode or CPU data transfer mode. DMA data transfer mode is set by LEDC_DMA_EN.

- **Data transfer in DMA mode**

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, LEDC sends DMA_REQ to require DMA to transfer data from DRAM to LEDC. The maximum data transfer size in DMA mode is 16 word.(The internal FIFO level is 32.)

- **Data transfer in CPU mode**

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, LEDC sends LEDC_CPUREQ_INT to require CPU to transfer data to LEDC. The transfer data size in CPU mode is controlled by software. The internal FIFO destination address is 0x06700014. The data width is 32-bit.(The lower 24-bit is valid.)

10.12.3.11. LEDC Interrupt

Module Name	Description
FIFO_OVERFLOW_INT	FIFO overflow interrupt. The data written by external is more than the maximum storage space of LED FIFO, LEDC will be in data loss state. At this time, software needs to deal with

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

	the abnormal situation. The processing mode is as follows. Software can query LED_FIFO_DATA_REG to determine which data has been stored in internal FIFO of LEDC. LEDC performs soft_reset operation to refresh all data.
WAITDATA_TIMEOUT_INT	Wait data timeout interrupt When internal FIFO of LEDC cannot get data because of some abnormal situation, after led_wait_data_time, timeout interrupt is set, LEDC is in WAIT_DATA state, LEDC outputs a level state configured by LED_POLARITY; in the course of wait_data, if new data arrives, LEDC will continue to send data, at this time software needs to notice whether the waiting time of LEDC exceeds the operation time of reset. If the waiting time of LEDC exceeds the operation time of reset(this is equivalent to reset operation sent by LEDC), LED may enter in refresh state, data has not been sent.
FIFO_CPUREQ_INT	FIFO request CPU data interrupt When FIFO data is less than threshold, the interrupt will be reported to CPU.
LEDC_TRANS_FINISH_INT	Data transfer complete interrupt The value indicates that the data configured as total_data_length has been transferred complete.

LEDC interrupt usage scenario:

(1) CPU mode

Software can enable GLOBAL_INT_EN,FIFO_CPUREQ_INT_EN,WAITDATA_TIMEOUT_INT_EN,FIFO_OVERFLOW_INT_EN,LEDC_TRANS_FINISH_INT_EN, and cooperate with LEDC_FIFO_TRIG_LEVEL to use. When FIFO_CPUREQ_INT is set to 1, the software can configure data of LEDC_FIFO_TRIG_LEVEL to LEDC.

(2) DMA mode

Software can enable GLOBAL_INT_EN,WAITDATA_TIMEOUT_INT_EN,FIFO_OVERFLOW_INT_EN,LEDC_TRANS_FINISH_INT_EN, and cooperate with LEDC_FIFO_TRIG_LEVEL to use. When DMA receives LEDC DMA_REQ, DMA can transfer data of LEDC_FIFO_TRIG_LEVEL to LEDC.

10.12.4. Programming Guidelines

10.12.4.1. LEDC Normal Configuration Process

Step1 Configure LEDC_CLK and bus pclk.

Step2 Configure the written LEDC data.

Step3 Configure LED_T1/0_TIMING_CTRL_REG, LEDC_DATA_FINISH_CNT_REG, LED_RESET_TIMING_CTRL_REG, LEDC_WAIT_TIME_CTRL_REG, LEDC_DMA_CTRL_REG, LEDC_INTERRUPT_CTRL_REG. Configure 0-code, 1-code, reset time, LEDC waiting time, and the number of external connected LEDC and the threshold of DMA transfer data.

Step4 Configure LEDC_CTRL_REG to enable LEDC_EN, LEDC will start to output data.

Step5 When LEDC interrupt is pulled up, it indicates the configured data has transferred complete,at this time LED_EN will be set to 0, and the read&write point of LEDC FIFO is cleared to 0.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step6 Repeat step1,2,3,4 to re-execute a new round of configuration, enable LEDC_EN, LEDC will start new data transfer.

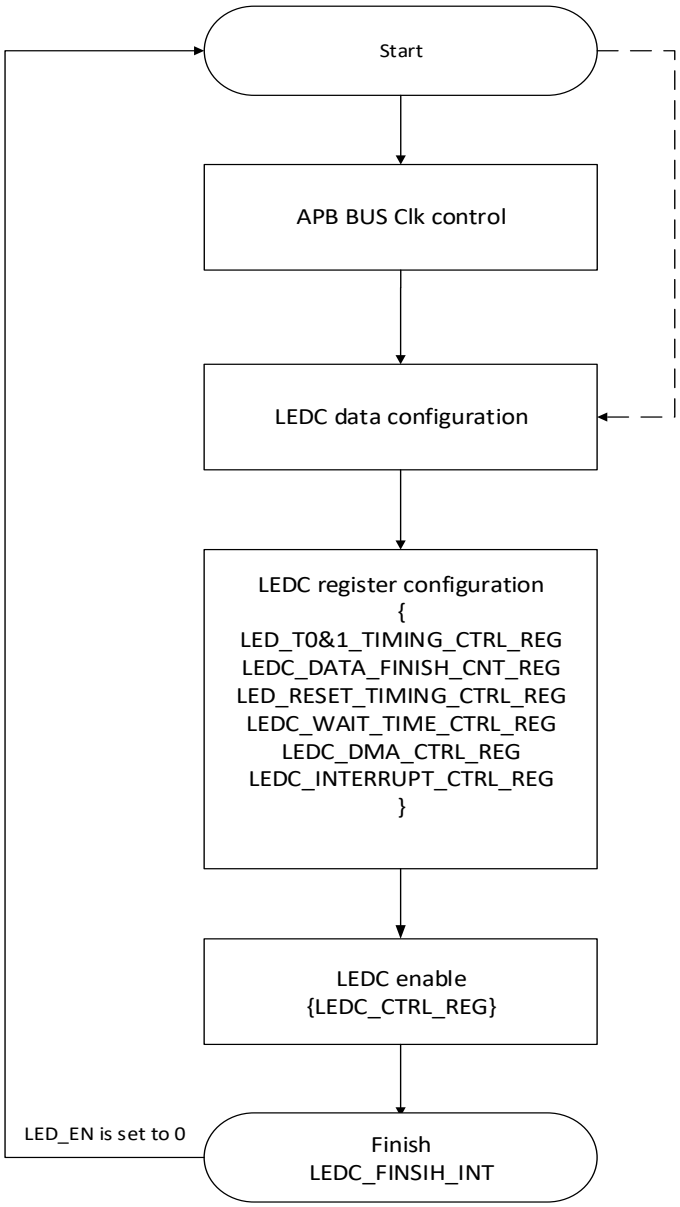


Figure 10- 76. LEDC Normal Configuration Process

10.12.4.2. LEDC Abnormal Scene Processing Flow

(1) WAITDATA_TIMEOUT Abnormal Status

Step1 WAITDATA_TIMEOUT_INT indicates internal FIFO data request of LEDC cannot obtain reponse, at this time if the default output level is low level, then external LED may think there was a reset operation and cause LED data to be flushed incorrectly.

Step2 LEDC needs be performed soft_reset operation, that is LEDC_SOFT_RESET=1; after soft_reset, LEDC_EN will be pulled-down automatically, all internal status register and control state machine will return to idle state, LEDC FIFO read &write point is cleared to 0, LEDC interrupt is cleared.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Step3 Setting reset_led_en to 1 indicates LEDC can send proactive a reset operation to ensure external LED lamp in right state.

Step4 Software reads the state of reset_led_en, when is 1, it indicates LEDC does not perform the transmission of LED reset operation; when is 0, LEDC completes the transmission of LED reset operation.

Step5 When LEDC reset operation finishes, the LEDC data and register configuration need be reoperated to start retransmission data operation.

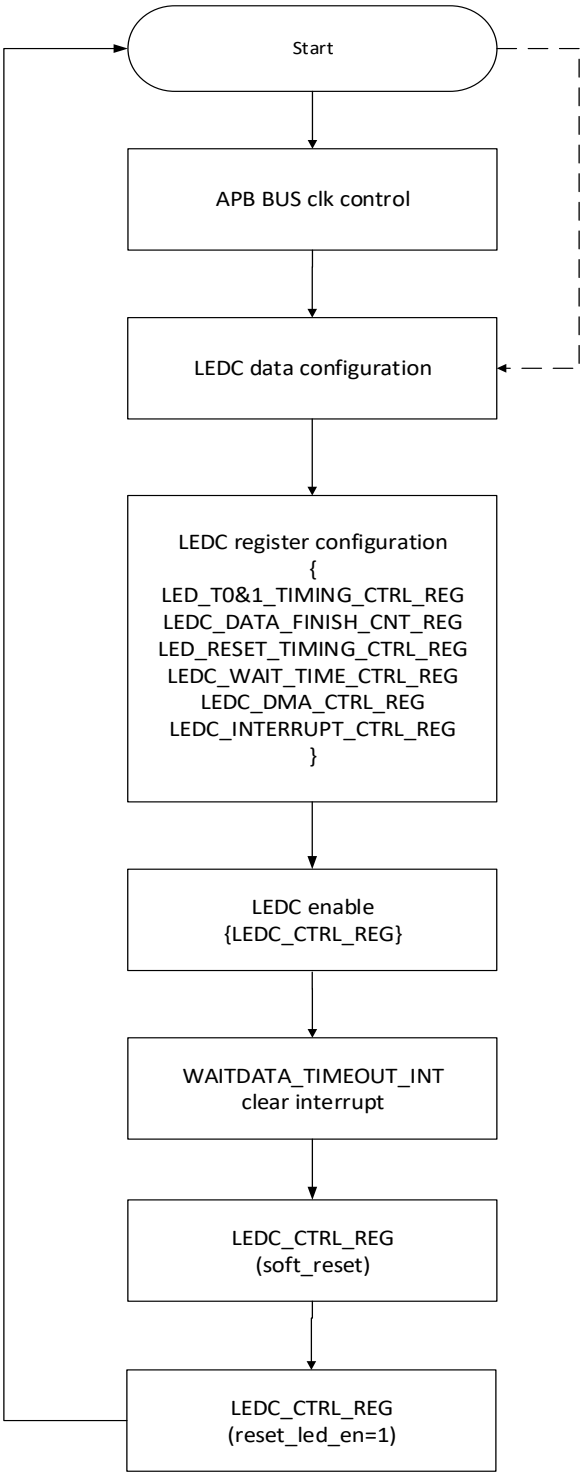


Figure 10- 77. LEDC Timeout Abnormal Processing Flow

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

(2) FIFO Overflow Abnormal Status

Step1 FIFO_OVERFLOW_INT indicates software configured data exceeds LEDC FIFO space, at this time redundant data will be lost.

Step2 Software needs read data in LEDC_FIFO_DATA_REG register to confirm the lost data.

Step3 Software re-configures the lost data to LEDC.

Step4 If software uses soft_reset operation, the operation is the same with timeout abnormal processing flow.

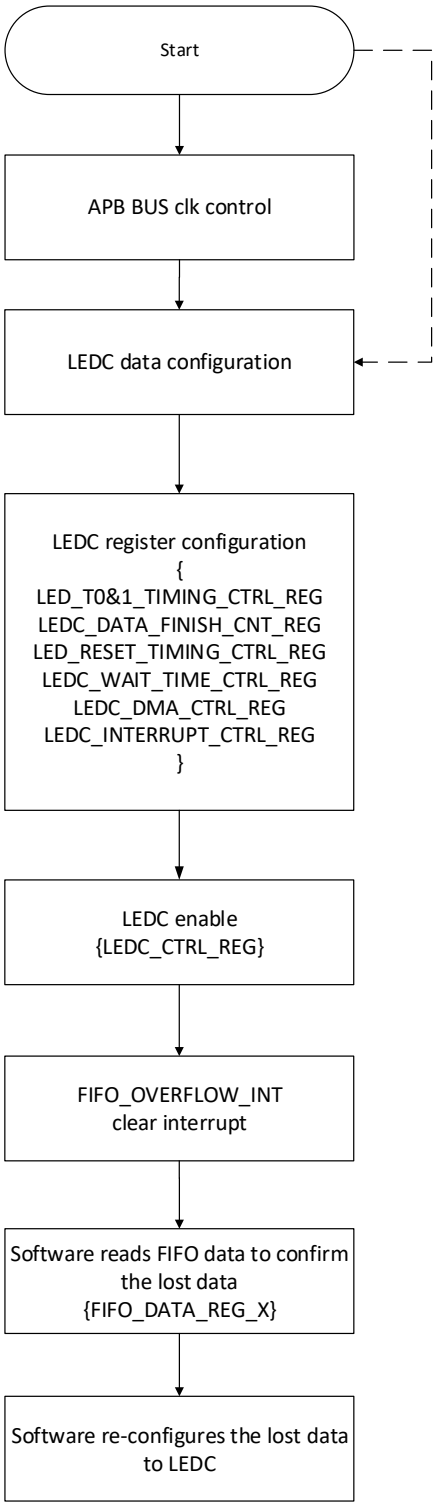


Figure 10- 78. FIFO Overflow Abnormal Processing Flow

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.12.5. Register List

Module Name	Base Address
LEDC	0x05018000

Register Name	Offset	Description
LEDC_CTRL_REG	0x0000	LEDC Control Register
LED_T1&0_TIMING_CTRL_REG	0x0004	LED T0 Timing Control Register
LEDC_DATA_FINISH_CNT_REG	0x0008	LEDC Data Finish Counter Register
LED_RESET_TIMING_CTRL_REG	0x000C	LED Reset Timing Control Register
LEDC_WAIT_TIME0_CTRL_REG	0x0010	Wait Time0 Control Register
LEDC_DATA_REG	0x0014	LEDC Data Register
LEDC_DMA_CTRL_REG	0x0018	DMA Control Register
LEDC_INT_CTRL_REG	0x001C	Interrupt Control Register
LEDC_INT_STS_REG	0x0020	Interrupt Status Register
LEDC_WAIT_TIME1_CTRL_REG	0x0028	Wait Time1 Control Register
LEDC_FIFO_DATA_REG	0x0030+4*N	LEDC FIFO Data Register

10.12.6. Register Description

10.12.6.1. 0x0000 LEDC Control Register (Default Value: 0x0000_003C)

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	TOTAL_DATA_LENGTH Total length of transfer data(range: 0 to 8K,unit:32-bit,only low 24-bit is valid) The field is recommended to be set to an integer multiple of (LED_NUM+1). If TOTAL_DATA_LENGTH is greater than (LED_NUM+1), but non integer multiple, the last frame of data will transfer data less than (LED_NUM+1).
15:11	/	/	/
10	R/W	0x0	RESET_LED_EN Write operation: Software writes 1, CPU triggers LEDC to transfer a reset to LED. **Note:** ● **Only when LEDC is in IDLE status, reset can be performed. After reset finished, the control state machine returns to the IDLE status. To return LEDC to the IDLE status, it also needs to be used with**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td></td><td></td><td></td><td>SOFT_RESET.
● When software sets the bit, software can read the bit to check if reset is complete.

Read operation:
0: LEDC completes the transmission of LED reset operation
1: LEDC does not complete the transmission of LED reset operation</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8:6</td><td>R/W</td><td>0x0</td><td>LED_RGB_MODE
000: GRB(bypass)
001: GBR
010: RGB
011: BGR
100: RBG
101: BRG
By default, software configures data to LEDC according to GRB(MSB) mode, LEDC internal combines data to output to the external LED.
Other modes configures as follows.
<table>
<tr><th>Software Input Mode</th><th>Configuration</th><th>LEDC Output Mode</th></tr>
<tr><td rowspan="6">GRB</td><td>000</td><td>GRB</td></tr>
<tr><td>001</td><td>GBR</td></tr>
<tr><td>010</td><td>RGB</td></tr>
<tr><td>011</td><td>RBG</td></tr>
<tr><td>100</td><td>BGR</td></tr>
<tr><td>101</td><td>BRG</td></tr>
<tr><td rowspan="6">GBR</td><td>000</td><td>GBR</td></tr>
<tr><td>001</td><td>GRB</td></tr>
<tr><td>010</td><td>BGR</td></tr>
<tr><td>011</td><td>BRG</td></tr>
<tr><td>100</td><td>RGB</td></tr>
<tr><td>101</td><td>RBG</td></tr>
<tr><td rowspan="6">RGB</td><td>000</td><td>RGB</td></tr>
<tr><td>001</td><td>RBG</td></tr>
<tr><td>010</td><td>GRB</td></tr>
<tr><td>011</td><td>GBR</td></tr>
<tr><td>100</td><td>BRG</td></tr>
<tr><td>101</td><td>BGR</td></tr>
<tr><td rowspan="6">RBG</td><td>000</td><td>RBG</td></tr>
<tr><td>001</td><td>RGB</td></tr>
<tr><td>010</td><td>BRG</td></tr>
<tr><td>011</td><td>BGR</td></tr>
<tr><td>100</td><td>GRB</td></tr>
</table></td></tr>
</table>

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

				101	GBR
			BGR	000	BGR
				001	BRG
				010	GBR
				011	GRB
				100	RBG
				101	RGB
			BRG	000	BRG
				001	BGR
				010	RBG
				011	RGB
				100	GBR
				101	GRB
5	R/W	0x1	LED_MSB_TOP Adjust sequence of the combined GRB data 0: LSB 1: MSB		
4	R/W	0x1	LED_MSB_G MSB control for Green data 0: LSB 1: MSB		
3	R/W	0x1	LED_MSB_R MSB control for Red data 0: LSB 1: MSB		
2	R/W	0x1	LED_MSB_B MSB control for Blue data 0:LSB 1: MSB		
1	R/W1C	0x0	LEDC_SOFT_RESET LEDC soft reset Write 1 to clear it automatically. The range of LEDC soft reset: all internal status registers, the control state machine returns to in idle status, LEDC FIFO read &write point is cleared to 0, LEDC interrupt is cleared, the affected registers are follow. 1.LEDC_CTRL_REG(LEDC_EN is cleared to 0); 2. PLL_T0&1_TIMING_CTRL_REG remains unchanged; 3. LEDC_DATA_FINISH_CNT_REG(LEDC_DATA_FINISH_CNT is cleared to 0) 4.LED_RESET_TIMING_CTRL_REG remains unchanged; 5. LEDC_WAIT_TIME_CTRL_REG remains unchanged; 6. LEDC_DMA_CTRL_REG remains unchanged; 7. LEDC_INTERRUPT_CTRL_REG remains unchanged; 8.LEDC_INT_STS _REG is cleared to 0; 9. LEDC_CLK_GATING_REG remains unchanged;		

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10.LEDC_FIFO_DATA_REG remains unchanged;
0	R/W	0x0	LEDC_EN LEDC Enable 0: Disable 1: Enable That the bit is enabled indicates LEDC can be started when LEDC data finished transmission or LEDC_EN is cleared to 0 by hardware in LEDC_SOFT_RESET situation.

10.12.6.2. 0x0004 LED_T01_Timing Control Register (Default Value: 0x0286_01D3)

Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:21	R/W	0x14	T1H_TIME LED T1H time Unit: cycle(24MHz), T1H_TIME =42ns*(N+1) The default value is 800ns, the range is 80ns~2560ns. N: 1~3F When is 0, T1H_TIME = 3F
20:16	R/W	0x6	T1L_TIME LED T1L time Unit: cycle(24MHz), T1L_TIME =42ns*(N+1) The default value is 280ns, the range is 80ns~1280ns. N: 1~1F When is 0, T1L_TIME = 1F
15:11	/	/	/
10:6	R/W	0x7	T0H_TIME LED T0h time Unit: cycle(24MHz), T0H_TIME =42ns*(N+1) The default value is 280ns, the range is 80ns~1280ns. N: 1~1F When is 0, T0H_TIME = 1F
5:0	R/W	0x13	T0L_TIME LED T0l time Unit: cycle(24MHz), T0L_TIME =42ns*(N+1) The default value is 800ns, the range is 80ns~2560ns. N: 1~3F When is 0, T0L_TIME = 3F

10.12.6.3. 0x0008 LEDC Data Finish Counter Register (Default Value: 0x1D4C_0000)

Offset: 0x0008	Register Name: LEDC_DATA_FINISH_CNT_REG

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x1d4c	LED_WAIT_DATA_TIME The value is the time that internal FIFO in LEDC is waiting data, when the setting time is exceeded , LEDC will send waitdata_timeout_int interrupt. (This is a abnormal situation, software needs to reset LEDC.) The value is 300 us by default. The adjust range is from 80 ns to 655 us, led_wait_data_time=42 ns*(N+1) N: 1~1FFF When the field is 0, LEDC_WAIT_DATA_TIME=1FFF
15:13	/	/	/
12:0	R	0x0	LED_DATA_FINISH_CNT The value is the total LED data that have been sent .(Range: 0~8k)

10.12.6.4. 0x000C LED Reset Timing Control Register(Default Value: 0x1D4C_0000)

Offset: 0x000C			Register Name: LED_RESET_TIMING_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1d4c	TR_TIME Reset time control of LED lamp Unit: cycle(24 MHz), tr_time=42ns*(N+1) The default value is 300 us. The adjust range is from 80 ns to 327 us. N: 1~1FFF When the field is 0, TR_TIME=1FFF
15:10	/	/	/
9:0	R/W	0x0	LED_NUM The value is the number of external LED lamp. Maximum up to 1024. The default value 0 indicates that 1 LED lamp is external connected. The range is from 0 to 1023.

10.12.6.5. 0x0010 LEDC Wait Time 0 Control Register (Default Value: 0x0000_00FF)

Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	WAIT_TIM0_EN WAIT_TIME0 enable When it is 1, the controller automatically insert waiting time before LED package data. 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
7:0	R/W	0xFF	TOTAL_WAIT_TIME0 Waiting time between 2 LED datas, LEDC output is low level. The adjust range is from 80 ns to 10 us. wait_time0=42 ns*(N+1) Unit: cycle(24 MHz) N: 1~FF When the field is 0, TOTAL_WAIT_TIME1E=FF.

10.12.6.6. 0x0014 LEDC Data Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LEDC_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	LEDC DATA LED display data(the lower 24-bit is valid)

10.12.6.7. 0x0018 LEDC DMA Control Register (Default: 0x0000_002F)

Offset: 0x0018			Register Name: LEDC_DMA_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x1	LEDC_DMA_EN LEDC DMA request enable 0: Disable request of DMA transfer data 1: Enable request of DMA transfer data
4:0	R/W	0x0F	LEDC_FIFO_TRIG_LEVEL The remaining space of internal FIFO in LEDC The internal FIFO in LEDC is 24*32. When the remaining space of internal FIFO in LEDC is more than or equal to LEDFIFO_TRIG_LEVEL, DMA or CPU request will generate. The default value is 15. The adjust value is from 1 to 31. The recommended configuration is 7 or 15. When the configuration value is 0, LEDFIFO_TRIG_LEVEL=F.

10.12.6.8. 0x001C LEDC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LEDC_INTERRUPT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	GLOBAL_INT_EN Global interrupt enable 0: Disable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
4	R/W	0x0	FIFO_OVERFLOW_INT_EN FIFO overflow interrupt enable When the data written by software is more than internal FIFO level of LEDC, LEDC is in data loss state. 0: Disable 1: Enable
3	R/W	0x0	WAITDATA_TIMEOUT_INT_EN The internal FIFO in LEDC cannot get data because of some abnormal situation, after the time of led_wait_data_time, the interrupt will be enabled. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	FIFO_CPUREQ_INT_EN FIFO request CPU data interrupt enable 0: Disable 1: Enable
0	R/W	0x0	LED_TRANS_FINISH_INT_EN Data transmission complete interrupt enable 0: Disable 1: Enable

10.12.6.9. 0x0020 LEDC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: LEDC_INT_STS _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x1	FIFO_EMPTY FIFO empty status flag
16	R	0x0	FIFO_FULL FIFO full status flag
15:10	R	0x0	FIFO_WLW FIFO internal valid data depth It indicates the space FIFO has been occupied.
9:5	/	/	/
4	R/W1C	0x0	FIFO_OVERFLOW_INT FIFO overflow interrupt The data written by external is more than the maximum storage space of LED FIFO, LEDC will be in data loss state. At this time, software needs to deal with the abnormal situation. The processing mode is as follows. Software can query LED_FIFO_DATA_REG to determine which data has been stored in internal FIFO of LEDC. LEDC performs soft_reset operation to refresh all data.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: FIFO not overflow 1: FIFO overflow
3	R/W1C	0x0	WAITDATA_TIMEOUT_INT When internal FIFO of LEDC cannot get data because of some abnormal situation, after led_wait_data_time, timeout interrupt is set, LEDC is in WAIT_DATA state, LEDC outputs a level state configured by LED_POLARITY; in the course of wait_data, if new data arrives, LEDC will continue to send data, at this time software needs to notice whether the waiting time of LEDC exceeds the operation time of reset. If the waiting time of LEDC exceeds the operation time of reset(this is equivalent to reset operation sent by LEDC), LED may enter in refresh state, data has not been sent. 0: LEDC not timeout 1: LEDC timeout
2	/	/	/
1	R/W1C	0x0	FIFO_CPUREQ_INT FIFO request CPU data interrupt When FIFO data is less than threshold, the interrupt will be reported to CPU. 0: FIFO does not request that CPU transfers data 1: FIFO requests that CPU transfers data
0	R/W1C	0x0	LED_TRANS_FINISH_INT Data transfer complete interrupt The value indicates that the data configured as total_data_length has been transferred complete. 0: Data not transfer complete 1: Data transfer complete

10.12.6.10. 0x0028 LEDC Wait Time 1 Control Register (Default Value: 0x1FF_FFFF)

Offset: 0x0028			Register Name: LEDC_WAIT_TIME1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	WAIT_TIM1_EN 0: Disable 1: Enable WAIT_TIME1 enable When the bit is 1, the controller automatically insert waiting time before LED frame data.
30:0	R/W	0x1FF_FFFF	TOTAL_WAIT_TIME1 Waiting time between 2 frame datas, LEDC output is low level. The adjust range is from 80 ns to 85 s. wait_time1=42 ns*(N+1) Unit: cycle(24 MHz) N: 80~7FFF_FFFF

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.12.6.11. 0x0030+N*0x4 LEDC FIFO Data Register X (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x4(N=0~31)			Register Name: LEDC_FIFO_DATA_X
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	LEDC_FIFO_DATA_X Internal FIFO data of LEDC The lower 24-bit is valid.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13. EMAC

10.13.1. Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with RMII/RGMII interface in both full and half duplex mode. The internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 2 KB TXFIFO and 8 KB RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC has the following features:

- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Supports RMII/RGMII PHY interface
- Supports MDIO
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

10.13.2. Block Diagram

The block diagram of EMAC is shown below.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

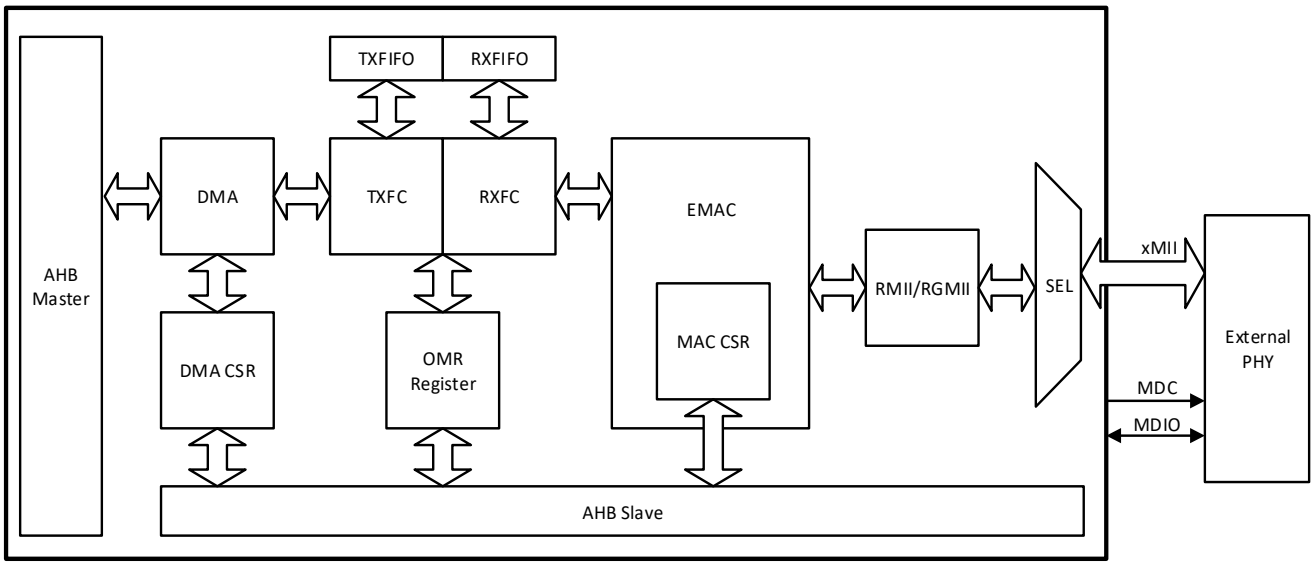


Figure 10- 79. EMAC Block Diagram

10.13.3. Operations and Functional Descriptions

10.13.3.1. External Signals

Table 10-34 describes the pin mapping of EMAC.

Table 10- 34. EMAC Pin Mapping

Pin Name	RGMII	RMII
RGMII0_RXD3/RMII0_NULL	RXD3	/
RGMII0_RXD2/RMII0_NULL	RXD2	/
RGMII0_RXD1/RMII0_RXD1	RXD1	RXD1
RGMII0_RXD0/RMII0_RXD0	RXD0	RXD0
RGMII0_RXCK/RMII0_NULL	RXCK	/
RGMII0_RXCTL/RMII0_CRS_DV	RXCTL	CRS_DV
RGMII0_CLKIN /RMII0_RXER	CLKIN	RXER
RGMII0_TXD3/RMII0_NULL	TXD3	/
RGMII0_TXD2/RMII0_NULL	TXD2	/
RGMII0_TXD1/RMII0_TXD1	TXD1	TXD1
RGMII0_TXD0/RMII0_TXD0	TXD0	TXD0
RGMII0_TXCK/RMII0_TXCK	TXCK	TXCK
RGMII0_TXCTL/RMII0_TXEN	TXCTL	TXEN
MDC0	MDC	MDC
MDIO0	MDIO	MDIO
EPHY0_25	EPHY0_25	EPHY0_25

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Table 10-35 describes the pin list of RGMII.

Table 10- 35. EMAC RGMII Pin List

Pin Name	Description	Type
RGMII0_TXD[3:0]	EMAC RGMII transmit data	O
RGMII0_TXCTL	EMAC RGMII transmit control	O
RGMII0_TXCK	EMAC RGMII transmit clock	O
RGMII0_RXD[3:0]	EMAC RGMII receive data	I
RGMII0_RXCTL	EMAC RGMII receive control	I
RGMII0_RXCK	EMAC RGMII receive clock	I
RGMII0_CKIN	EMAC RGMII 125M reference clock input	I
MDC0	EMAC management data clock	O
MDIO0	EMAC management data input output	I/O
EPHY0_25	25 MHz output for EMAC PHY	O

Table 10-36 describes the pin list of RMII.

Table 10- 36. EMAC RMII Pin List

Pin Name	Description	Type
RMII0_TXD[1:0]	EMAC RMII transmit data	O
RMII0_TXEN	EMAC RMII transmit enable	O
RMII0_TXCK	EMAC RMII 50M reference clock input	I
RMII0_RXD[1:0]	EMAC RMII receive data	I
RMII0_CRS_DV	EMAC RMII receive data valid	I
RMII0_RXER	EMAC RMII receive error	I
MDC0	EMAC management data clock	O
MDIO0	EMAC management data input output	I/O
EPHY0_25	25 MHz output for EMAC PHY	O

10.13.3.2. Clock Sources

Table 10-37 describes the clock of EMAC.

Table 10- 37. EMAC Clock Characteristics

Clock Name	Description	Type
RGMII0_TXCK/RMII0_TXCK	In RGMII mode, output 2.5 MHz/25 MHz/125 MHz. In RMII mode, input 50 MHz.	O/I
RGMII0_RXCK	In RGMII mode, input 2.5 MHz/25 MHz/125 MHz. In RMII mode, no input.	I

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

RGMII0_CLKIN	In RGMII mode, input 125M Reference Clock In RMII mode, no clock.	I

10.13.3.3. Typical Application

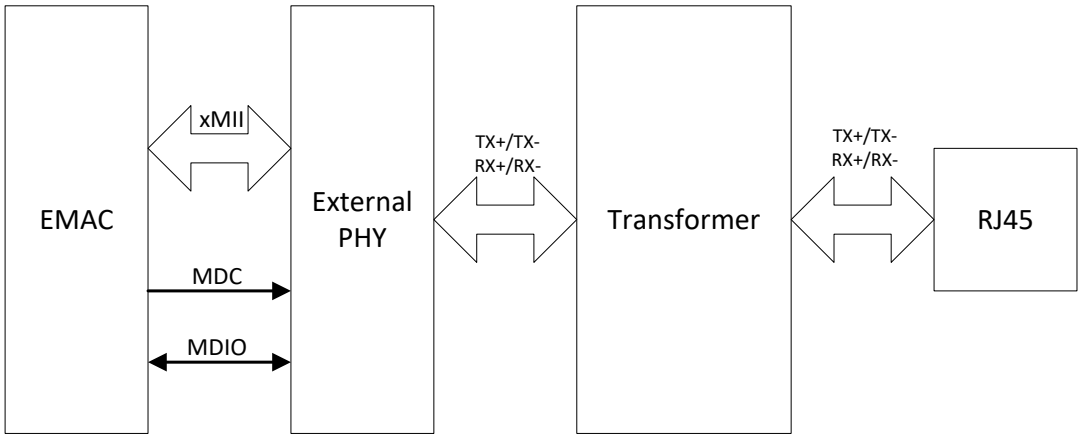


Figure 10- 80. EMAC Typical Application

10.13.3.4. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 10-81. The address of each descriptor must be 32-bit aligned.

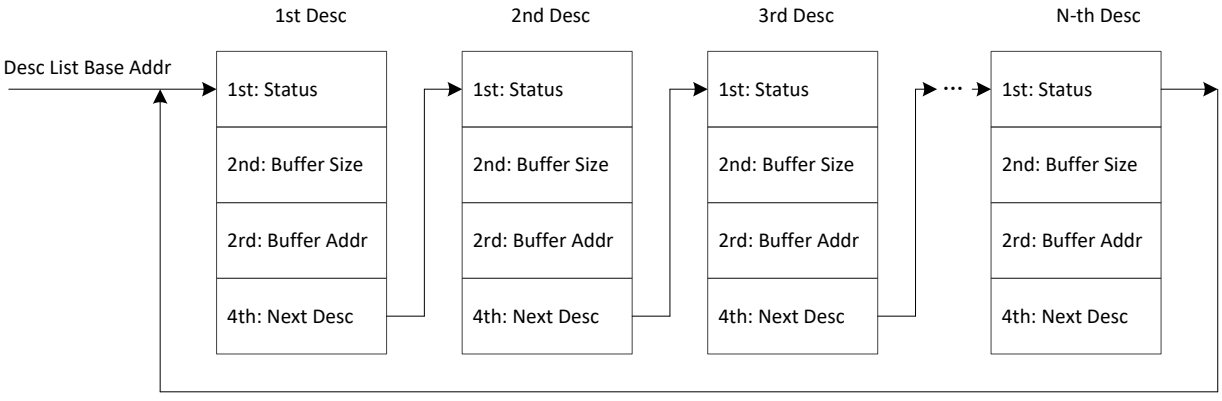


Figure 10- 81. EMAC RX/TX Descriptor List

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.3.5. Transmit Descriptor

10.13.3.5.1. 1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all datas in the buffer of current descriptor are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of header of transmitted frame is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of payload of transmitted frame is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

10.13.3.5.2. 2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

	When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

10.13.3.5.3. 3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

10.13.3.5.4. 4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

10.13.3.6. Receive Descriptor

10.13.3.6.1. 1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When setting the bit, the current descriptor can be used by DMA. This bit is cleared by DMA when the complete frame is received or the buffer of current descriptor is full.
30	RX_DAF_FAIL When setting the bit, the current frame does not pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When setting the bit, the current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When setting the bit, the current fame does not pass SA filter.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

12	Reserved
11	RX_OVERFLOW_ERR When setting the bit, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When setting the bit, current descriptor is the first descriptor for current frame.
8	LAST_DESC When setting the bit, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When setting the bit, the checksum of the frame header is wrong.
6	RX_COL_ERR When setting the bit, there is a late collision during reception in half-duplex mode.
5	Reserved
4	RX_LENGTH_ERR When setting the bit, the length of current frame is wrong.
3	RX_PHY_ERR When setting the bit, the receive error signal from PHY is asserted during reception.
2	Reserved
1	RX_CRC_ERR When setting the bit, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When setting the bit, the checksum or length of the payload of received frame is wrong.

10.13.3.6.2. 2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When setting the bit, and a frame has been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer is specified by current descriptor.

10.13.3.6.3. 3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.3.6.4. 4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

10.13.4. Register List

Module Name	Base Address
EMAC0	0x05020000

Register Name	Offset	Description
EMAC_BASIC_CTL0	0x0000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x0004	EMAC Basic Control Register1
EMAC_INT_STA	0x0008	EMAC Interrupt Status Register
EMAC_INT_EN	0x000C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x0010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x0014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x001C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x0020	EMAC Transmit Descriptor List Address Register
EMAC_RX_CTL0	0x0024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x0028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x0034	EMAC Receive Descriptor List Address Register
EMAC_RX_FRM_FLT	0x0038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x0040	EMAC Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC Hash Table Register1
EMAC_MII_CMD	0x0048	EMAC Management Interface Command Register
EMAC_MII_DATA	0x004C	EMAC Management Interface Data Register
EMAC_ADDR_HIGH0	0x0050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x0054	EMAC MAC Address Low Register0
EMAC_ADDR_HIGHx	0x0050+0x08*N(N=1~7)	EMAC MAC Address High RegisterN(N:1~7)
EMAC_ADDR_LOWx	0x0054+0x08*N(N=1~7)	EMAC MAC Address Low RegisterN(N:1~7)
EMAC_TX_DMA_STA	0x00B0	EMAC Transmit DMA Status Register
EMAC_TX_CUR_DESC	0x00B4	EMAC Current Transmit Descriptor Register
EMAC_TX_CUR_BUF	0x00B8	EMAC Current Transmit Buffer Address Register
EMAC_RX_DMA_STA	0x00C0	EMAC Receive DMA Status Register
EMAC_RX_CUR_DESC	0x00C4	EMAC Current Receive Descriptor Register
EMAC_RX_CUR_BUF	0x00C8	EMAC Current Receive Buffer Address Register
EMAC_RGMII_STA	0x00D0	EMAC RGMII Status Register

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.5. Register Description

10.13.5.1. 0x0000 EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

10.13.5.2. 0x0004 EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: EMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA Priority 0: Same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset All clock inputs must be valid before soft reset. This bit is cleared internally when the reset operation is completed fully. Before writing any register, this bit should read a 0.

10.13.5.3. 0x0008 EMAC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008	Register Name: EMAC_INT_STA

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First Data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this asserted, the RX DMA cannot acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when writing to RX_DMA_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame is transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Write ‘1’ to clear it.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear it.
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear it.
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to TX_DMA_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear it.
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear it.

10.13.5.4. 0x000C EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: EMAC_INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

10.13.5.5. 0x0010 EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010	Register Name: EMAC_TX_CTL0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disable, the transmit will continue until the current transmit finishes.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

10.13.5.6. 0x0014 EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0.
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission 1: Start and run TX DMA
29:11	/	/	/
10:8	R/W	0x0	TX_TH Threshold value of TX DMA FIFO When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, the full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Enable 1: Disable

10.13.5.7. 0x001C EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before writing register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME.
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

10.13.5.8. 0x0020 EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.5.9. 0x0024 EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

10.13.5.10. 0x0028 EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will not work. It is cleared internally and always read a 0.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable, base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 **Note: Only valid when RX_MD == 0, the full frames with a length less than the threshold are transferred automatically.**
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When setting, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Disable

10.13.5.11. 0x0034 EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

10.13.5.12. 0x0038 EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive all
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass frames whose SA field matches SA MAC address registers 1: Pass frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it passes the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

10.13.5.13. 0x0040 EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: EMAC_RX_HASH0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

10.13.5.14. 0x0044 EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: EMAC_RX_HASH1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.5.15. 0x0048 EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved **Note: MDC Clock is divided from AHB clock.**
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/W	0x0	MII_BUSY 0: Write no valid, read 0 indicates finish in read or write operation 1: Write start read or write operation, read 1 indicates busy.

10.13.5.16. 0x004C EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

10.13.5.17. 0x0050 EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The upper 16 bits of the 1st MAC address.

10.13.5.18. 0x0054 EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

10.13.5.19. 0x0050+0x08*N EMAC MAC Address High Register N (Default Value: 0x0000_0000)

Offset: 0x0050+0x08*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16 bits of the MAC address.

10.13.5.20. 0x0054+0x08*N EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x08*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32 bits of MAC address N (N: 1~7).

10.13.5.21. 0x00B0 EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, when reset or disable TX DMA 001: RUN_FETCH_DESC, fetching TX DMA descriptor 010: RUN_WAIT_STA, waiting for the status of TX frame 011: RUN_TRANS_DATA, passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

10.13.5.22. 0x00B4 EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

10.13.5.23. 0x00B8 EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer.

10.13.5.24. 0x00C0 EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, when reset or disable RX DMA 001: RUN_FETCH_DESC, fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, waiting for frame 100: SUSPEND, RX descriptor unavailable 101: RUN_CLOSE_DESC, closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, passing frame from host memory to RX DMA FIFO

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

10.13.5.25. 0x00C4 EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive descriptor

10.13.5.26. 0x00C8 EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive DMA buffer

10.13.5.27. 0x00D0 EMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: EMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: down 1: up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Contents

Chapter 11 Security System 1058
11.1. Crypto Engine 1058
11.1.1. Overview 1058
11.1.2. Block Diagram 1059
11.1.3. Operations and Functional Descriptions 1060
11.1.4. Register List 1070
11.1.5. Register Description 1070
11.2. Security ID 1076

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Figures

Figure 11- 1. CE Block Diagram 1059
Figure 11- 2. Task Chaining of Hash Algorithms and Random Bit Generator Algorithms 1061
Figure 11- 3. Task Chaining of Symmetrical Algorithms and Asymmetrical Algorithms 1064

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 11 Security System

11.1. Crypto Engine

11.1.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithm accelerator. It supports kinds of symmetric, asymmetric, Hash, and RNG algorithms. There are two software interfaces for secure and non-secure world each. The software interface is simple for configuration, only setting interrupt control, task description address and load tag. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels, and has an internal DMA controller to transfer data between CE and memory.

The CE has the following features:

- Symmetrical algorithms
  - Supports AES, XTS-AES, DES, 3DES, SM4
  - 128-, 192-, 256-bit key size for AES
  - ECB, CBC, CTR, CTS, OFB, CFB, CBC-MAC, GCM modes for AES
  - AES-CFB mode supports CFB1, CFB8, CFB64, CFB128
  - AES-CTR supports CTR16, CTR32, CTR64, CTR128
  - 256-bit, 512-bit key for XTS-AES
  - ECB, CBC, CTR, CBC-MAC modes for DES
  - DES-CTR mode supports CTR16, CTR32, CTR64
- Hash algorithms
  - Supports MD5, SHA1, SHA224, SHA256, SHA384, SHA512, SM3, HMAC-SHA1, HMAC-SHA256
  - Supports hardware padding
- Asymmetrical algorithms
  - Supports RSA, ECC, SM2
  - RSA512/1024/2048/3072/4096-bit
  - ECC160/224/256/384/521-bit
- Radom bit generator(RBG) algorithms
  - Hardware PRNG with 175-bit seed width. Output aligns with 5 words
  - Hardware TRNG. Output aligns with 8 words
  - HASH-DRBG (SHA1, SHA256, SHA512)
  - Instantiate/Reseed/Generate/Uninstantiate 4 process
  - prediction resistance requests

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

- 8 separate suits of internal state
- Maximum 2^32 BYTE length of Entropy input, Nonce, Personalization, Additional input, and length is multiple of word

- Security strategy and system feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, which can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
  - Supports task chain mode for each request. Task or task chain are executed at request order
  - 8 scatter group(sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, donot know the existence of each other
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other

11.1.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

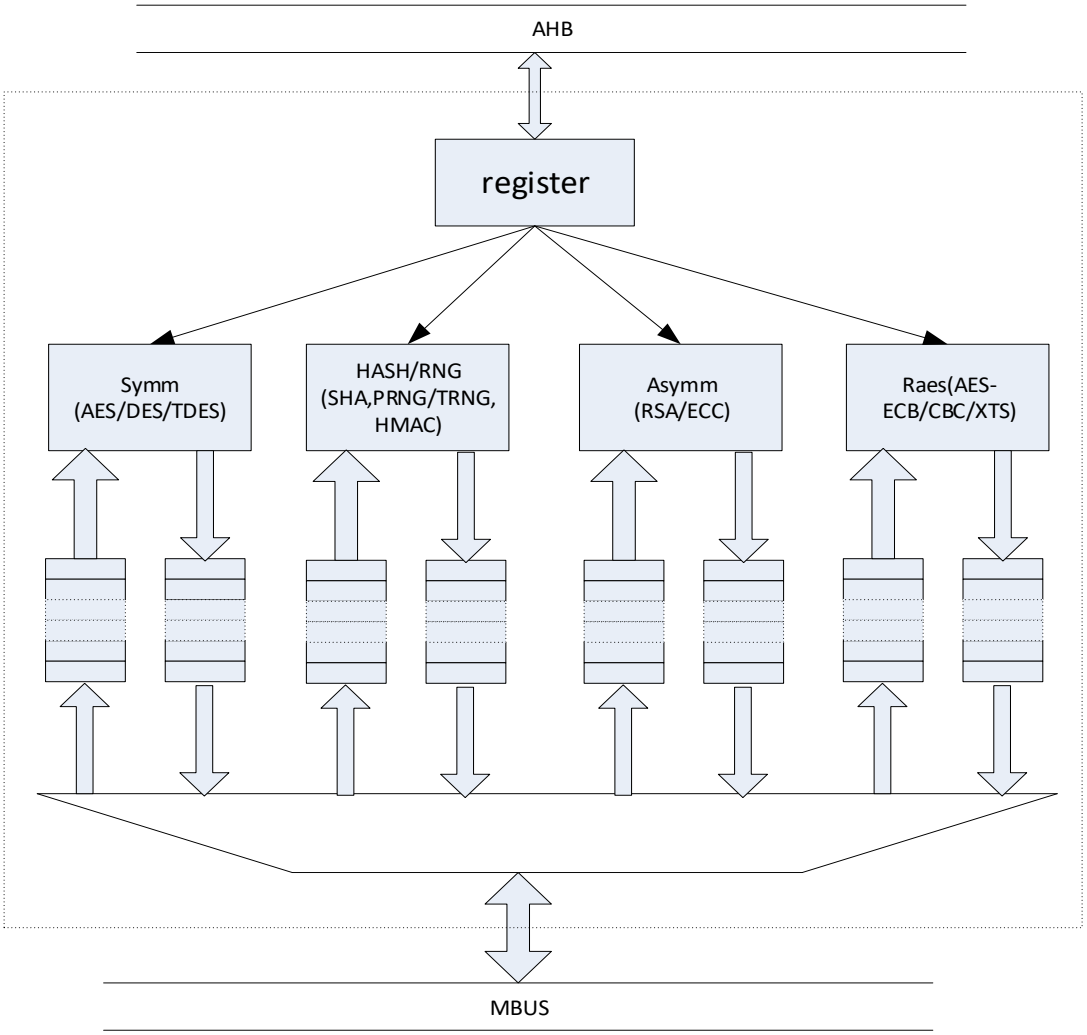


Figure 11- 1. CE Block Diagram

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.3. Operations and Functional Descriptions

11.1.3.1. Task Descriptor of Hash Algorithms and RBG Algorithms

The task descriptor is data written by software to a contiguous space in memory. The data describes the various properties of a task, such as algorithm type, mode, subcommand, key address, data source address, the data size read from data source, abstract destination address, the written destination data size, and the information of other tasks. First, we configures the task descriptor by software; then we operates the registers of CE to start this task. After the task starts, CE will read task descriptor based on the address of the task descriptor configured in register, and perform the task one time based on the described properties.

In applications, the “NEXT TASK ADDR” field can be configured as the starting address of the next task descriptor, to concatenate multi task descriptors into a task chain. After starting the first task, CE will perform every task in order until the “NEXT TASK ADDR” field is invalid (that is 0).

The HASH/RBG algorithms and Symmetrical/Asymmetrical algorithms use the different descriptor structure, separately.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

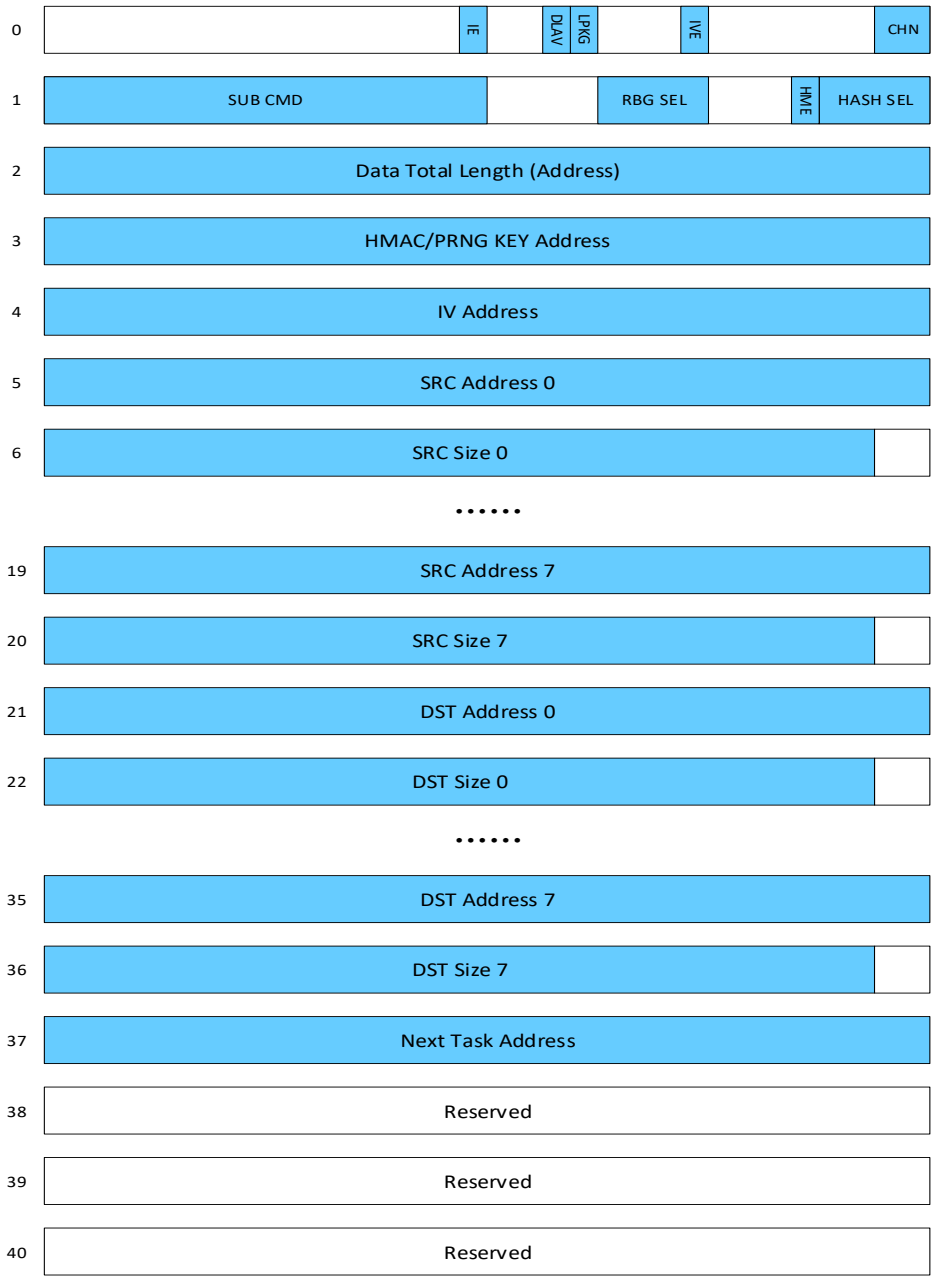


Figure 11- 2. Task Chaining of Hash Algorithms and Random Bit Generator Algorithms

The detail structures are as follows.

No.	Descriptor	Name	Width	Description
0	CTRL	CHN	[1:0]	Channel ID
		IVE	[8]	IV mode enable, active high
		LPKG	[12]	Last package flag, active high

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

		DLAV	[13]	Data length valid For last package, the bit needs be configured. For non last package, the bit needs not be configured. (Please configure it as 0 in PRNG/TRNG/DRBG .) 1: DLA means the WORD address where data total length (by bits) is saved. 0: DLA means the value of message total length (by bits).
		IE	[16]	Interrupt enable for current task, active high
1	CMD	HASH SEL	[3:0]	Hash algorithms select 0: MD5 1: SHA1 2: SHA224 3: SHA256 4: SHA384 5: SHA512 6: SM3 Other: Reserved
		HME	[4]	HMAC mode enable, active high
		RGB SEL	[11:8]	RGB algorithms select 0: No RGB use 1: PRNG 2: TRNG 3: DRBG Other: Reserved
		SUB CMD	[31:16]	Sub-command in a specific algorithms
2	DLA	DLA	[31:0]	Data length OR its address. For last package, the field needs be configured. For non last package, the field needs not be configured. (Not used in PRNG/TRNG/DRBG.) When DLAV=1, here is the WORD address where data total length (by bits) is saved. When DLAV=0, here is the value of message total length (by bits)
3	KA	KA	[31:0]	KEY address The WORD address where HMAC KEY or PRNG KEY is saved.
4	IVA	IVA	[31:0]	IV address The WORD address where IV is saved.
5+2*x	SRCAx	SRCAx	[31:0]	Source data address x The WORD address where source datax is saved.
6+2*x	SRCSx	SRCSx	[31:2]	Source data address x The length (by words) of source datax. If the length is less than 1 word, it will calculate as 1 word. except the last word of total HASH message can be non-integer word, others must be integer word.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

21+2*x	DSTAx	DSTAx	[31:0]	Output data address x The WORD address where output datax is saved.
22+2*x	DSTSx	DSTSx	[31:2]	Source data address x The Length (by words) of source datax.
37	NTA	NTA	[31:0]	Next task address The WORD address where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 30'h0.
38	Reserved	Reserved	/	/
39	Reserved	Reserved	/	/
40	Reserved	Reserved	/	/

11.1.3.2. Specific in DRBG Base on HASH/RBG Task Descriptor

11.1.3.2.1. Sub-Cmd in DRBG

Name	Width	Description
CMD	[2:0]	Process Command 0: Instantiate 1: Reseed 2: Generate 3: Uninstantiate
/	[3]	/
Internal States ID	[6:4]	Internal States ID: 0-7
/	[7]	/
PRR	[12]	Prediction Resistance Request. Active HIGH.

11.1.3.2.2. SRCAx/SRCSx in DRBG

Name in Basic HASH	Width	Description In DRBG
SRCA0	[31:0]	Entropy Input Address
SRCS0	[31:0]	Entropy Input Length (By Bytes), should be multiple of 4
SRCA1	[31:0]	Nonce Address
SRCS1	[31:0]	Nonce Length (By Bytes), should be multiple of 4
SRCA2	[31:0]	Personalization Address
SRCS2	[31:0]	Personalization Length (By Bytes) , should be multiple of 4
SRCA3	[31:0]	Additional Input Address
SRCS3	[31:0]	Additional Input Length (By Bytes) , should be multiple of 4

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.3.3. Task Descriptor of Symmetrical Algorithms and Asymmetrical Algorithms

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

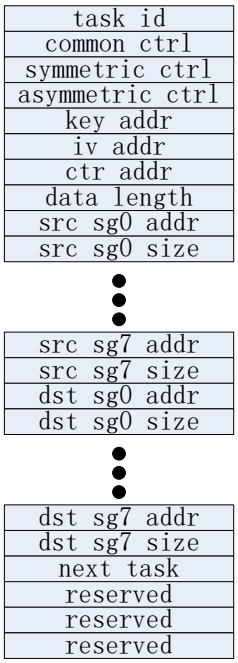


Figure 11- 3. Task Chaining of Symmetrical Algorithms and Asymmetrical Algorithms

Task chaining id supports 0~3.

The key addr field is address for the key of each algorithm, also for extension feature micro codes address. **Must be word address.**

The iv addr field is tweak value address for XTS.

The ctr addr is address for the IV of next block. **Must be word address.**

The src/dst sgX adr field indicates 32-bit address for source and destination data. **Must be word address.**

The src/dst sgX size field indicates size for each sg respectively.

The next task field should be set to 0 when no next task, else set to the descriptor of next task.

11.1.3.3.1. Task Descriptor Queue Common Control

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len The field is used as the outcome bit length of CBC-MAC when in CBC-MAC mode. The field also is used as the tag_len of GCM/OCB mode.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0x0	Algorithm Type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3： SM4 …. 0x20: RSA 0x21: ECC 0x22: SM2 … 0x30: RAES Others: Reserved

11.1.3.3.2. Task Descriptor Queue Symmetric Control

Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	no_modk 0: have module key derivation function 1: no module key derivation function
25:24	/	/	/
23:20	R/W	0x0	KEY_SELECT key select for AES/SM4/3DES （3DES only configured as 0,or 8-15） 0: Select input CE_KEYx (Normal Mode) 1: Select {SSK} 2: Select {HUK} 3-7: Reserved 8-15: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1 01: CFB8 10: CFB64 11: CFB128
17	/	/	/

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

16	R/W	0x0	AES CTS last package flag When setting to '1', it means this is the last package for CTS mode(the size of the last package >128bit). The bit also is used as the gcm_last/ocb_last for GCM/OCB mode.
15:14	/	/	/
13	R/W	0x0	xts_last 0: not last block for XTS 1: last block for XTS
12	R/W	0x0	xts_first 0: not first block for XTS 1: first block for XTS
11:8	R/W	0x0	Operation Mode for Symmetric AES/DES/3DES/RAES Modes DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC/XTS. 0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: CipherText Stealing (CTS) mode 0100: Output feedback (OFB) mode 0101: Cipher feedback (CFB) mode 0110: CBC-MAC mode 0111: OCB mode 1000: GCM mode 1001: XTS mode Others: Reserved
7:6	/	/	/
5:4	R/W	0x0	gcm_iv_mode[1:0] gcm_iv_mode[0]: value 1 show the last req for iv calculate gcm_iv_mode[1]: 0 :no GHASH calculate mode 1: GHASH calculate mode gcm_iv_mode[1:0]: 00: IDLE state ,this calculate do not have the process from iv to J0 01: by iv padding generating J0. On the mode, iv padding is 96 bits, so iv_length will be 96 bits 10: by GHASH calculate for iv generating J0, and this is not the last req for iv calculate 11: by GHASH calculate for iv generating J0, and this is the last req for iv calculate
3:2	R/W	0x0	CTR WIDTH Counter width for CTR mode 00: 16-bit Counter 01: 32-bit Counter

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES KEY SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

11.1.3.3.3. Task Descriptor Queue Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	PKC algorithm mode For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved For SM2： 00000: encryption 00001: decryption 00010: sign 00011: sign verify 00100: key exchange
15:8	/	/	/
7:0	R/W	0x0	Asymmetric algorithms operation width field It indicates how much width this request apply, as words.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.3.4. Security Operations

CE has two sets of complete registers, the base address of one register is CE_NS, is called non-secure world; the base address of the other register is CS_S, is called secure world. The configurations of two registers are independent each other. The task started by configuring the non-secure world register is called non-secure task; otherwise, called secure task. The difference between secure world and non-secure world has mainly two aspects.

- Non-secure CPU only can access the registers of non-secure world; secure CPU can access the registers of non-secure world and the registers of secure world;
- Non-secure task can not access any secure domain in system, such as KEYSRAM and SID. But secure task can.

For example, if the EK stored in KEYSRAM needs to do a MD5 operation, the task requires CE to read the EK of KEYSRAM during execution, so it can only access secure-world registers by secure CPU to configure and start the task.

11.1.3.5. Task Parallel

Algorithms are divided into 4 types: symmetric, HASH/RBG, asymmetric, and RAES. These four algorithms can run in parallel. Among these 4 types, the task request and complete time are not sure. If one type uses the outcome of another type, software should make sure to start one type after another type is finished.

Each type has a task queue with 8 elements for requests. Tasks in each queue are handled in sequence. If software makes several requests with the same type, these tasks will be executed in request sequence. If software makes several requests with different types, these tasks will be executed in parallel.

CE supports 4 virtual channels with ID 0-3 in each world. Because parallel tasks would finish out of order, software should make different type request with different channel id, which results in generating different interrupt status bit.

11.1.3.6. PKC Microcode

PKC module supports RSA, ECC, SM2 algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC/SM2 encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC/SM2 are implemented as microcode in PKC module. The encryption, decryption, sign, verify operations of asymmetric algorithms are composed with certain fixed microcode with hardware.

11.1.3.7. PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.
For RSA, parameters should be at the order of key, modulus, plaintext.
For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.
For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.
For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.
For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.
For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.
For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.
For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

11.1.3.8. Error Check

After CE reads the task descriptor, CE can monitor error during algorithm operation. When the error is monitored, CE will do the following operations:
The task will pause immediately
Generates interrupt
The corresponding channel of the task status register is Fail
The corresponding channel bit of error status register can be read error number

The error number has the following types.

Code	Name	Description	Algorithms Type
0x01	algorithm not support	The algorithm type is not supported.	All
0x11	KEYSRAM access error	In AES decryption task, RSSK is used as plaintext, the DST address is not in KEYSRAM space.	AES decryption
0x31	data length error	Input size or output size configuration size error.	All
0x42	DRBG internal state invalid	The internal status ID is invalid in the task. For example: 1. When executing the instantiate, an internal status that has been instantiated but not destroyed is used. 2. When executing the reseed/generate/ uninstantiate, an internal status that has not been used and has been destroyed is used.	DRBG
0x44	DRBG entropy or nonce missing	The size of entropy or nonce required for the task is 0.	DRBG
0x46	DRBG does not support prediction resistance in current instantiate	The task requests prediction resistance, but the used internal status is instantiate, prediction resistance enable has not been signed.	DRBG

11.1.3.9. Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24 MHz ~ 200 MHz
m_clk	MBUS clock	24 MHz ~ 400 MHz

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

ce_clk	CE work clock	24 MHz ~ 300 MHz
osl_clk	TRNG sample clock	<3 MHz

11.1.4. Register List

Module Name	Base Address
CE_NS	0x01904000
CE_S	0x01904800

Register Name	Offset	Description
CE_TDA	0x0000	Task Descriptor Address
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_TSR	0x0014	Task Status Register
CE_ESR	0x0018	Error Status Register
CE_DRL	0x001C	DRBG Request Limit Register
CE_SCSA	0x0024	Symmetric Algorithm DMA Current Source Address(For CE_S only)
CE_SCDA	0x0028	Symmetric Algorithm DMA Current Destination Address(For CE_S only)
CE_HCSA	0x0034	HASH Algorithm DMA Current Source Address(For CE_S only)
CE_HCDA	0x0038	HASH Algorithm DMA Current Destination Address(For CE_S only)
CE_ACSA	0x0044	Asymmetric Algorithm DMA Current Source Address(For CE_S only)
CE_ACDA	0x0048	Asymmetric Algorithm DMA Current Destination Address(For CE_S only)
CE_XCSA	0x0054	XTS Algorithm DMA Current Source Address(For CE_S only)
CE_XCDA	0x0058	XTS Algorithm DMA Current Destination Address(For CE_S only)

11.1.5. Register Description

11.1.5.1. 0x0000 CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Task Descriptor Address Must be word address.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.5.2. 0x0008 CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

11.1.5.3. 0x000C CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W1C	0x0	Channel 3 Task Status Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	Channel 2 Task Status Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	Channel 1 Task Status Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	Channel 0 Task Status Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.5.4. 0x0010 CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	Task Load for Channel RAES Type Read as 1: CE is busy to load another task, or the task queue is full. Writing this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
2	R/W	0x0	Task Load for Channel ASYM Type Read as 1: CE is busy to load another task, or the task queue is full. Writing this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
1	R/W	0x0	Task Load for Channel HASH/RBG type Read as 1: CE is busy to load another task, or the task queue is full. Writing this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
0	R/W	0x0	Task Load for Channel SYMM type Read as 1: CE is busy to load another task, or the task queue is full. Writing this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect

11.1.5.5. 0x0014 CE Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	indicate which channel in run for XTS 00: task channel0 01: task channel1 10: task channel2 11: task channel3
5:4	R	0x0	indicate which channel in run for asymmetric 00: task channel0 01: task channel1 10: task channel2

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: task channel3
3:2	R	0x0	indicate which channel in run for digest 00: task channel0 01: task channel1 10: task channel2 11: task channel3
1:0	R	0x0	indicate which channel in run for symmetric 00: task channel0 01: task channel1 10: task channel2 11: task channel3

11.1.5.6. 0x0018 CE Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31:data length error 0x42: DRBG internal state invalid 0x44: DRBG Entropy or Nonce missing 0x46: DRBG do not support Prediction Resistance in current Instantiate others: reserved
23:16	R	0x0	Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31:data length error 0x42: DRBG internal state invalid 0x44: DRBG Entropy or Nonce missing 0x46: DRBG do not support Prediction Resistance in current Instantiate others: reserved
15:8	R	0x0	Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31:data length error 0x42: DRBG internal state invalid 0x44: DRBG Entropy or Nonce missing 0x46: DRBG do not support Prediction Resistance in current Instantiate others: reserved
7:0	R	0x0	Error code for task channel 0

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31:data length error 0x42: DRBG internal state invalid 0x44: DRBG Entropy or Nonce missing 0x46: DRBG do not support Prediction Resistance in current Instantiate others: reserved

11.1.5.7. 0x001C CE DRBG Request Limit Register (Default: 0x0000_0000)

Offset: 0x001C			Register Name: CE_DRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The register remains unchanged before all DRBG task is completed. Only when there are no tasks to be completed, the register can be configured.

11.1.5.8. 0x0024 CE Symmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current source address read by DMA.

11.1.5.9. 0x0028 CE Symmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current destination address written by DMA.

11.1.5.10. 0x0034 CE HASH Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_HCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current source address read by DMA.

11.1.5.11. 0x0038 CE HASH Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_HCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current destination address written by DMA.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.1.5.12. 0x0044 CE Asymmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_ACSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current source address read by DMA.

11.1.5.13. 0x0048 CE Asymmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_ACDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current destination address written by DMA.

11.1.5.14. 0x0054 CE XTS Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current source address read by DMA.

11.1.5.15. 0x0058 CE XTS Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current destination address written by DMA.

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.

11.2. Security ID

The Security ID(SID) is 2 Kbits electrical efuse for saving key, which includes chip ID, thermal sensor, and security key, etc.

The SID module has the following features:

- The module register is non-secure forever, and the efuse has secure zone and non-secure zone
- A fuse only can program one time

 Copyright©2023 Allwinner Technology Co.,Ltd. All Rights Reserved.